Hardware Documentation

FSSMBB
F&S SMARC V2.2 Carrier Board
for HW Revision 1.20

Version 007/09.2026

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About This Document

This document describes how to use the F&S SMARC Base Board (further named as carrier) with mechanical and electrical information. The latest version of this document can be found at: https://www.fsembedded.com/en.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/09.2024	-	-	All	Initial Version	SM
002/02.2025	-	M	All	New Revision, new template	SM
003/02.2025	-	-	-	Change filename	SM
005/10.2025	-	M	4.2	Change link	SM
006/03.2026	-	 M A A R M M M M M M M M M A M A M M A	 All All All All 1.2 1.2, 1.3.1 1.3.1, 1.3.2 1.4.1 1.4.2 1.4.3 1.5 1.6.3 1.8 1.10.2 1.12 1.13 1.14 1.16 1.19.1 1.19.2	New Rev. 1.20 Update hyperlinks Added SMARC pins to tables Used interfaces added, for connectors without pin description Micro SD and Mini PCI Express is removed Added Information New outline Connectors added; connector type & descriptions changed Description and pining changed Change to M.2 Change block diagram Pos 4 added to SW5 SER2 description added USB description changed New CSI1 pinout SerDes added Added pining of J26 Chapter M.2 added Pinning J24 changed SMARC fan description changed M.2 fan added	SM
007/09.2026		A	1.9.4	Add comment that display port is not functional in rev 1.20	SM

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1 Overview

1.1 Additional Documentation

The carrier follows the SMARC V2.2 specification and is designed to support F&S SMARC modules (further called module). The latest versions of the documents can be found on https://www.fsembedded.com/en

1.2 General Parameter

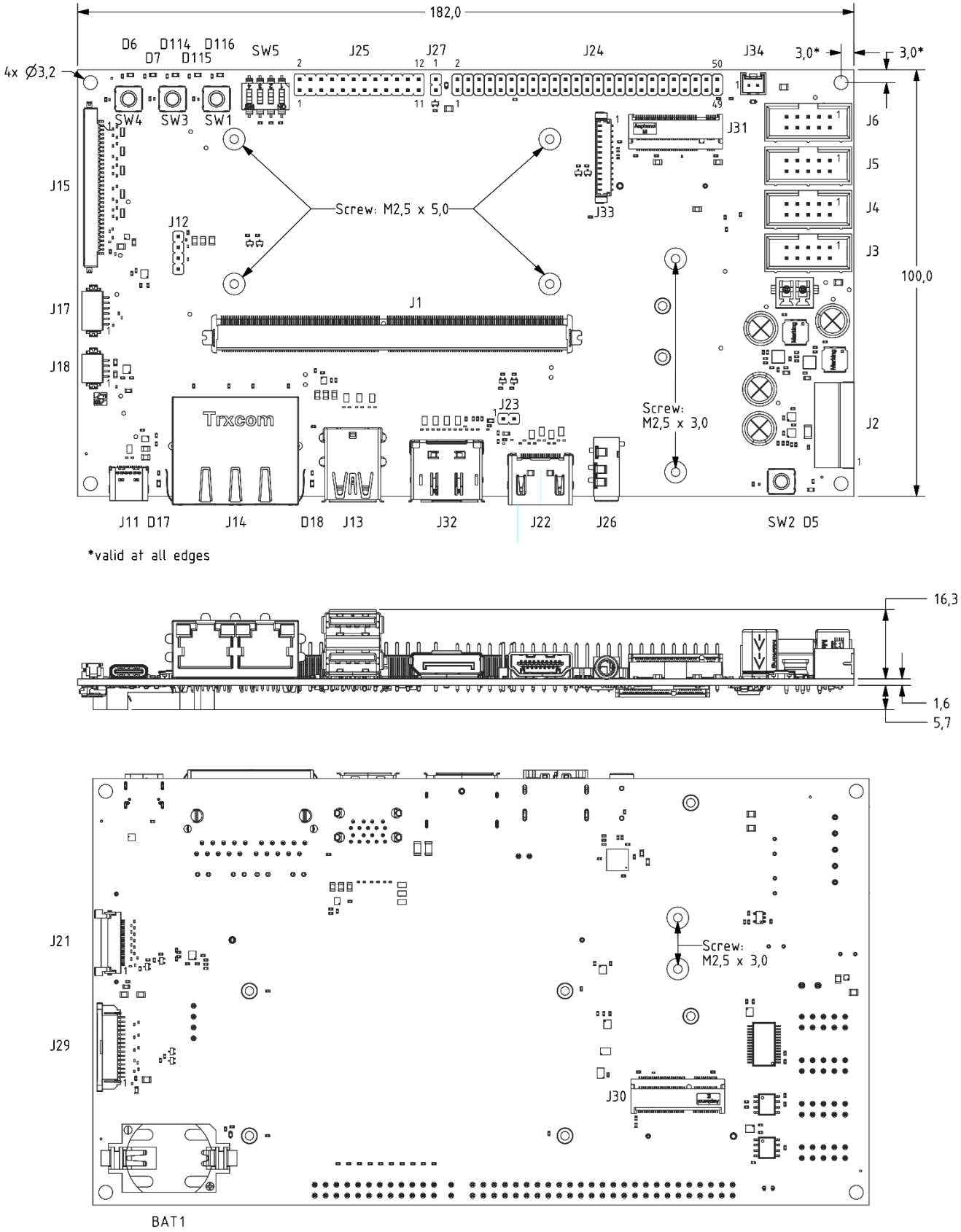
Parameter	Description
Dimension	182.0 mm x 100.0 mm x 25.5 mm
Weight	≈ 130.0 g
Operating Temperature	-20.0 °C … +70.0 °C
Mounting Holes	4x Ø 3.2 mm
Mounting Holes SMARC Module	4x M 2.5 (recommended screw length: 5.0 mm)
M.2 Key M Module Sizes	2280 (2230, 3030)[1]
M.2 Key E Module Sizes	2242, 3042 (2230, 3030) [1]
Mounting Hole M.2	1x M 2.5 (recommended screw length: 3.0 mm)
Supported SMARC Interfaces	GPIO SER 0 to 3 SDIO SPI 0 to 1 PCIe A to D SerDes 0 CAN 0 to 1 USB 0 to 4 GBE 0 to 1 LVDS/DSI 0 to 1 HDMI DP 0 CSI 0-1 I2S 0, 2

[1] Mounting option

Table 1: General parameter

1.3 Dimensions and Connectors

1.3.1 Technical Drawing



Note: All dimensions are in mm.

Figure 1: Technical drawing

1.3.2 Connector Description

Ref.	Description	Connector Type	Counter Part
J1	Board-to-board connection	MXM3 314pos RM: 0,50mm	
J2	Power Input	Phoenix Contact, MC 1,5/5-G-3,81	Phoenix Contact, MC 1,5/ 5-ST-3,81[1]
J3	UART A (RTS/CTS)	2x5 RM: 2.54 mm, shrouded	
J4	UART B	2x5 RM: 2.54 mm, shrouded	
J5	UART C	2x5 RM: 2.54 mm, shrouded	
J6	CAN A	2x5 RM: 2.54 mm, shrouded	
J11	USB0 (USB 2.0, OTG)	Type C	
J12	USB5 (USB 2.0)	1x5 pin header, RM: 2.54 mm	
J13	USB2 (top) & USB3 (bottom) (USB 3.0)	2x Type A 3.0	
J14	GBE0 (right) & GBE1 (left)	2x RJ45 Gigabit Ethernet Connector	
J15	LVDS0&1 incl. I2C_LCD	Hirose, MDF76GW-30S-1H	Hirose, MDF76-30P-1C[1]
J17	General Purpose Connector (I2C_LCD, GPIO, 3.3 V)	Hirose, DF13-06	Hirose, DF13-6S-1.25C
J18	Backlight	Hirose, DF13-04	Hirose, DF13-4S-1.25C[1]
J21	DSI CAM1	Hirose, FH12A-22S-0.5H	FFC/FPC, 22pos, pitch: 0.5 mm, thickness: 0.3 mm
J22	HDMI	Type A	
J23	HDMI CEC & HEC	1x2 pin header, RM: 2.54 mm	
J24	Feature Connector	2x25 pin header, RM: 2.54 mm	
J25	SMARC Signal Connector	2x12 pin header, RM: 2.54 mm	
J26	Audio Jack	4-pin, 3.5 mm Audio Jack	
J27	5.0 V SMARC cooling fan	1x2 pin header, RM: 2.54 mm	
J29	DSI CAM0	Amphenol, SFW15R-1	FFC/FPC, 15pos, pitch: 1.0 mm, thickness: 0.3 mm[1]
J30	M.2	Key E	
J31	M.2	Key M	
J32	Display Port		
J33	SerDes	Molex, 533981371	Molex, 510211300
J34	5.0 V external (M.2 cooling fan)	Amphenol, G8610211X1T2HR	Amphenol, G862H021AEU
SW1	Force Recovery	Tactile button	
SW2	Power	Tactile button	
SW3	Sleep	Tactile button	
SW4	Reset	Tactile button	
SW5	Boot Select / M.2 Key E enable	DIP switch	
D5	V_MOD Indicator	LED yellow	
D6	V_5V0_PWON Indicator	LED yellow	
D7	V_3V3_STBY Indicator	LED yellow	
D114	M.2 Key M LED1	LED yellow	
D115	M.2 Key E LED1	LED yellow	
D116	M.2 Key E LED2	LED yellow	
D17	GBE0 L100	LED yellow	
D18	GBE1 L100	LED yellow	
BAT1	RTC Battery	CR2032 3.0V	

[1] Connectors and preassembled cables are available for purchase at https://www.fsembedded.com/en.

Table 2: Connector description

1.4 Power Management

1.4.1 Power Supply (J2)

The power (PWR) supply for the carrier must be connected at J2. There are three different supplies.
The RTC (Real Time Clock) and the backlight (BL) only must be connected when needed.

If higher input voltages are needed, the ADP-NT24V4[1] power supply module can be directly connected.

[1] More Information can be found on https://www.fsembedded.com/en.

Pin	Signal Name	Voltage	Description
1	GND		
2	V_3V0_RTC	3.0V	Voltage input for the RTC, parallel to BAT1 see 2.15
3	V_IN_RAW	5.0V	Voltage Input, max. 8A[1]
4	GND		
5	V_IN_BL	3.3V to 24.0V	External backlight supply, connected to J18 (see chapter 1.9.2)

[1] Maximum possible power consumption of the carrier: 10 A. Please see chapter 1.4.3.

Table 3: J2 (PWR) pin description

1.4.2 System Control

There are various buttons (see Table 4) to control the carrier and the mounted SMARC module. As simple indicators, three LEDs (see Table 5) show the active voltages.

Ref	Signal Name	J1 Pin#	Description
SW1	FORCE_RECOV#	S155	Allows restoring from USB0 or invoke the native force recovery on the module
SW2	POWER_BTN#	P128	Start standby voltage rails on module
SW3	SLEEP#	S149	
SW4	RESET_IN#	P127	Triggers a forced reset

Table 4: Button description

Ref	Signal Name	Voltage	Description
D5	V_MOD_IN	5.0 V	Main supply for the SMARC module
D6	V_5V0_PWON	5.0 V	Supply domain for USB, CAM, HDMI, Backlight, & 5V ext. (Fan)
D7	V_3V3_STBY	3.3 V	Supply domain for UART, CAN, M.2 Key E, Audio, LVDS, DP

Table 5: Indicator LED description

1.4.3 Power Usage Block Diagram

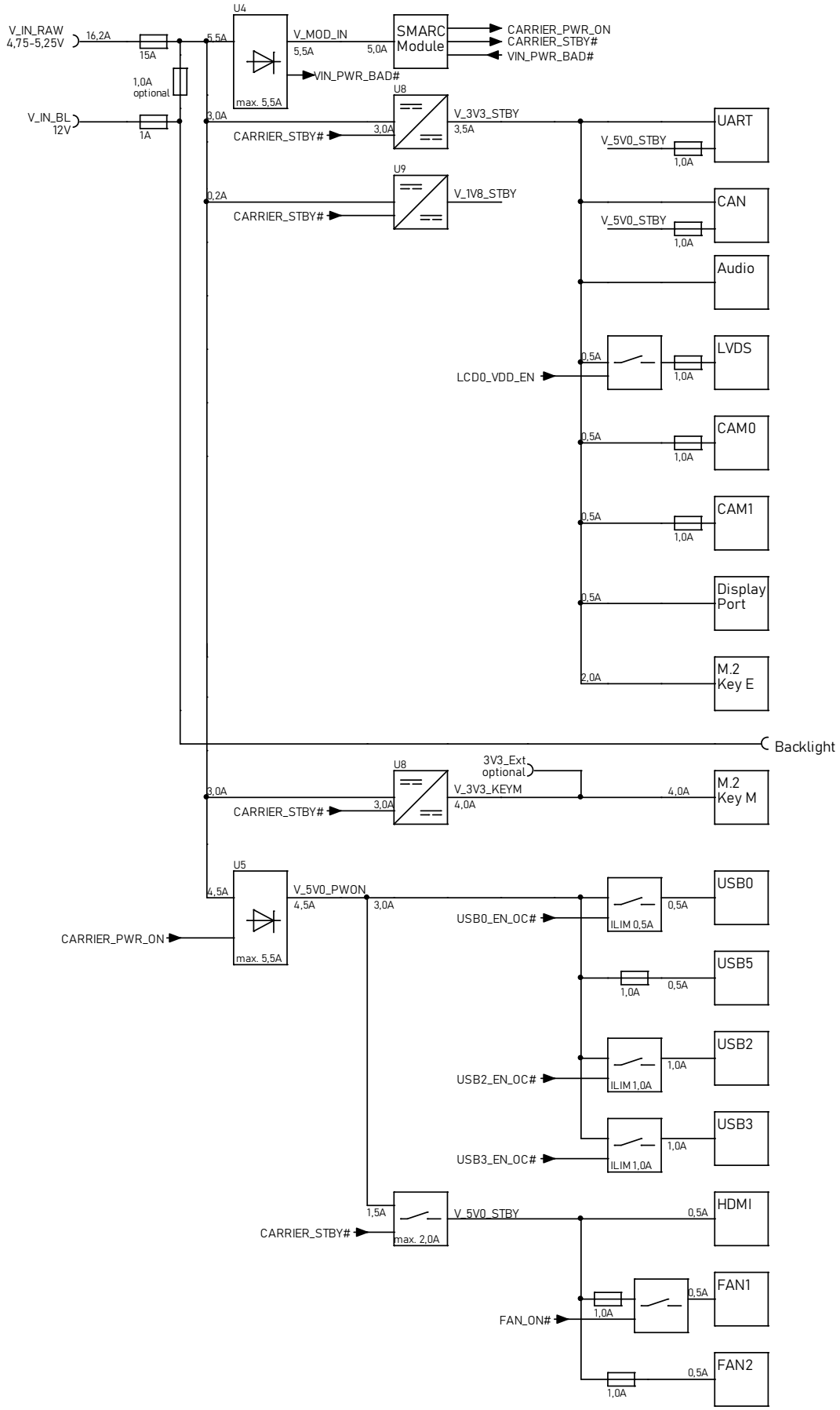


Figure 2: Power usage block diagram

1.5 Boot Select

The boot select signals are connected to dip switch SW5. The selectable boot sources are listed in table 7 and depend on the module.

Pos	J1 Pin#	Signal Name
1	P123	BOOT_SEL2#
2	P124	BOOT_SEL1#
3	P125	BOOT_SEL0#
4		M.2 Key E enable ON: PCIe A and SER2 are only available on M.2 Key E (J30) OFF: PCIe A is connected to M.2 Key M (J31), SER2 is additionally available as RS485 at J5.

Table 6: SW5 (BOOT SEL & KEY E EN) description

	Boot select dip position			
#	2	1	0	Boot source
0	ON	ON	ON	Not available on this carrier
1	ON	ON	OFF	Carrier SD Card
2	ON	OFF	ON	Not available on this carrier
3	ON	OFF	OFF	Carrier SPI (CS0#)
4	OFF	ON	ON	Module device (NAND, NOR) – vendor specific
5	OFF	ON	OFF	Remote boot (GBE, serial) – vendor specific
6	OFF	OFF	ON	Module eMMC Flash
7	OFF	OFF	OFF	Module SPI

Table 7: Truth table boot device

1.6 UART

The carrier supports four serial ports (SER0 to SER3).
SER 3 is connected to the feature connector without transceiver (see chapter 1.16).

1.6.1 SER0 (RS232) (J3)

Pin	Signal Name	J1 Pin#	Voltage	Description
3	UART_A_RX	P130	5.5 V	
4	UART_A_RTS	P131	5.5 V	
5	UART_A_TX	P129	5.5 V	
6	UART_A_CTS	P132	5.5 V	
9	GND			
10	V_UART_5V0		5.0 V	Max. 1.0 A, fused

Table 8: J3 (SER0) pin description

1.6.2 SER1 (RS232) (J4)

Pin	Signal Name	J1 Pin#	Voltage	Description
3	UART_B_RX	P135	5.5 V	
5	UART_B_TX	P134	5.5 V	
9	GND			
10	V_UART_5V0		5.0 V	Max. 1.0 A, fused

Table 9: J4 (SER1) pin description

1.6.3 SER2 (RS485) (J5)

SER2 is parallel used on the M.2 Key E connector J30 (see chapter 1.14.1). To activate the port for RS485, SW5 switch no. 4 must be OFF (see chapter 1.5) and no module with UART should be connected to the connector J30.

Pin	Signal Name	Voltage	Description
3	UART_C_N		
4	UART_C_P		
9	GND		
10	V_UART_5V0	5.0 V	Max. 1.0 A, fused

Table 10: J5 (SER2) pin description

1.7 CAN

The carrier supports two CAN ports. CAN0 is connected to a transceiver, CAN1 is directly connected to the feature connector (see chapter 1.16)

1.7.1 CAN0 (CAN FD) (J6)

Pin	Signal Name	Voltage	Description
1	V_CAN_5V0	5.0 V	Max. 1.0 A, fused
2	GND		
3	CAN_A_LOW		120 Ω terminated
4	CAN_A_HIGH		
5	GND		

Table 11: J6 (CAN) pin description

1.8 USB

The carrier supports six USB ports. Four are available on generic connectors. Two ports are used for the M2. Interfaces (see chapter 1.14).

1.8.1 USB0 (USB 2.0, OTG) (J11)

EN/OC- (Enable / Overcurrent) and OTG- (On the Go) functionalities are supported. The current is limited to 0.50 A. This port is used for recovery.

J11	SMARC	J1 Pin#
USB 2.0	USB0	P60, P61, P62, P64

Table 12: J11 (USB0) used interfaces

1.8.2 USB5 (USB 2.0) (J12)

The carrier does not support the EN/OC functionality for these ports.

Pin	Signal Name	J1 Pin#	Voltage	Description
1	USB15_VBUS		5.0 V	Max. 1.0 A, fused
2	USB5_D_N	S60		
3	USB5_D_P	S59		
4	GND			

Table 13: J12 (USB5) pin description

1.8.3 USB2 & USB3 (USB 3.0) (J13)

EN/OC functionality is supported. The current is limited to 1.0 A.

J13	SMARC	J1 Pin#
Top USB 2.0	USB 2	P69, P70
Top USB 3.0	USB 2	S71, S72, S74, S75
Bottom USB 2.0	USB 3	S68, S69
Bottom USB 3.0	USB 3	S62, S63, S65, S66

Table 14: J13 (USB2&3) used interfaces

1.8.4 USB4 (USB 2.0) (J30)

USB4 is connected to the M.2 Key E port (see chapter 1.14.1).
EN/OC is not supported.

1.8.5 USB1 (USB 2.0) (J31)

USB1 is connected to the M.2 Key M port (see chapter 1.14.2).
EN/OC is not supported.

1.9 Display

The carrier supports HDMI, two 8-bit LVDS display signals and Display Port for video applications.

1.9.1 LVDS0 & LVDS1 (8-bit) (J15)

Pin	Signal Name	J1 Pin#	Voltage	Description
1	LVDS0_D0_N	S126		
2	LVDS0_D0_P	S125		
3	LVDS0_D1_N	S129		
4	LVDS0_D1_P	S128		
5	LVDS0_D2_N	S132		
6	LVDS0_D2_P	S131		
7	GND			
8	LVDS0_CLK_N	S135		
9	LVDS0_CLK_P	S134		
10	LVDS0_D3_N	S138		
11	LVDS0_D3_P	S137		
12	LVDS1_D0_N	S112		
13	LVDS1_D0_P	S111		
14	GND			
15	LVDS1_D1_N	S115		
16	LVDS1_D1_P	S114		
17	GND			
18	LVDS1_D2_N	S118		
19	LVDS1_D2_P	S117		
20	LVDS1_CLK_N	S109		
21	LVDS1_CLK_P	S108		
22	LVDS1_D3_N	S121		
23	LVDS1_D3_P	S120		
24	GND			
25	I2C_LCD_SDA_3V3	S140	3.3 V	
26	LCD0_IRQ_3V3	S127	3.3 V	SMARC signal: LCD0_BKLT_EN

27	I2C_LCD_SCL_3V3	S139	3.3 V	
28	LCD0_RST_3V3	S141	3.3 V	SMARC signal: LCD0_BKLT_PWM
29 30	V_LCD_3V3_F1A		3.3 V	Max. 1.0 A, fused; switched with Signal LCD0_VDD_EN

Table 15: J15 (LVDS) pin description

1.9.2 Backlight Supply (J18)

J18 is meant to supply a backlight (BL) with 5.0 V, especially designed for F&S displays. For other displays, the connector can be reassigned to fit a large variety of products.

Pin	Signal Name	Voltage	Description
1	V_BL	up to 24.0 V	Max. 1.0 A, fused; connected to J2 pin 5 [1] (see chapter 1.4.1)
2	V_BL	up to 24.0 V	Optional LCD1_BKLT_EN (3.3 V)
3	GND		Optional LCD1_BKLT_PWM (3.3 V)
4	GND		

[1] As a mounting option V_BL can be connected to V_5V_IN on J2

Table 16: J18 (BL) pin description

1.9.3 HDMI (J22, J23)

The carrier supports one HDMI interface.

J22	SMARC	J1 Pin#
Video	HDMI	P92, P93, P95, P96, P98, P99, P101, P102, P104
I2C	HDMI CTRL	P105, P106

Table 17: J22 (HDMI) used interfaces

Pin	Signal Name	Comment
1	HDMI_CEC	Connected to J22, for development purpose only.
2	HDMI_HEC	

Table 18: J23 (HDMI) pin description

1.9.4 Display Port (J32)

Display Port is not functional in rev 1.20! Do not connect if connector is available. This will be fixed in the next revision.

The carrier supports one Display Port (DP) interface.

J32	SMARC	J1 Pin#
Video	DP 0	S93, S94, S96, S97, S98, S99, S100, S102, S103, S105, S106

Table 19: J32 (DP) used interfaces

1.10 Camera

The carrier supports two CSI camera interfaces.

1.10.1 CSI0 (1-lane) (J29)

CSI0 is a single lane CSI camera interface, which follows the Raspberry Pi camera connector layout.

Pin	Signal Name	J1 Pin#	Voltage	Comment
1	GND			
2	CSI0_D0_N	S12		
3	CSI0_D0_P	S11		
4	GND			
5	CSI0_D1_N	S15		

6	CSI0_D1_P	S14		
7	GND			
8	CSI0_CLK_N	S9		
9	CSI0_CLK_P	S8		
10	GND			
11	CAM0_PWR#	P108	3.3 V	
12	CAM0_RST#	P110[1]	3.3V	Optional: Master Clock
13	I2C_CAM0_SCL	S5	3.3 V	
14	I2C_CAM0_SDA	S7	3.3 V	
15	V_3V3_STBY		3.3 V	Max. 1.0 A, fused

[1] Optional connected to CAM_MCK (J1 pin S6)

Table 20: J29 (CSI0) pin description

1.10.2 CSI1 (2-lane) (J21)

CSI1 is a 2-lane CSI camera interface that follows the Raspberry Pi camera connector layout.

Pin	Signal Name	J1 Pin#	Voltage	Description
1	GND			
2	CSI1_D0_N	P8		
3	CSI1_D0_P	P7		
4	GND			
5	CSI1_D1_N	P11		
6	CSI1_D1_P	P10		
7	GND			
8	CSI1_CLK_N	P4		
9	CSI1_CLK_P	P3		
10	GND			
11	CSI1_D2_N	P14		
12	CSI1_D2_P	P13		
13	GND			
14	CSI1_D3_N	P17		
15	CSI1_D3_P	P16		
16	GND			
17	CAM1_PWR#	P109	3.3 V (1,8 V[1])	
18	CAM1_RST#	P111[2]	3.3 V	Optional: Master Clock
19	GND			
20	I2C_CAM1_SCL		3.3 V (1,8 V[1])	
21	I2C_CAM1_SDA		3.3 V (1.8 V[1])	
22	V_CAM1_F1A		3.3 V (5.0 V[1])	Max. 1.0A, fused

[1] Mounting option

[2] Optional connected to CAM_MCK (J1 pin S6)

Table 21: J21 (CSI1) pin description

1.11 Ethernet (Gigabit) (J14)

The carrier supports two gigabit ethernet ports.

J14	SMARC	J1 Pin#
Left RJ45	GBE0	P19, P20, P23, P24, P26, P27, P29, P30
Left LED yellow	GBE0_LINK_ACT#	P25
Left LED green	GBE0_LINK1000#	P22
Right RJ45	GBE1	S17, S18, S20, S21, S23, S24, S26, S27
Right LED yellow	GBE1_LINK_ACT#	S31
Right LED green	GBE1_LINK1000#	S22

Table 22: J14 (GBE) used interfaces

The two separate LEDs (D17, D18) are connected to the GBE LINK100# signals.

1.12 SerDes (J33)

The carrier supports one SerDes port. The connector is designed to fit our SFP Adapter (ADP-SFP1). When the SerDes connector is mounted, the 3rd PCI on the M.2 Key M interface is not connected.

Pin	Signal Name	J1 Pin#	Voltage	Comment
1	n.c.			
2	I2C_GP_SDA	S49	3.3 V	
3	I2C_GP_SCL	S48	3.3 V	
4			3.3 V	PU 10k
5	SERDES_TX_P	S29		
6	SERDES_TX_N	S30		
7	SERDES_RX_P	S32		
8	SERDES_RX_N	S33		
9	GND			
10	n.c.			
11	n.c.			
12	SERDES_RST#	S77		
13	V_3V3_STBY		3.3 V	

Table 23: J33 (SerDes) pin description

1.13 Audio (J26)

A SGTL5000 audio codec is applied on the carrier. Head- and microphone signals are connected to J26 (see Table 25). Line in & out signals are connected to the feature connector (see chapter 1.16)

Audio codec	SMARC	J1 Pin#
I2S	I2S0	S39, S40, S41, S42
I2C	I2C GP	S49, S48

Table 24: Audio codec used interfaces

Pin	Signal Name	Description
1	AU_MICIN	Microphone IN
2	AU_HP_R	Headphones RIGHT
3	AU_HP_L	Headphones LEFT
4	GND	

Table 25: J26 (Audio) pin description

1.14 M.2

The carrier supports two M.2 sockets for Key E and Key M modules.

1.14.1 M.2 Key E (J30)

The key E socket has the purpose of connecting Wi-Fi / BT modules or an SD card.
The PCIe on this interface is shared with the M.2 Key M (J31) socket. The UART is shared is shared with the RS485 port on J5. To activate the PCIe and UART on this socket, switch no. 4 on SW5 must be set to “ON” (see Table 6).
Supported module sizes: 2242, 3042 (2230, 3030) [1]

[1] Mounting option

J30	SMARC	J1 Pin#
USB	USB 4	S35, S36
PCIe0	PCIE A[1]	P75, P78, P83, P84, P86, P87, P89, P90
PCIe1	n.c.	
UART	SER 2[2]	P136, P137, P138, P139
SDIO	SDIO	P34, P36, P39, P40, P41, P42
I2S	I2S2	S50, S51, S52, S53
SMB	I2C GP	S49, S48
LED1	Connected to LED D115	
LED2	Connected to LED D116	

[1] PCIe is shared with M.2 Key M (J31)

[2] UART is shared with J5.

Table 26: J30 (M.2 Key E) used interfaces

1.14.2 M.2 Key M (J31)

The key M socket has the purpose of connecting AI modules like our ADP-ARAM2 or large flash storages.
The first PCIe on this interface is shared with the M.2 Key E (J30) socket. To activate the this PCIe for this socket, switch no. 4 on SW5 (see Table 6) must be set to “OFF” (see Table 6).
The fourth PCIe slot is also occupied by SerDes on J33 (see chapter 1.12). When J33 is mounted, PCIe3 ist not available on this socket.
Supported module sizes: 2280 (2230, 3030)[1]

[1] Mounting option

J31	SMARC	J1 Pin#
USB	USB 1	P65, P66
PCIe0	PCIE A[1]	P75, P78, P83, P84, P86, P87, P89, P90
PCIe1	PCIE B	S87, S88, S90, S91
PCIe2	PCIE C	S78, S79, S81, S82
PCIe3	PCIE D[2]	S29, S30, S32, S33
SMB	I2C GP	S49, S48
LED1	Connected to LED D114	

[1] PCIe is shared with M.2 Key E (J30)

[2] PCIe is shared with SerDes (J33)

Table 27: J31 (M.2 Key M) used interfaces

1.15 General Purpose Connector (J17)

The general purpose (GP) connector is designed to connect a peripheral device like a touch sensor.

Pin	Signal Name	J1 Pin#	Voltage	Description
1	V_3V3_STBY		3.3 V	
2	I2C_LCD_SDA	S139	3.3 V	
3	I2C_LCD_SCL	S140	3.3 V	
4	GPIO12	S142	3.3 V	
5	GPIO13	S123	3.3 V	
6	GND			

Table 28: J17 (GP) pin description

1.16 Feature Connector (J24)

The feature connector (FCON) includes several signals and buses for easy access.

Pin	Signal Name	J1 Pin#	Voltage	Description
1	V_3V3_STBY		3.3 V	
2	V_5V0_STBY		5.0 V	
3	SPI0_CLK	P44		
4	SPI0_CS0#	P43		
5	SPI0_MOSI	P46		
6	SPI0_MISO	P45		
7	RSVD_3	P73		
8	GPIO4	P112		
9	RSVD_2	P72		
10	AU_MCLK			Audio master clock
11	GND			
12	FAN_ON#		5.0 V	Connect to GND (pin 11) to turn SMARC fan always on
13	SER3_TX	P140		
14	RSVD_1	S4		Optional SMARC fan PWM control signal
15	SER3_RX	P141		
16	I2C_GP_SCL	S48		
17	I2C_GP_SDA	S49		
18	SPI0_CS1#	P31		
19	SPI1_CS0#	P54		
20	SPI1_CS1#	P55		
21	SPI1_CLK	P56		
22	SPI1_MOSI	P58		
23	SPI1_MISO	P57		
24	CAN1_RX	P146		No transceiver, no termination
25	V_1V8_STBY		1.8 V	
26	CAN1_TX	P145		No transceiver, no termination
27	GND			
28	V_1V8_STBY		1.8 V	
29	I2C_PM_SDA	P122		
30	I2C_PM_SCL	P121		
31	GPIO5	P113		
32	GPIO6	P114		
33	GPIO7	P115		
34	GPIO8	P116		

35	GPIO9	P117		
36	GPIO10	P118		
37	GND			
38	GPIO11	P119		
39	V_3V3_STBY		3.3 V	
40	V_5V0_STBY		5.0 V	
41	AU_MICIN			Microphone IN to audio codec, parallel to J26
42	GND			
43	n.c.			
44	FCON_A_LIN_R			LINE IN right to audio codec
45	FCON_A_LOUT_R			LINE OUT right from audio codec
46	GND			
47	GND			
48	FCON_A_LIN_L			LINE IN left to audio codec
49	FCON_A_LOUT_L			LINE OUT left from audio codec
50	GND			

Table 29: J24 (FCON) pin description

1.17 SMARC Signal Connector (J25)

The SMARC signal connector includes unused signals. A 1 kΩ pull down is provided for some signals.

Pin	Signal Name	J1 Pin#	Description
1	GBE0_SDP	P6	IEEE 1588 trigger signal for hardware implementation of PTP (Precision Time Protocol)
2	n.c.		
3	GBE1_SDP	P5	IEEE 1588 trigger signal for hardware implementation of PTP (Precision Time Protocol)
4	n.c.		
5	USB3_ID	S104	Input pin to announce OTG device insertion on USB port 3.
6	1 kΩ pull down		
7	USB4_EN_OC#	P76	USB over-current sense for USB port 4, low active
8	1 kΩ pull down		
9	RESET_OUT#	P126	General purpose reset output to carrier board, low active
10	1 kΩ pull down		
11	WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active
12	1 kΩ pull down		
13	SMB_ALERT#	P1	SM Bus Alert# (Interrupt) Signal, low active
14	1 kΩ pull down		
15	LID#	S148	Lid open/close indication to module. LOW: lid closure. Carrier floats the line in inactive state
16	1 kΩ pull down		
17	CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.
18	1 kΩ pull down		
19	CHARGING#	S151	Held LOW by carrier during battery charging. Carrier to float the line when charge is complete.
20	1 kΩ pull down		
21	TEST#	S157	Held LOW by carrier to invoke module vendor specific test functions.
22	1 kΩ pull down		
23	BATLOW#	S156	Battery low indication to module. Carrier to float the line in inactive state. Low active.
24	1 kΩ pull down		

Table 30: J25 pin description

1.18 RTC Battery (BAT1)

To supply the RTC on the module, there is a CR2032 battery socket for a 3V lithium cell on the carrier. The battery is connected in parallel to J2 pin 2 (see Table 3).

Note: The battery cell is not part of the carrier.

1.19 Cooling

1.19.1 SMARC Module Fan (J27)

J27 is a connector to supply a fan for the SMARC module. The fan can be controlled through a PWM signal from the module pin S4. The control signal is also available on the Feature Connector J24 pin 12(see Table 29).
For an always on application, place a jumper over pin 11 and pin 12 of J24 (see Table 29).

Pin	Signal Name	Voltage	Description
1	GND		
2	V_5V0_STBY	5.0 V	Max. 1 A, fused; PWM controlled or always on

Table 31: J27 (SMARC fan) pin description

1.19.2 M.2 Key M Module Fan (J34)

The supply for the M.2 Key M cooling fan is always on.

Pin	Signal Name	Voltage	Description
1	GND		
2	V_5V0_STBY	5.0 V	Max. 1 A, fused; always on

Table 32: J34 (M.2 Key M fan) pin description

2 Characteristics

2.1 Absolute Maximum Ratings

Description	Min	Max	Unit
Power Input			
Supply voltage	0.00	6.00	V
Real time clock supply voltage	-0.50	6.50	V
Signal Input			
UART input voltage (SER0 to SER2)	-0.30	5.70	V
Signal input voltage from SMARC connector (SER, I2C, CAN, GPIO)	-0.50	4.60	V
I2S0 signal input voltage to Audio codec	-0.30	2.20	V
Input voltage CAN A signals	-58.00	58.00	V
USB0 input voltage	-0.50	29.00	V
USB0 CC signal input voltage	-0.50	3.60	V
Audio Line IN input voltage	-0.30	3.60	V

Table 33: Absolute maximum ratings

2.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ.	Max	Unit
General						
V_IN_RAW	Carrier supply voltage		4.75	5.00	5.25	V
V_3V0_RTC	RTC supply voltage		2.20	3.00	3.45	V
Storage						
T_{STORE}	Storage time	room temperature, no humidity control		6	months	
		t_{amb} = 25°C ± 5°C humidity max. 60%		12[4]	months	

[4] For longer storage time, vacuum dry packs are recommended.

Table 34: Recommended operating conditions

3 Packaging & Labels

3.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

3.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit https://www.fsembedded.com/en/support/serial-number-info-and-rma/.

4 Appendix

4.1 Second source rules

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