Hardware Documentation

PicoCOM™A9X
for HW Revision 1.20

Version 005
(2021-08-27)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCOM™A9X board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
14.12.2016	001	PicoCOMA9X		*	New document	KW
02.02.2017	002	PicoCOMA9X	A	3.2, 4.5	Add comments for VBUS pin USB CNX	KW
24.03.2017	003	PicoCOMA9X	M	4.1	Added two notes for 18Bit mode.	HF
13.03.2018	004	PicoCOMA9X	M R A	3.2 4.11 4.14, 5	Correct some PU Remove mounting option Add NAND, RTC	KW
26.08.2021	005	PicoCOMA9X	M	All	New Document Format	MD

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

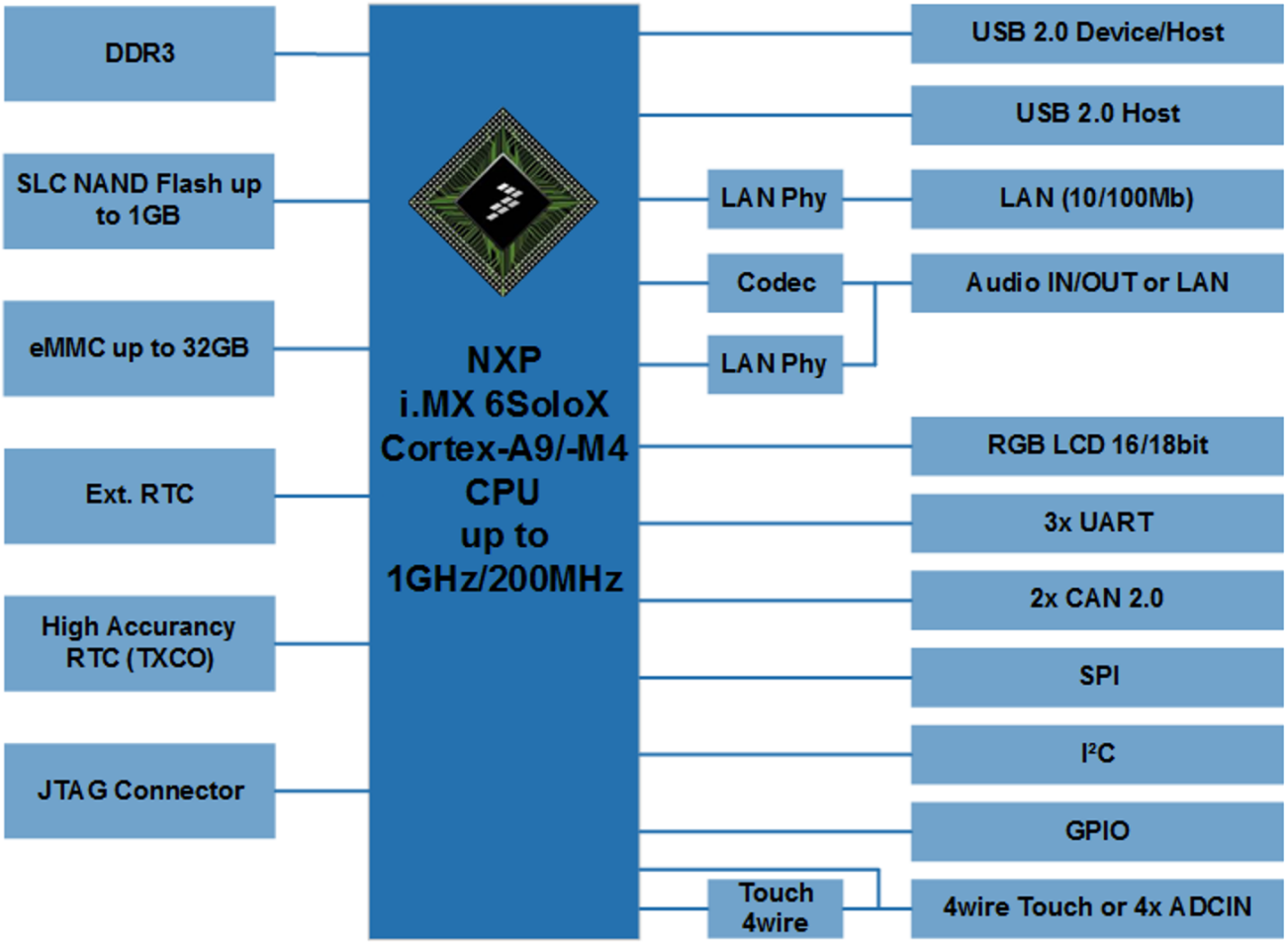


Figure 1: Block Diagram

2 Mechanical Dimension

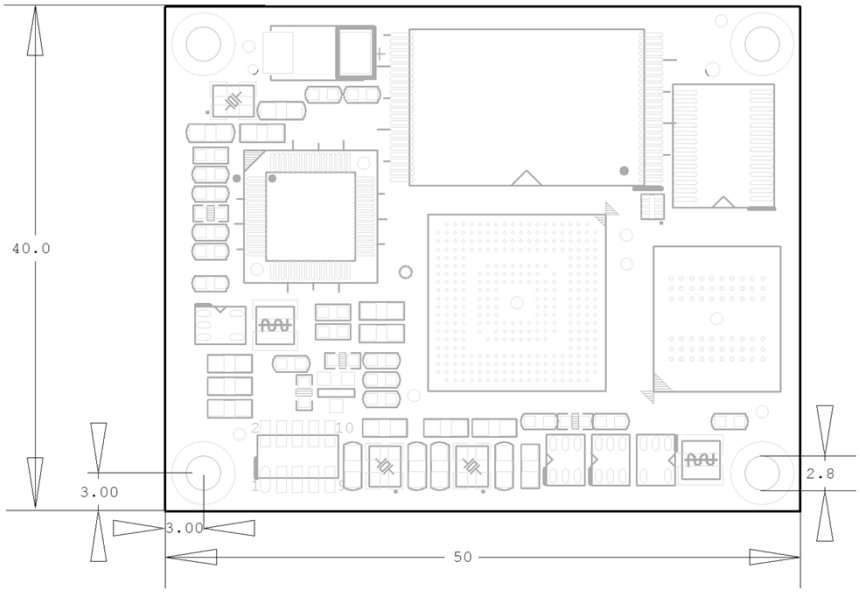


Figure 2: Top view (*Mounting holes are isolated from signal ground)*

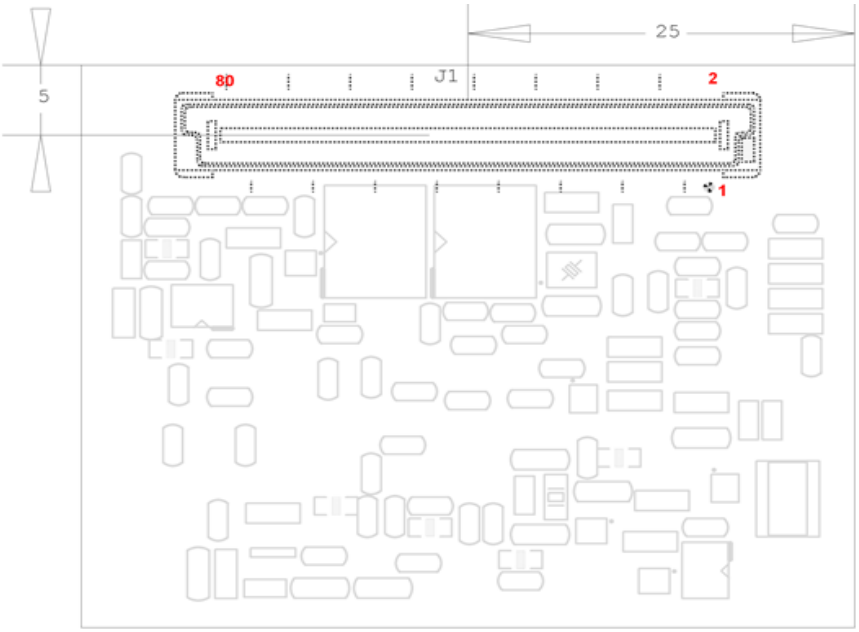


Figure 3: Bottom view

Dimensions	Description
Size	50mm x 40mm
PCB Thickness	1.6mm ± 0.16mm
Height of the parts on the top side	3mm
Height of the parts on the bottom side (without connectors)	2mm
Weight	~15gr

3 Interface and signal description

3.1 IO-Pin Limitations

PicoCOMA™9X is equipped with 48 pins that can be used as digital-IO. Most of these pins are multiplexed, so you have to make sure that these pins are used for one purpose only. For example, if you intend to use IO0 to IO3 you have to make sure that the COM2 is disabled.

Additionally there are some IO-Pins which are used internally and whose primary function can't be disabled completely. These pins may carry active signals while the device is booting, which must be kept in mind when connecting external hardware. For example even if you want to use IO14 to IO19 in your application these pins are configured for SD/MMC usage for a short period of time by the boot program to enable booting from SD-Card. Pins that could toggle during boot are tagged in the following table.

3.2 Interface Connector

The PicoCOM Module is equipped with:

Tyco Electronics 5177984-3 (80 pin, 0.8mm)

Connector from '0.8mm Free Height (FH) Connectors' series.

Mating connectors are:

5mm stacking height:	Tyco Electronics	5177983-3
9mm stacking height:	Tyco Electronics	5-5179009-3
13mm stacking height:	Tyco Electronics	5-5179010-3

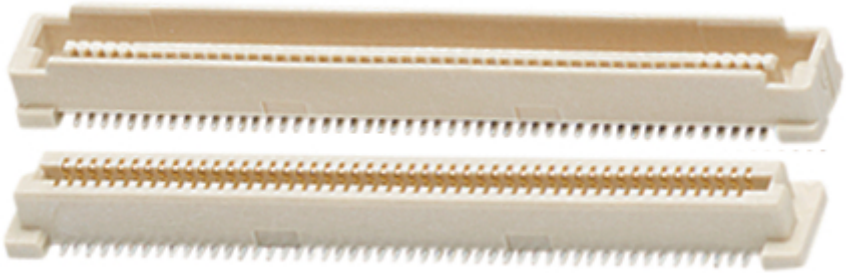


Figure 4: PicoCOM Interface Connector

3.3 Interface Connector

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	1	ETH0TX-	-	O	3.3V	Eth0 TX-
J1	2	ETH0RX-	-	I	3.3V	Eth0 RX-
J1	3	ETH0TX+	-	O	3.3V	Eth0 TX+
J1	4	ETH0RX+	-	I	3.3V	Eth0 RX+
J1	5	+V3.3S		PWR	3.3V	Power Supply Voltage
J1	6	+V3.3S		PWR	3.3V	Power Supply Voltage
J1	7	GND		PWR	GND	
J1	8	GND		PWR	GND	
J1	9	BATT		PWR	3.3V	RTC backup battery 3.0V – 3.6V
J1	10	RESETINn		I	3.3V	Reset In (open drain) 10k pull-up on module
J1	11	CTSA*2	SD3_DATA2	O	3.3V	UART_A CTS
J1	12	SDHC_CD*2	GPIO1_IO06	I	3.3V	SDHC Card Detect
J1	13	TXDB*2	QSPI1B_SS0	I	3.3V	UART_B TXD
J1	14	RXDB*2	QSPI1B_SCLK	O	3.3V	UART_B RXD
J1	15	RTSB*2 TXDC*2	QSPI1B_DATA0	I	3.3V	UART_B RTS UART_C TXD
J1	16	CTSB*2 RXDC*2	QSPI1B_DATA1	O	3.3V	UART_B CTS or UART_C RXD
J1	17	TXDA*1	SD3_CMD	I	3.3V	UART_A TXD
J1	18	RXDA*1	SD3_DATA3	O	3.3V	UART_A RXD
J1	19	USB1_DP	USB_OTG2_DP	I/O		USB Host 1 +
J1	20	USB1_DM	USB_OTG2_DN	I/O		USB Host 1 -
J1	21	USB0_DP	USB_OTG1_DP	I/O		USB Device +
J1	22	USB0_DM	USB_OTG1_DN	I/O		USB Device -
J1	23	USB0_VBUS*9	USB_OTG1_VBUS	I	5.0V	USB Device Supply Voltage
J1	24	USB1_PWRON	GPIO1_IO12	O	3.3V	USB Host Power Enable
J1	25	GND				
J1	26	SPI_MISO*2	KEY_COL1	I/O	3.3V	SPI Master In Slave Out
J1	27	SPI_MOSI*2*8	KEY_ROW0	I/O	3.3V	SPI Master Out Slave In
J1	28	SPI_CLK*2	KEY_COL0	I/O	3.3V	SPI Clock
J1	29	SPI_CS*2*8	KEY_ROW1	I/O	3.3V	SPI Chip Select
J1	30	CAN0_TX|I2C1DAT*2*7	SD3_DATA5	I/O	3.3V	CAN0 TX or I2C1 Data
J1	31	CAN0_RX|I2C1CLK*2*7	SD3_DATA7	I/O	3.3V	CAN0 RX or I2C1 Clock
J1	32	I2DAT|CAN1_TX*2*7	SD3_DATA6	I/O	3.3V	CAN1 TX or I2C Data

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	33	I2CLK|CAN1_RX*2*7	SD3_DATA4	I/O	3.3V	CAN1 RX or I2C Clock
J1	34	SDHC_DAT0*2	SD2_DATA0	I/O	3.3V	SDHC Data0
J1	35	SDHC_DAT1*2	SD2_DATA1	I/O	3.3V	SDHC Data1
J1	36	SDHC_DAT2*2	SD2_DATA2	I/O	3.3V	SDHC Data2
J1	37	SDHC_DAT3*2	SD2_DATA3	I/O	3.3V	SDHC Data3
J1	38	SDHC_CLK*2	SD2_CLK	O	3.3V	SDHC Clock
J1	39	SDHC_CMD*2	SD2_CMD	O	3.3V	SDHC Command
J1	40	EINT2*2	GPIO1_IO11	I/O	3.3V	
J1	41	ETH1LED*5 PWM1*2	- GPIO1_IO13	O I/O	3.3V 3.3V	ETH1 Link Led PWM Output (if no ETH1)
J1	42	GND		PWR		GND
J1	43	LCD_R3*3	LCD1_DATA13	O	3.3V	
J1	44	LCD_R4*3	LCD1_DATA14	O	3.3V	
J1	45	LCD_R5*3	LCD1_DATA15	O	3.3V	
J1	46	LCD_R6*3	LCD1_DATA16	O	3.3V	
J1	47	LCD_R7*3	LCD1_DATA17	O	3.3V	
J1	48	LCD_G2*3	LCD1_DATA06	O	3.3V	
J1	49	LCD_G3*3	LCD1_DATA07	O	3.3V	
J1	50	LCD_G4*3	LCD1_DATA08	O	3.3V	
J1	51	LCD_G5*3	LCD1_DATA09	O	3.3V	
J1	52	LCD_G6*3	LCD1_DATA10	O	3.3V	
J1	53	LCD_G7*3	LCD1_DATA11	O	3.3V	
J1	54	LCD_B3*3	LCD1_DATA01	O	3.3V	
J1	55	LCD_B4*3	LCD1_DATA02	O	3.3V	
J1	56	LCD_B5*3	LCD1_DATA03	O	3.3V	
J1	57	LCD_B6*3	LCD1_DATA04	O	3.3V	
J1	58	LCD_B7*3	LCD1_DATA05	O	3.3V	
J1	59	LCD_CLK*3	LCD1_CLK	O	3.3V	
J1	60	LCD_DE*3	LCD1_ENABLE	O	3.3V	
J1	61	GND		PWR		GND
J1	62	GND		PWR		GND
J1	63	LCD_HSYNC*3 LCD_B2*3	LCD1_HSYNC LCD1_DATA0	O O	3.3V 3.3V	Can be switched via SW Default: LCD_HSYNC
J1	64	LCD_VSYNC*3 LCD_R2*3	LCD1_VSYNC LCD1_DATA12	O O	3.3V 3.3V	Can be switched via SW Default: LCD_VSYNC
J1	65	BL_CTRL*2	LCD1_DATA21	O	3.3V	Backlight PWM
J1	66	VLCD_ONn*2	LCD1_RESET	O	3.3V	Display On(active low)
J1	67	VBL_ONn*2	LCD_DATA23	O	3.3V	Backlight On (active low)

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	68	LCD_DEN*[2]	LCD_DATA22	O	3.3V	
J1	69	RTSA*[2]	SD3_CLK	I	3.3V	UART_A RTS
J1	70	ETH0LED	-	O	3.3V	ETH0 Link Led
J1	71	TOUCH_X+	-	I/O	3.3V	Touch Interface X+
J1	72	GND		PWR	GND	
J1	73	GND		PWR	GND	
J1	74	TOUCH_X-	-	I/O	3.3V	Touch Interface X-
J1	75	TOUCH_Y+	-	I/O	3.3V	Touch Interface Y+
J1	76	TOUCH_Y-	-	I/O	3.3V	Touch Interface Y-
J1	77	LINEOUTL | ETH1TX-*[5]	- -	O O	3.3V 3.3V	LineOut Left or Eth1 TX-
J1	78	LINEOUTR| ETH1RX-*[5]	- -	I O	3.3V 3.3V	LineOut Right or Eth1 RX-
J1	79	LINEINL | ETH1TX+*[5]	- -	O I	3.3V 3.3V	LineIn Left or Eth1 TX+
J1	80	LINEINR | ETH1RX+*[5]	- -	I I	3.3V 3.3V	LineIn Right or Eth1 RX+

Table 1: Interface connector pinout

*[1]: These IO-Pins are active signals during boot. Don't drive during boot process.

*[2]: These IO-Pins can be reconfigured as GPIO.

*[3]: If display is not used all these IO-Pins can be reconfigure as GPIO together

*[5]: Mounting option for 2nd LAN instead Audio

*[6]: Mounted on HW. Some additional PU/PD can be switched on by software. Please refer SW manual or ask our support team.

*[7]: Alternate pin configuration function in software. Please refer the software manual or ask our technical support. I2C0 can only used on one pair of pins at the same time (identical hardware block), I2C1 also. There is no compatibility to other picoCOM using this alternative function.

*[8]: From HW version 1.2 on.IO9 and IO11 are exchanged on HW Rev 1.1 please refer chapter 4.6

*[9]: Connect directly to VCC pin of USB device connector without serial resistor!

All digital signals does have 3.3V logic compliant level.

See starterkit documentation for connection examples.

4 Interfaces

4.1 Display Interface

All signals are working with 3.3V logic level. For all LCD signals we strictly recommend serial resistors or filter nearby the module connector to reduce EMI.

PicoCOM™A9X RGB Interface					
J1	Signal	18-bit (without HSYNC/VSYNC)[1]	18-bit (with HSYNC/VSYNC)[2]	16-bit	15-bit
43	LCD0	R1	R1	R0(LSB)	R0(LSB)
44	LCD1	R2	R2	R1	R1
45	LCD2	R3	R3	R2	R2
46	LCD3	R4	R4	R3	R3
47	LCD4	R5(MSB)	R5(MSB), R0(LSB)	R4(MSB)	R4(MSB)
48	LCD5	G0(LSB)	G0(LSB)	G0(LSB)	---
49	LCD6	G1	G1	G1	G0(LSB)
50	LCD7	G2	G2	G2	G1
51	LCD8	G3	G3	G3	G2
52	LCD9	G4	G4	G4	G3
53	LCD10	G5(MSB)	G5(MSB)	G5(MSB)	G4(MSB)
54	LCD11	B1	B1	B0(LSB)	B0(LSB)
55	LCD12	B2	B2	B1	B1
56	LCD13	B3	B3	B2	B2
57	LCD14	B4	B4	B3	B3
58	LCD15	B5(MSB)	B5(MSB), B0(LSB)	B4(MSB)	B4(MSB)
59	LCDCLK	DCLK			
63	LCD16	B0(LSB)	HSYNC	HSYNC	HSYNC
64	LCD17	R0(LSB)	VSYNC	VSYNC	VSYNC
60	LCDDEN	DE	DE	DE	DE
68	LCDENA	---	---	---	---
65	LCDCC	PWM Backlight			
66	LCDPOWn	LCD Power On (active low)			
67	CFLPOWn	Backlight Power On (active low)			

Table 2: RGB Interface Connection Table

[1] This mode PicoCOM™A9X outputs 18 data bits. Please also configure your display driver in the same way. HSYNC/VSYNC mode is not possible in this configuration. You must enable DE mode.
[2] This mode PicoCOM™A9X outputs 16 data bits. Please also configure your display driver in the same way.

Note: Most displays support **HSYNC/VSYNC** or **DE mode**. Please be sure just connect only useful signals at same time. The 18bit w/o HSYNC/VSYNC mode needs a special configuration made by software. Please refer the SW manual for this configuration.

4.2 USB Host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports EMV protection is required nearby the USB connector.

With the USB_PWR signal you could switch on the USB power on your current limiting IC.

The usb.org webpage provides "High Speed USB Platform Design Guidelines" with highly recommended informations for a proper working USB design.
ESD and EMV protection is required on baseboard.

If the USB port is not used please leave open.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
USB Host						
J1	19	USB1_DP	USB_OTG2_DP	I/O		USB Host 1 +
J1	20	USB1_DM	USB_OTG2_DN	I/O		USB Host 1 -
J1	24	USB1_PWRON	GPIO1_IO12	O	3.3V	USB Host Power Enable

Table 3: USB Host Pinout

4.3 USB Device

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

The USB0_VBUS signal does detect a connected host by detecting the voltage. This signal is 5V tolerant and needs a level above 3.7V. Do not use a voltage divider or serial resistor.

If the USB device port is not used please leave open.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
USB Device						
J1	21	USB0_DP	USB_OTG1_DP	I/O		USB Device +
J1	22	USB0_DM	USB_OTG1_DN	I/O		USB Device -
J1	23	USB0_VBUS	USB_OTG1_VBUS	I	5.0V	USB Device Supply Voltage

Table 4: USB Device Pinout

4.4 SD Card Interface

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org. Pullups are integrated on the module. Card detection signal and write protection signal are not supported by the PicoCOM™ standard. Unused signals should be left unconnected. Signals can be optional used as GPIO.

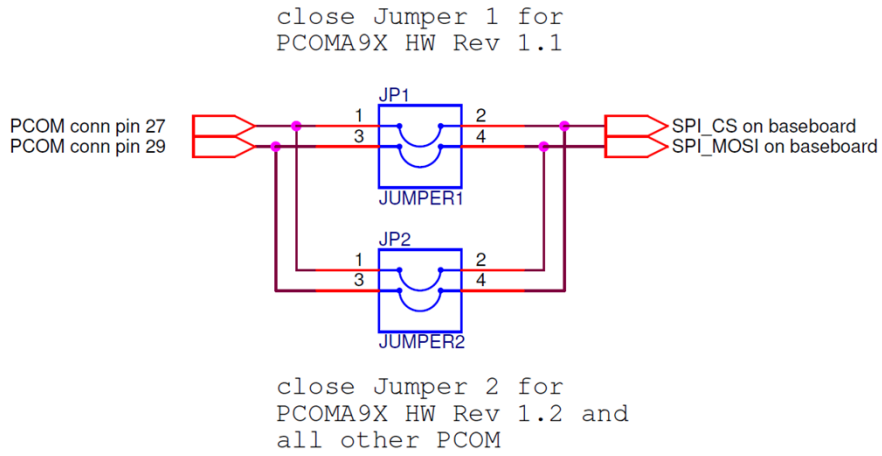
	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
SD Card Interface						
J1	12	SDHC_CD	GPIO1_IO06	I	3.3V	
J1	34	SDHC_DAT0	SD2_DATA0	I/O	3.3V	100k pull-up
J1	35	SDHC_DAT1	SD2_DATA1	I/O	3.3V	
J1	36	SDHC_DAT2	SD2_DATA2	I/O	3.3V	
J1	37	SDHC_DAT3	SD2_DATA3	I/O	3.3V	
J1	38	SDHC_CLK	SD2_CLK	O	3.3V	
J1	39	SDHC_CMD	SD2_CMD	O	3.3V	100k pull-up

Table 5: SD Card Interface Pinout

4.5 Serial Peripheral Interface (SPI)

The module supports one HS SPI (Serial Peripheral Interface) with one chip select. Signals are 3.3V compliant.

At HW Rev. 1.1 is a failure (is fixed on HW Rev 1.2). SPI is not backward compatible to other modules in PicoCOM formfactor. The signals SPI_CS on pin 29 and SPI_MOSI on pin 27 are interchanged. For full support on customers system it needs jumper:



Both pins are configurable as GPIO. In this case this interchange can be handled in SW.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
SPI Interface						
J1	26	SPI_MISO	KEY_COL1	I/O	3.3V	SPI Master In Slave Out
J1	27	SPI_MOSI	KEY_ROW0	I/O	3.3V	SPI Master Out Slave In
J1	28	SPI_CLK	KEY_COL0	I/O	3.3V	SPI Clock
J1	29	SPI_CS	KEY_ROW1	I/O	3.3V	SPI Chip Select

Table 6: SPI Interface Pinout

4.6 I2C Interface

The module supports a maximum of three I2C interfaces. One is compatible with PicoCOM standard.

Signals are 3.3V compliant and don't have pullups on module. So please add 2.2 kOhm pullups to 3.3V on baseboard. 5V devices on baseboard need a level shifter.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
I2C Interface						
J1	30	I2C0_SDA	SD3_DATA5	I/O	3.3V	Optional: CAN0_TX
J1	31	I2C0_SCL	SD3_DATA7	O	3.3V	Optional: CAN0_RX
J1	32	I2C1_SDA	SD3_DATA1	I/O	3.3V	Optional: CAN1_TX
J1	33	I2C1_SCL	SD3_DATA0	O	3.3V	Optional: CAN1_RX

Table 7: I2C Interface Pinout

4.7 Serial Interface (UART)

The module provides a maximum of three different serial ports with 3.3V TTL signals. These signals are not 5V compliant. Please use a transceiver with 3.3V power supply.

If you don't need the serial port this pins can be used optional as GPIOs.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
UART Interface						
J1	11	CTSA	SD3_DATA2	O	3.3V	Default: GPIO
J1	69	RTSA	SD3_CLK	I	3.3V	Default: GPIO
J1	13	TXDB	QSPI1B_SS0	O	3.3V	
J1	14	RXDB	QSPI1B_SCLK	I	3.3V	
J1	15	TXDC RTSB	KEY_COL3 QSPI1B_DATA1	O	3.3V	Optional: RTSB
J1	16	RXDC CTSB	KEY_ROW3 QSPI1B_DATA0	I	3.3V	Optional: CTSB
J1	17	TXDA	SD3_CMD	O	3.3V	
J1	18	RXDA	SD3_DATA3	I	3.3V	

Table 8: UART Interface Pinout

4.8 CAN Interface

PicoCOM™A9X provides up-to two CAN interfaces. One is compatible with the PicoCOM standard. The second shares pins with the I2C interface. The Vybrid SoC is used for the CAN function.

CAN bus transmits and receive 3.3V TTL signal without any termination.

Needs a 3.3V transceiver like SN65HVD230 to the CAN bus.

Signals can be optional used as GPIO or I2C.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
CAN Interface						
J1	30	CAN0_TX	SD3_DATA5	O	3.3V	Optional: I2C0_SDA
J1	31	CAN0_RX	SD3_DATA7	I	3.3V	Optional: I2C0_SCL
J1	32	CAN1_TX	SD3_DATA6	O	3.3V	Optional: I2C1_SDA
J1	33	CAN1_RX	SD3_DATA4	I	3.3V	Optional: I2C1_SCL

Table 9: CAN Interface Pinout

4.9 Ethernet Connection

On PicoCOM™A9X board there are 1 standard and 1 optional Ethernet connections. Ethernet TX+/- and RX+/- lines are 100 ±20% Ohm differential pairs to a 1:1/1:1 transformer. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm). The transformer midpoint should be connected to the 3.3V power supply. LED signal is able to drive a 3.3V powered LED with 5mA directly to GND. If Ethernet is not used please leave signals unconnected.

The Ethernet PHYs on module: DP83848J

	Pin	Signal	Alternative	I/O	Voltage	Remarks
Ethernet Interface						
J1	1	ETH0_TX-		O	3.3V	Ethernet0 Transmit-
J1	2	ETH0_RX-		I	3.3V	Ethernet0 Receive-
J1	3	ETH0_TX+		O	3.3V	Ethernet0 Transmit+
J1	4	ETH0_RX+		I	3.3V	Ethernet0 Receive+
J1	77	ETH1_TX-	LINEOUT_L	O	3.3V	Ethernet1 Transmit-
J1	78	ETH1_RX-	LINEOUT_R	I	3.3V	Ethernet1 Receive-
J1	79	ETH1_TX+	LINEIN_L	O	3.3V	Ethernet1 Transmit+
J1	80	ETH1_RX+	LINEIN_R	I	3.3V	Ethernet1 Receive+

Table 10: Ethernet Interface

4.10 Audio Interface

PicoCOM™A9X board provides stereo analog input and output lines. SGTL5000 is used as audio codec. The module also supports digital audio input and output over I2S protocol. For mounting option with I2S codec on baseboard please ask our technical support. To avoid ESD and EMV problems, it is necessary to have a protection on the baseboard.

	Pin	Signal	Alternative	I/O	Voltage	Remarks
Audio Interface						
J1	77	LINEOUT_L	ETH1_TX-	O	3.3V	Analog Stereo Line Out Left
J1	78	LINEOUT_R	ETH1_RX-	O	3.3V	Analog Stereo Line Out Right
J1	79	LINEIN_L	ETH1_TX+	I	3.3V	Analog Stereo Line In Left
J1	80	LINEIN_R	ETH1_RX+	I	3.3V	Analog Stereo Line In Right

Table 11: Audio Interface

4.11 Touch Interface

The integrated resistive touch controller will support 4 wire analog resistive touch panels without any additional circuit.

Pin		Signal	Alternative	I/O	Voltage	Remarks
Touch Interface						
J1	71	TOUCH_X+		I	3.3V	4-wire Touchscreen : X+ Electrode
J1	74	TOUCH_X-		I	3.3V	4-wire Touchscreen : X- Electrode
J1	75	TOUCH_Y+		I	3.3V	4-wire Touchscreen : Y+ Electrode
J1	76	TOUCH_Y-		I	3.3V	4-wire Touchscreen : Y- Electrode

Table 12: Touch Control Interface

4.12 JTAG

Pin		Signal	CPU Pad	I/O	Voltage	Remarks
JTAG Connector						
J2	1	+V3.3S		PWR	3.3V	
J2	2	JTAG_TMS	JTAG_TMS	O	3.3V	JTAG Test Mode Select
J2	3	GND		PWR	GND	
J2	4	JTAG_TCK	JTAG_TCK	O	3.3V	JTAG Test Clock
J2	5	GND		PWR	GND	
J2	6	JTAG_TDO	JTAG_TDO	O	3.3V	JTAG Test Data Out
J2	7	JTAG_nTRST	JTAG_TRST	I	3.3V	JTAG Test Reset
J2	8	JTAG_TDI	JTAG_TDI	I	3.3V	JTAG Test Data In
J2	9	GND		PWR	GND	
J2	10	JTAG_nSRST	POR	I	3.3V	JTAG System Reset

Table 13: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.13 Power Signals

J1 Pin	Signal Name	I/O	Voltage	Description
5, 6	+V3.3S	PWR In	3.3V	Main Power Supply Input Please refer Electrical characteristic (Ch7)
9	VBAT	PWR In	3V	RTC Battery Input, leave open if not used Please refer Electrical characteristic (Ch7)
23	USB_OTG_VBUS	I	5V	USB Supply Voltage
10	RESETINn	I	3.3V	Power On Reset Input, 10K Pull-Up
	GND	PWR	GND	Connect all GND pins to a GND plane

Table 14: Power and Power Control

By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

RESETINN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On power fail VDD_VIN has to be switched off and on to avoid latch up effects.

The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

5 Flash

5.1 NAND Flash

By default, boot mode of PicoCOM™A9X is configured for NAND boot.

PicoCOMA™9X implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S to be robust against power failures

5.1.1 NAND Flash Data Retention

The NAND Flash is based on “single level cell” (SLC) technology. This technology is ten times more robust compared to “multi-level cell” (MLC) technology. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 Real Time Clock (RTC)

There is a NXP PCA8565 or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift over the day.

7 Electrical characteristic

7.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V

Table 15: Absolute Maximum Ratings

7.2 DC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIN	Input supply voltage	3.135	3.3	3.465	V
I_{IN}	Input Current			1.0	A
VBAT	RTC Power Supply	2.2	3.0	3.45	V
P_{VBAT}	Power Consumption		0.22	0.6*	µA
USB_OTG_VBUS	USB supply voltage	4.4	5.5		V
I_{VBUS}	USB supply current		100		mA
VDD_SNVS_IN	SNVS supply	2.4	3.6		V
V_{ih}	High Level Input Voltage	0.7*OVDD	OVDD		V
V_{il}	Low Level Input Voltage	0	0.3*OVDD		V
I_o	Output current IOs		5.0		mA

Table 16: DC Electrical Characteristics

8 Thermal Specification

Description	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Industrial Range Environmental Temperature (I)	-40		+85	°C

Table 17: Thermal Specs

Note 1: Maximum junction temperature of the CPU is 105°C. In this case cooling is a necessity and highly recommended. See also: Power Consumption and Power Consumption and Cooling

9 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

10 ESD and EMC Implementing

Because there is no connector to „out of case“there is no ESD protection for any interface. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A good guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the PicoCOMA™9X supports Spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

11 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

12 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d.** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d.** and **t.b.d.** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

13 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

14 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

15 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

16 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 5: Matrix Code Sticker

17 Appendix

Important Notice

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