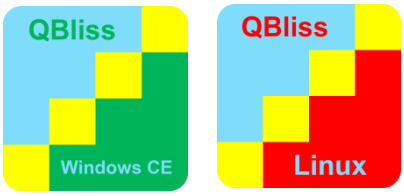
Hardware Documentation

QBlissA9R2

Version 1
(2018-09-19)



Preliminary

This document is subject to change without notice

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About This Document

This document describes how to use the QBlissA8 board with mechanical and electrical information. The latest version of this document can be found at http://www.fs-net.de.

History

Date	V	A,M,R	Chapter	Description	Au
30.05.2017	1			First release	KW
19.09.2018	1	A	2	Extend thermal specification	JG

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Content

1 Introduction

This document does describe the mechanical and electrical information for the QBlissA9R2 embedded module with Freescale i.MX6 ARM Cortex™-A9 based CPU. Please also refer the design guide by using this module for your application.

2 Dimensions

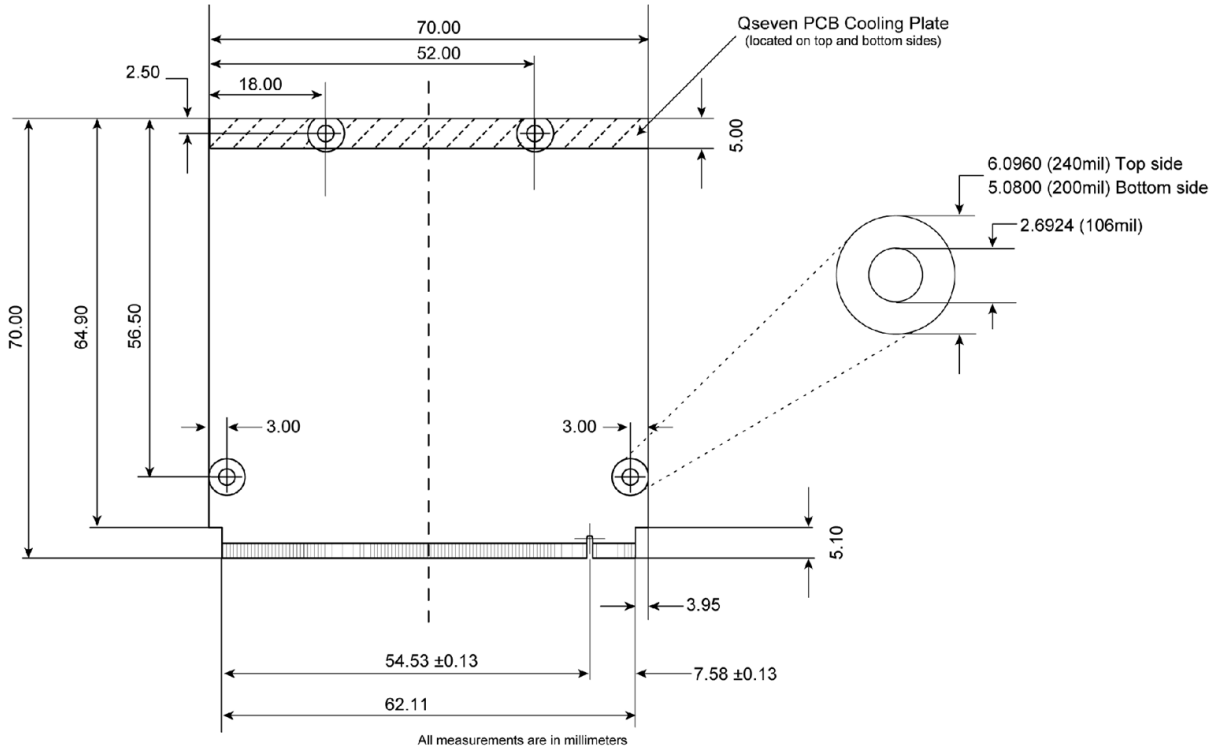


Figure 1: mechanical dimensions

PCB thickness:	1.2 ±0.1 mm
Height of parts on top side:	2.5 mm
Height of parts on bottom side: (without connectors)	1.5 mm
Weight:	25g

2.1 Thermal Specification

	Min	Typ	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MX6	-20		+105	°C
Junction temperature i.MX6 (“I”) [2]	-20		+105	°C
Junction to Top of i.MX6 (Psi-JT)[3]		2		°C/W

[1] Depending on cooling solution. See also: Power Consumption and cooling

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3 Technical Data Qseven IF connector

The QBliss module is equipped with a goldfinger connector.

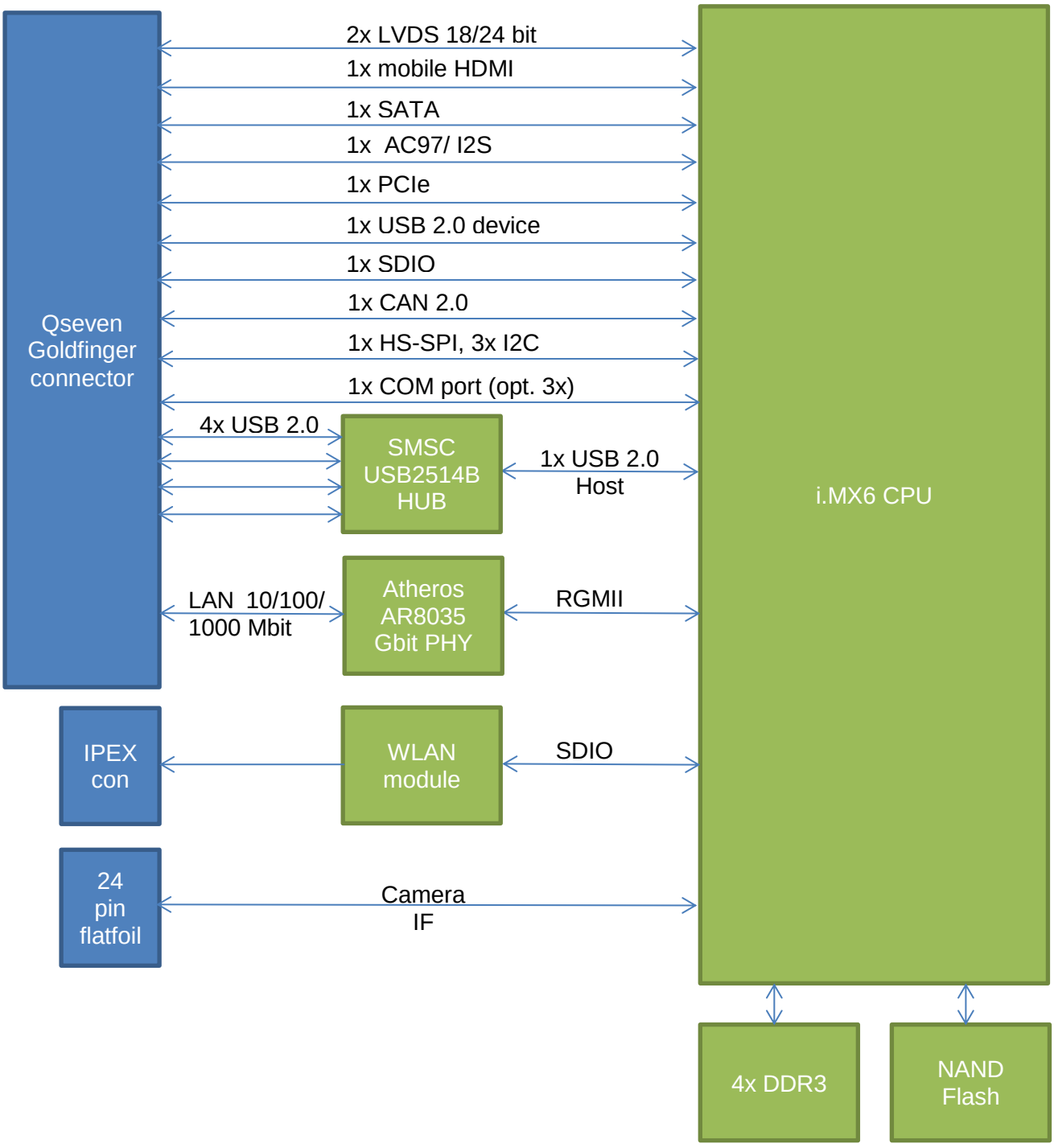
Matching connectors are:

Foxconn	AS0B326-S78N-7F
Speedtech	B33P102-XX1X
Speedtech	B33P102-XX2X
Lotes	SP-AAA-MXM-001
YAMAICHI	BEC-0.5-230-S9-BFR-EDC
YAMAICHI	BEC-0.5-230-S9-BFR-EDC

Further information are also available from http://www.qseven-standard.org

Power supply:	5V DC ±5%
Interfaces:	1x Ethernet 10/100/1000Mbit 4x USB 2.0 Host 1x USB 2.0 Device 2x I2C 1x SPI 1x CAN 2.0 1x SD card 1x AC97 digital audio 1x SATA 2x serial port (optional)
LCD-interfaces:	2x 18/24bit LVDS 1x mobile HDMI
Memory:	4 GByte DDR3 DRAM 16 GByte NAND Flash
CPU:	i.MX6 CPU up to 1GHz
Operating temperature:	0°C...+70°C/ -40..+85°C

4 Block Diagram



5 Pin Assignment

Use list from QBlissA9R2_IO-Pins.xls

GND	1	2	GND
GBE_MDI3-	3	4	GBE_MDI2-
GBE_MDI3+	5	6	GBE_MDI2+
GBE_LINK100#	7	8	GBE_LINK1000#
GBE_MDI1-	9	10	GBE_MDI0-
GBE_MDI1+	11	12	GBE_MDI0+
GBE_LINK#	13	14	GBE_ACT#
GBE_CTREF (open)	15	16	PMIC ON (SUS_S5#)
GPI (WAKE#)	17	18	PMIC STBY (SUS_S3#)
GPO (SUS_STAT#)	19	20	PWRBTN#
SLP_BTN#	21	22	LID_BTN#
GND	23	24	GND
KEY			KEY
GND	25	26	PWGIN
GPI (BATLOW#)	27	28	RSTBTN#
SATA0_TX+	29	30	n.u.
SATA0_TX-	31	32	n.u.
GPO (SATA_ACT#)	33	34	GND
SATA0_RX+	35	36	n.u.
SATA0_RX-	37	38	n.u.
GND	39	40	GND
BIOS_DIS#/BOOT_ALT#	41	42	SDIO_CLK#
SDIO_CD#	43	44	SDIO_LED
SDIO_CMD	45	46	SDIO_WP
SDIO_PWR#	47	48	SDIO_DAT1
SDIO_DAT0	49	50	SDIO_DAT3
SDIO_DAT2	51	52	SDIO_DAT5 (N/A)
SDIO_DAT4 (N/A)	53	54	SDIO_DAT7 (N/A)
SDIO_DAT6 (N/A)	55	56	RSVD
GND	57	58	GND
AC97_SYNC)*2	59	60	SMB_CLK
AC97_RST#)*2	61	62	SMB_DAT
AC97_BITCLK)*2	63	64	SMB_ALERT#
AC97_SDI)*2	65	66	I2C_CLK
AC97_SDO)*2	67	68	I2C_DAT
GPI (THRM#)	69	70	GPO (WDTRIG#)
n.u.	71	72	GPI (WDOUT)
GND	73	74	GND

Table 1: Pin Assignment part 1

n.u.	75	76	n.u.
n.u.	77	78	n.u.
n.u.	79	80	n.u.
n.u.	81	82	USB_P4-
n.u.	83	84	USB_P4+
USB_2_3_OC#	85	86	USB_0_1_OC#
USB_P3-	87	88	USB_P2-
USB_P3+	89	90	USB_P2+
USB_HOST_PRES#	91	92	USB_HC_SEL
USB_P1- (client port)	93	94	USB_P0-
USB_P1+ (client port)	95	96	USB_P0+
GND	97	98	GND
LVDS_A0+	99	100	LVDS_B0+
LVDS_A0-	101	102	LVDS_B0-
LVDS_A1+	103	104	LVDS_B1+
LVDS_A1-	105	106	LVDS_B1-
LVDS_A2+	107	108	LVDS_B2+
LVDS_A2-	109	110	LVDS_B2-
LVDS_PPEN	111	112	LVDS_BLEN
LVDS_A3+	113	114	LVDS_B3+
LVDS_A3-	115	116	LVDS_B3-
GND	117	118	GND
LVDS_A_CLK+	119	120	LVDS_B_CLK+
LVDS_A_CLK-	121	122	LVDS_B_CLK-
LVDS_BLT_CTRL	123	124	RSVD
LVDS_DID_DAT	125	126	LVDS_BLC_DAT
LVDS_DID_CLK	127	128	LVDS_BLC_CLK
CAN0_TX	129	130	CAN0_RX
TMDS_CLK+	131	132	NC
TMDS_CLK-	133	134	NC
GND	135	136	GND
TMDS_LANE1+	137	138	NC
TMDS_LANE1-	139	140	NC
GND	141	142	GND
TMDS_LANE0+	143	144	NC
TMDS_LANE0-	145	146	NC
GND	147	148	GND
TMDS_LANE2+	149	150	HDMI_CTRL_DAT
TMDS_LANE2-	151	152	HDMI_CTRL_CLK
HDMI_HPD#	153	154	NC
PCIE_CLK_REF+	155	156	(N/A)
PCIE_CLK_REF-	157	158	RSTOUT#
GND	159	160	GND

Table 2: Pin Assignment part 2

n.u. (RX1))*4	161	162	n.u. (CTS1))*4
n.u. (TX1))*4	163	164	n.u. (RTS1))*4
GND	165	166	GND
(N/A)	167	168	(N/A)
(N/A)	169	170	(N/A)
TX1	171	172	RTS1
(N/A)	173	174	(N/A)
(N/A)	175	176	(N/A)
RX1	177	178	CTS1
PCIE0_TX+	179	180	PCIE0_RX+
PCIE0_TX-	181	182	PCIE0_RX-
GND	183	184	GND
n.u. (RX0))*3	185	186	n.u. (TX0))*3
n.u. (CTS0))*3	187	188	n.u. (RTS0))*3
(N/A)	189	190	(N/A)
(N/A)	191	192	(N/A)
VCC_RTC	193	194	GPO (SPKR)
GPI (FAN_TACHOIN)	195	196	GPO (FAN_PWMOUT)
GND	197	198	GND
SPI_MOSI	199	200	SPI_CS0
SPI_MISO	201	202	SPI_CS1
SPI_SCK	203	204	MFG_NC4
VCC_5V_SB	205	206	VCC_5V_SB
MFG_NC0	207	208	RX3/MFG_NC2
TX3/ MFG_NC1	209	210	MFG_NC3
VCC	211	212	VCC
VCC	213	214	VCC
VCC	215	216	VCC
VCC	217	218	VCC
VCC	219	220	VCC
VCC	221	222	VCC
VCC	223	224	VCC
VCC	225	226	VCC
VCC	227	228	VCC
VCC	229	230	VCC

Table 3: Pin Assignment part 3

comments:
)*2 AC97 instead HDA channel, HDA codec will not work on this pins, but will not be destroyed. Combi Layout possible
)*3 not spec conform version with COM ports possible on this pins
)*4 not spec conform version with COM ports possible on this pins; same signals as on Spec 2.0 conform pins 171,172,177,178. Mount option for backward compatibility

) Interface and signal description

5.1 USB host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports EMV protection is required nearby the USB connector.
Low level on the overcurrent detection signal USB_*_OC# signal will popup a message on some OS. This signal is not a part of USB specification and should be unconnected, if this popup messages is not needed. Just a single OC# signal is used for 2 USB ports together.
The usb.org webpage provides "High Speed USB Platform Design Guidelines" with highly recommended informations for a proper working USB design.
If a USB port is not used please leave open.

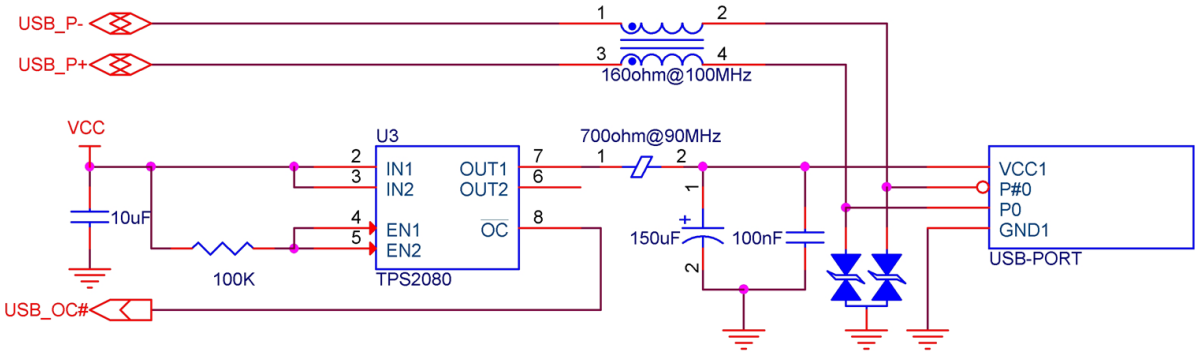


Figure 2: USB Host connection

5.2 USB device

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.
The USB_CC signal does detect a connected host by detecting the voltage. This signal does have a pullup on the CPU module, don't drive a active high level on this pin.
If the USB client port is not used please leave open.

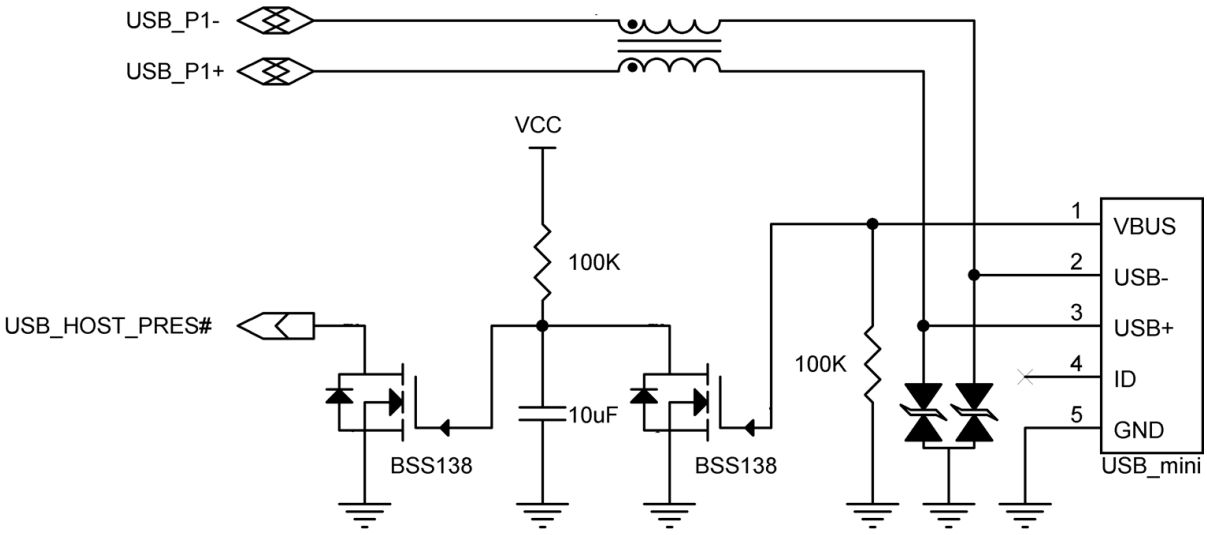


Figure 3: USB device connection

5.3 LVDS port

The single channel LVDS display port can be direct connected with 95 ohm ±20% differential lines to a LVDS 18/24 bit display. We recommend EMV differential protection on each differential pair to reduce electromagnetic interferences.
Each LVDS signal (data, strobes, and clocks) should be length-matched to within ±20 mils of any other LVDS signal.
The maximum signal and cable length is 7 inch in summary
(1 inch = 25.4 mm; 1mil = 25.4 µm).
The "High Speed USB Platform Design Guidelines" from usb.org webpage will help you with rules and hints on differential pairs.
LVDS_BLC_CLK and LVDS_BLC_DAT are for a external software controlled D/A converter to provide a dimming voltage. This needs additional software.
LVDS_PPEN is a 3.3V TTL high active signal to switch on the LCD power
LVDS_BLEN is a 3.3V TTL high active signal to switch on the backlight power
LVDS_BLT_CTRL can provide you a 3.3V TTL PWM output for dimming the CFL converter
Unused signals should be left unconnected.

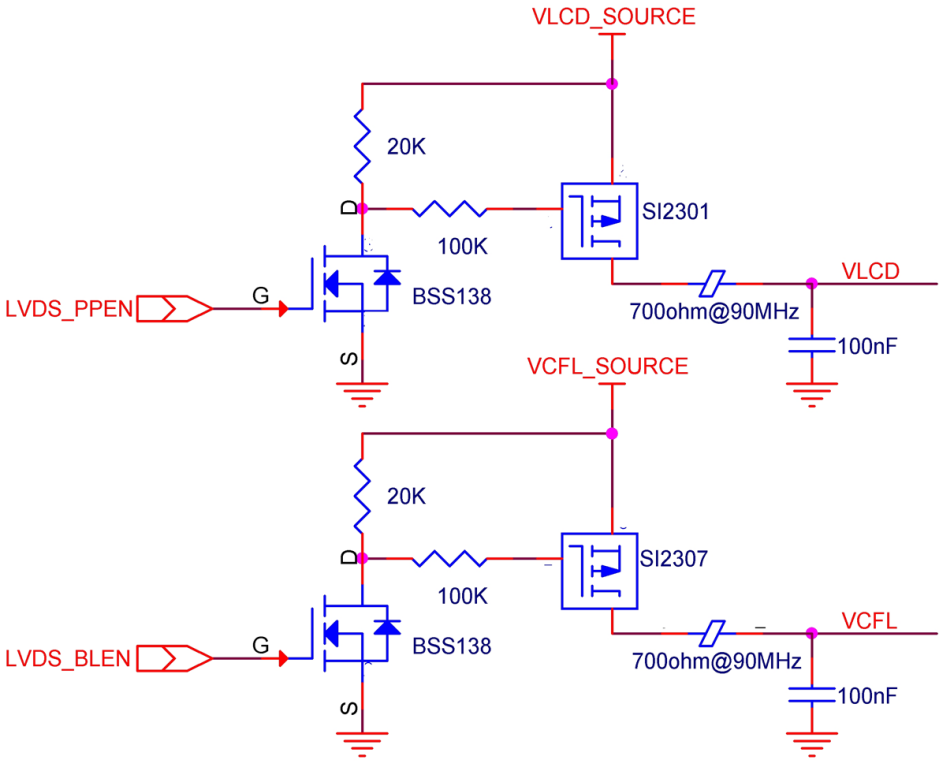


Figure 4: LCD power and CFL power circuit

5.4 CAN Bus

The chip does provide the CAN bus transmit and receive TTL signal without any termination. Needs a interface chip to the CAN bus. If not used, please left signals unconnected.

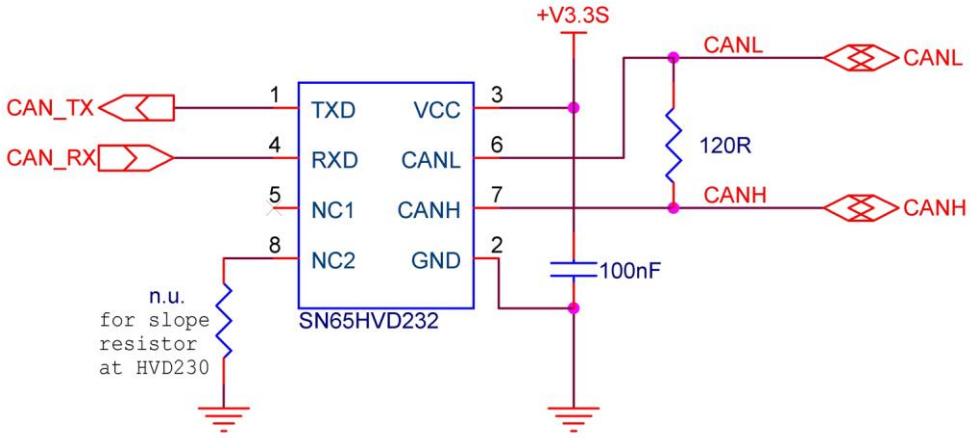


Figure 5: CAN transceiver circuit

5.5 HDMI & DVI

The QBlissA8 module allows to connect HDMI or single channel DVI monitor without any transmitter chip. Audio transmitting is not supported. The signals should be routed with 100 ohm ±15% differential lines. The length difference between a differential pair should be limited to 5 mils maximum.Each pair should be length-matched to within ± 20 mils of any other signal pair.
If HDMI is not used, please leave unconnect.

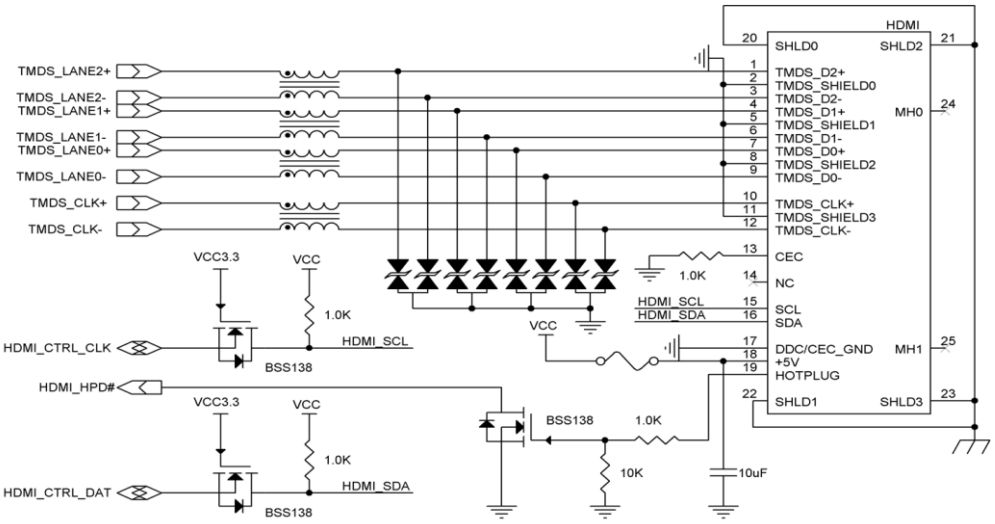


Figure 6: HDMI circuit

5.6 SD/MMC card

The interface is supporting a SD card channel. For specificiation and licensing please refer the website of the SD Association http://www.sdcard.org.
Unused signals should be left unconnected.

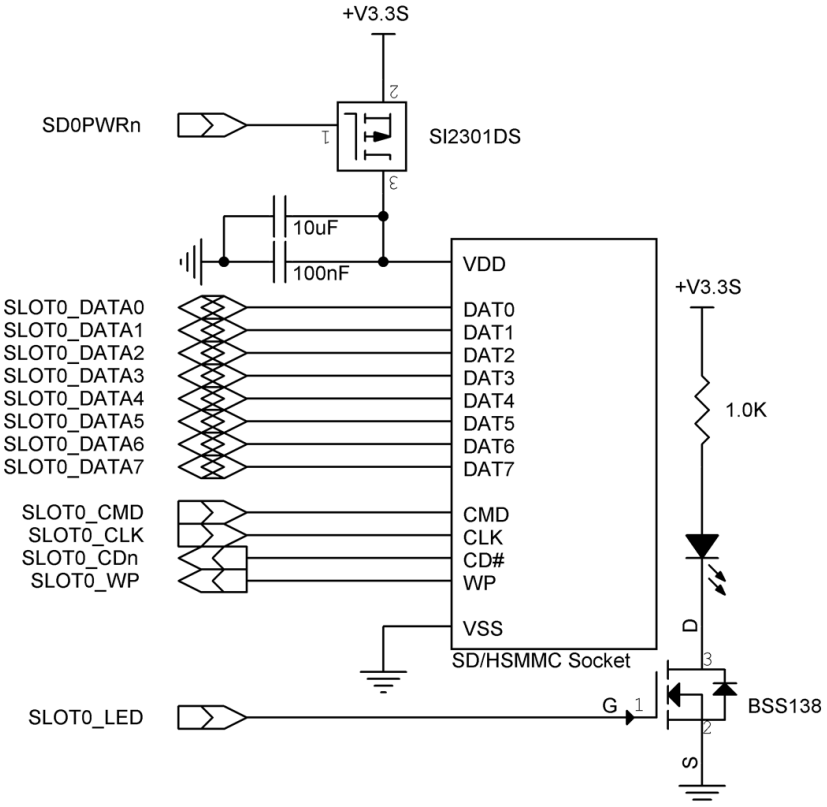


Figure 7: SD/ MMC circuit

5.7 SPI

The module supports a HS SPI (Serial Peripheral Interface) with 2 chip selects. Signals are 3.3V compliant and does have pullup on module. Devices on baseboard with other voltage need a level shifter.

5.8 I2C

The module supports a I2C interface as I2C master. Signals are 3.3V compliant and does have pullup on module. Devices on baseboard with other voltage need a level shifter.

5.9 AC97 sound

The QBlissA8 module supports a AC97 sound codec. A HDA codec connected on this interface will not be supported, but will not be destroyed.

5.10 PCIe

A single lane PCI Express port (Gen 2.0) is supported.
Please following design rules from PCI-SIG and the Qseven Designguide on you design.

5.11 Power

VCC_5V_SBY separate 5V standby power supply for standby and suspend supporting systems. If you don't use suspend and/or standby it must connected to VCC. **Don't leave unconnect !**

VCC 5V power supply input
For tolerances and power consumption please refer chapter 7..

5.12 COM ports (optional function)

Two COM ports are a optional mounting option and doesn't following the Qseven specification. COM0 is mounted all the time and will not have any influence with a LPC device on baseboard. LPC is not supported on any version of the module.
COM1 on pin 161..164 will be shipped only on customer request. With this option the module will not longer working in all Qseven baseboards. If mounted, the following signals are available on the goldfinger connector:

COM0 (not following Qseven spec)	RX	185
	TX	186
	CTS	187
	RTS	188
COM1 (conform to Spec 2.0)	RX	177 (161)*
	TX	171 (163)*
	CTS	178 (162)*
	RTS	172 (164)*
COM3	RX	208
	TX	209

(XXX)* for backward compatibility to older versions, mounting option

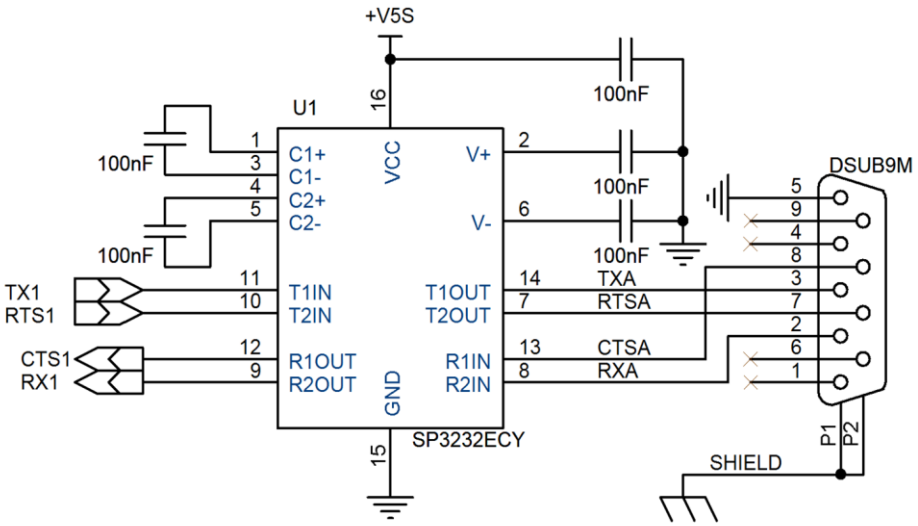


Figure 8: COM port connection

5.13 SATA

A single SATA device can be connected on the SATA interface. Because the stucture of several ARM-OS SATA is only to store data. The OS will be loaded from the onboard mounted Flash. Leave signals unconnect if not used.

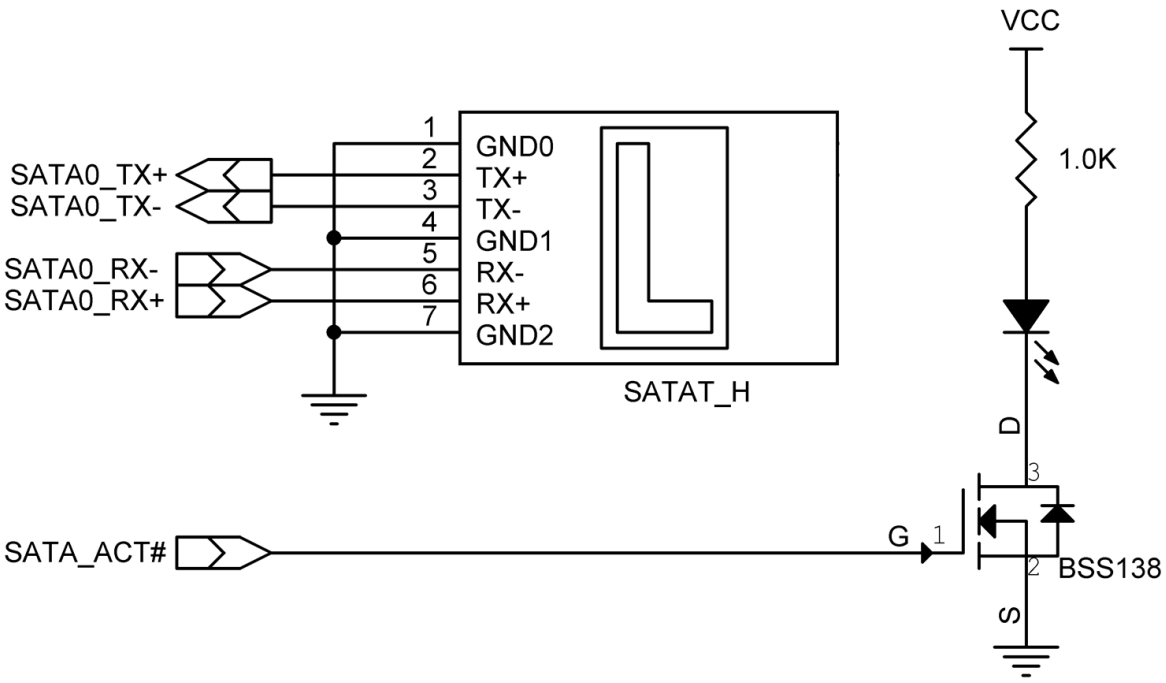


Figure 9: SATA circuit

6 Electrical Data

Power supply 5V	5V +/- 5%
Power supply 5VSBY	5V +/- 5%
Power supply BATT	2.5 … 3.3 V

power consumtion, all values in Ampere, CPU Quadcore, 1GHz, w/o WLAN option, with external LAN transformer consumption

typical current consumption BATT (from HW Rev 1.2 on):	1 uA
maximum current consumption BATT (from HW Rev 1.2 on):	1.3 uA
maximum power consumption 5V (summary all chips):	2.0 A

6.1 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.
The operating temperature can be measured on the mounting holes or the golden cooling plate on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C for the most of our QBlissA9 boards).

The maximum power consumption of the board could be 10 Watt. This value is with 100% working of 4 cores and full working 3D engines. Calculating with this scenario does need an expensive cooling.
Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. 4 and 7 Watt on different applications.
Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD you have to calculate a working cooling solution for the board. Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.
To calculate your cooling we recommend this helpful literature

- AN4579 from freescale.com
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

6.2 ESD and EMI requirements

Because there is no connector to „out of case“ there is no ESD protection for any interface. It needs ESD protection on every connector out oft the case on your baseboard.
To reduce EMI the QBlissA9 supports Spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend to have your baseboard with controlled impedance and wires as short as possible.
Please also refer the Qseven Design Guide for additional informations.

7 Storage conditions

Maximum storage on room temperature with non condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
Above we recommend vacuum dry packs.

8 Errata

HW Revision 1.1

- **Boot fail:** Intermittent, very low rate boot fail. Under some circumstances it might happen that the board is not booting properly. This is caused by an internal error in CPU ROM code.
  Workaround: none

HW Revision 1.2

- **Boot fail:** Intermittent, very low rate boot fail. Under some circumstances it might happen that the board is not booting properly. This is caused by an internal error in CPU ROM code on Linux UBoot.
  Workaround: none

HW Revision 1.3

- **Boot fail**: Fixed by external watchdog. On newer Freescale CPU Revisions this failure is fixed and Watchdog is not longer mounted.

9 Appendix

List of figures

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.
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