Hardware Documentation

PicoCore™MX6UL
for HW Revision 1.20

Version 007
(2022-11-09)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCore™MX6UL board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
18.07.2018	000	All		-	Initial Version	KW
14.12.2018	001	All		-	Inserted new B2B connector. Schematic examples are still preliminary.	HF
18.12.2018	002	All	A	2.1	Description SMT Steel Spacer added	HF
18.12.2018	002	All	M	2	Drawing “Mechanical Dimensions” extended	HF
18.12.2018	003	All	M	4.8	Added name of Phy	HF
25.06.2019	004	All	M	2, 4.10	Add designator J1 and J2. Correct 18-Bit column	TM
09.03.2020	005	All	M	3.1, 4.14, 6, 8	Change Name to PowerGood, Add Information about VDD_VBAT	MW
10.08.2021	006	All	M	3.1, 6	Change for Revision 1.20	MW
07.11.2022	007	All	M	3.1	Correct J1 Pin 1-4 & 29	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block diagram

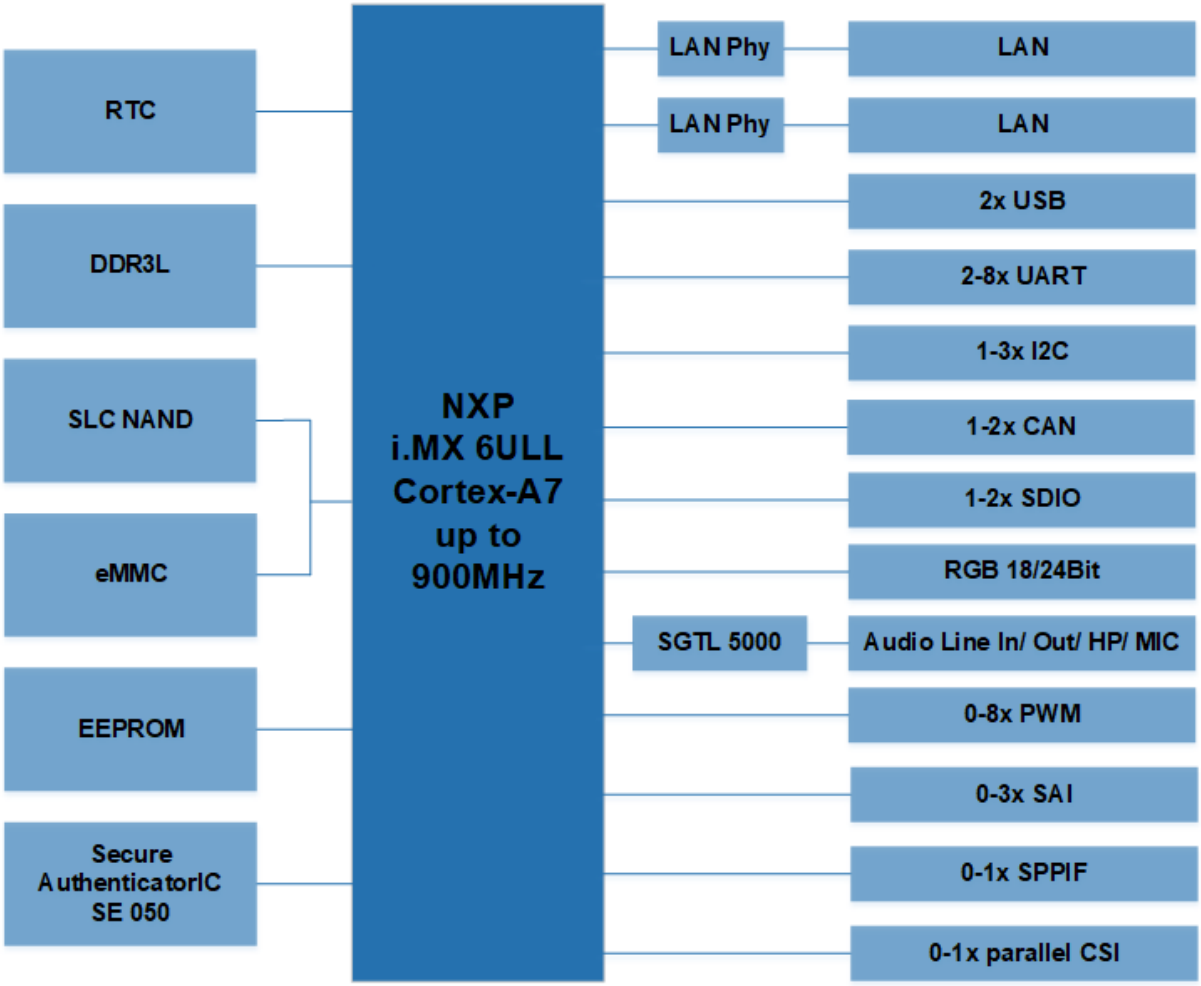

Figure 1: Block Diagram

2 Mechanical Dimension

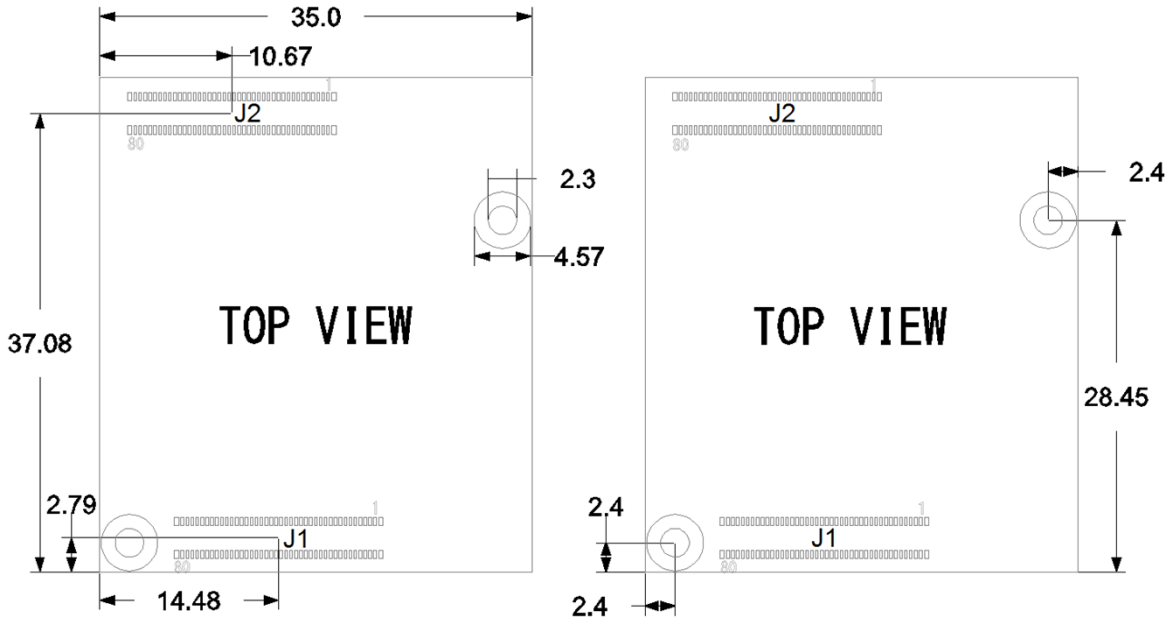

Figure 2: Mechanical Dimension

Size:	40mm x 35mm
PCB thickness:	1.2 ± 0.1mm
Height of the parts on the top side:	max.5 mm
Height of the parts on the bottom side:	max. 1.4 mm
Weight:	14g

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer from supplier “Würth Elektronik” order number “9774015243R”. You can also order via our web shop.

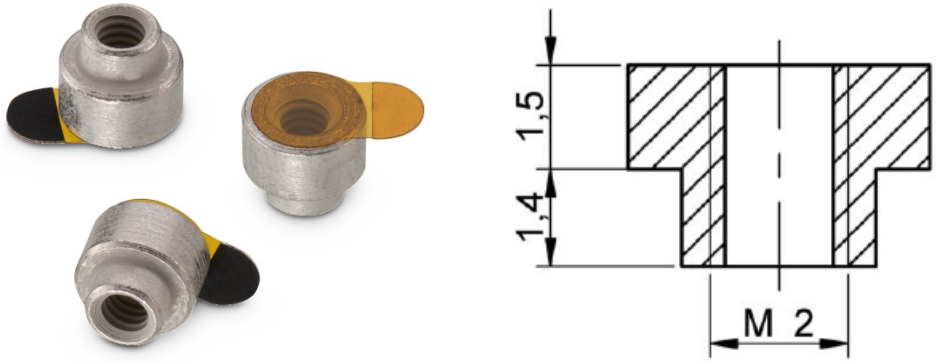

Figure 3: WE SMT Steel Spacer

Data sheet and 3D model (STP) is available on our web side.

3 Interface and signal description

3.1 B2B connectors

PicoCoreMX6UL is using two 80 pin connectors from manufacturer Hirose.
Part number: DF40C-80DP-0.4V
Part number counterpart: DF40C-80DS-0.4V
With this combination, you get minimal stacking height of 1,5mm. Other possible stacking heights by using different counterpart connector are: 2mm, 3mm, 3,5mm and 4mm.
The connector with 1,5mm stacking height is available at F&S and can be ordered via our web shop.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	1	GPIO4_12	NAND_READY*2		1,8V / 3,3V	
J1	2	GPIO4_11	NAND_WP*2		1,8V / 3,3V	
J1	3	GPIO4_15	NAND_CLE*2		1,8V / 3,3V	
J1	4	GPIO4_13	NAND_CE0*2		1,8V / 3,3V	
J1	5	UART_B_RXD	UART3_RX_DATA		3,3V	onboard Pull-Up 100k
J1	6	UART_A_RXD	UART1_RX_DATA		3,3V	Reserved for A7 debug, onboard Pull-Up 100k
J1	7	UART_B_TXD	UART3_TX_DATA		3,3V	
J1	8	UART_A_TXD	UART1_TX_DATA		3,3V	Reserved for A7 debug
J1	9	UART_C_CTS	CSI_DATA02		3,3V	
J1	10	CAN_A_RX	UART2_RTS	I	3,3V	onboard Pull-Up 100k
J1	11	UART_C_RTS	CSI_DATA03		3,3V	
J1	12	CAN_A_TX	UART2_CTS	O	3,3V	
J1	13	UART_C_RXD	CSI_DATA01		3,3V	onboard Pull-Up 100k
J1	14	SPI_A_SS0	UART4_RX_DATA	I	3,3V	
J1	15	UART_C_TXD	CSI_DATA00		3,3V	
J1	16	SPI_A_MISO	UART5_RX_DATA	I	3,3V	
J1	17	UART_D_RXD	CSI_PIXCLK		3,3V	onboard Pull-Up 100k
J1	18	SPI_A_MOSI	UART5_TX_DATA	O	3,3V	
J1	19	UART_D_TXD	CSI_MCLK		3,3V	
J1	20	SPI_A_SCLK	UART4_TX_DATA	O	3,3V	
J1	21	I2C_A_SCL	CSI_HSYNC	I/O	3,3V	onboard Pull-Up 2,49k
J1	22	GPIO_J1_22	CSI_DATA04		3,3V	
J1	23	I2C_A_SDA	CSI_VSYNC	I/O	3,3V	onboard Pull-Up 2,49k
J1	24	GPIO_J1_24	CSI_DATA05		3,3V	
J1	25	GPIO_J1_25	CSI_DATA07		3,3V	
J1	26	GPIO_J1_26	CSI_DATA06		3,3V	
J1	27	GPIO_J1_27	SNVS_TAMPER5		3,3V	
J1	28	GPIO_J1_28	SNVS_TAMPER4		3,3V	
J1	29	GPIO_J1_29	NAND_DQS		1,8V / 3,3V	
J1	30	GPIO_J1_30	SNVS_TAMPER6		3,3V	
J1	31	GPIO_J1_31	U\A\R\T\3_\C\T		3,3V	

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	32	GPIO_J1_32	U\A\R\T\3_\R\T		3,3V	
J1	33	N.C.				
J1	34	N.C.				
J1	35	N.C.				
J1	36	N.C.				
J1	37	N.C.				
J1	38	N.C.				
J1	39	I2C_B_IRQ	SNVS_TAMPER0		3,3V	
J1	40	N.C.				
J1	41	I2C_B_SCL	UART2_TX_DATA	I/O	3,3V	onboard Pull-Up 2,49k
J1	42	PMIC_ON_REQ	SNVS_PMIC_ON_REQ		3,3V	
J1	43	I2C_B_SDA	UART2_RX_DATA	I/O	3,3V	onboard Pull-Up 2,49k
J1	44	ON_OFF	ONOFF		3,3V	
J1	45	GND				
J1	46	GND				
J1	47	LCD_R0	LCD_DATA00		3,3V	
J1	48	BKLT_PWM	GPIO1_IO08		3,3V	Preferred as VLCD enable
J1	49	LCD_R1	LCD_DATA01		3,3V	
J1	50	LCD_PCLK	LCD_CLK		3,3V	
J1	51	LCD_R2	LCD_DATA02		3,3V	
J1	52	GND				
J1	53	LCD_R3	LCD_DATA03		3,3V	
J1	54	VLCD_EN	LCD_RESET		3,3V	Preferred as VLCD enable, onboard Pull-Up 100k
J1	55	LCD_R4	LCD_DATA04		3,3V	
J1	56	LCD_DE	LCD_ENABLE		3,3V	
J1	57	LCD_R5	LCD_DATA05		3,3V	
J1	58	LCD_HSYNC	LCD_HSYNC		3,3V	
J1	59	LCD_R6	LCD_DATA06		3,3V	
J1	60	LCD_VSYNC	LCD_VSYNC		3,3V	
J1	61	LCD_R7	LCD_DATA07		3,3V	
J1	62	GND				
J1	63	GND				
J1	64	LCD_B0	LCD_DATA16		3,3V	
J1	65	LCD_G0	LCD_DATA08		3,3V	
J1	66	LCD_B1	LCD_DATA17		3,3V	
J1	67	LCD_G1	LCD_DATA09		3,3V	
J1	68	LCD_B2	LCD_DATA18		3,3V	
J1	69	LCD_G2	LCD_DATA10		3,3V	
J1	70	LCD_B3	LCD_DATA19		3,3V	
J1	71	LCD_G3	LCD_DATA11		3,3V	
J1	72	LCD_B4	LCD_DATA20		3,3V	

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	73	LCD_G4	LCD_DATA12		3,3V	
J1	74	LCD_B5	LCD_DATA21		3,3V	
J1	75	LCD_G5	LCD_DATA13		3,3V	
J1	76	LCD_B6	LCD_DATA22		3,3V	
J1	77	LCD_G6	LCD_DATA14		3,3V	
J1	78	LCD_B7	LCD_DATA23		3,3V	
J1	79	LCD_G7	LCD_DATA15		3,3V	
J1	80	GND				
J2	1	ETH1_TX+				1st PHY 100MBit
J2	2	+V5S				
J2	3	ETH1_TX-				1st PHY 100MBit
J2	4	+V5S				
J2	5	ETH1_RX+				1st PHY 100MBit
J2	6	+V5S				
J2	7	ETH1_RX-				1st PHY 100MBit
J2	8	GND				
J2	9	N.C.				1st PHY Gbit*3
J2	10	GND				
J2	11	N.C.				1st PHY 1Gbit*3
J2	12	GND				
J2	13	N.C.				1st PHY 1Gbit*3
J2	14	ETH_A_LEDn		O	3,3V	1st PHY Activity LED
J2	15	N.C.				1st PHY 1GBit*3
J2	16	ETH_B_LEDn		O	3,3V	2nd PHY Activity LED
J2	17	GND				
J2	18	JTAG_TCK	JTAG_TCK*1		3,3V	JTAG_TCK or I2S_DIN
J2	19	ETH2_TX+				2nd PHY 100MBit
J2	20	JTAG_TMS	JTAG_TMS*1		3,3V	JTAG_TMS or I2S_MCLK
J2	21	ETH2_TX-				2nd PHY 100MBit
J2	22	JTAG_TDI	JTAG_TDI*1		3,3V	JTAG_TDI or I2S_SCLK
J2	23	ETH2_RX+				2nd PHY 100MBit
J2	24	JTAG_TDO	JTAG_TDO*1		3,3V	JTAG_TDO or I2S_LRCLK
J2	25	ETH2_RX-				2nd PHY 100MBit
J2	26	SD_A_VCC	NVCC_SD1	I	1,8V / 3,3V	Power supply in for external SDIO interface **In HW Revision 1.20 Pin can be powered on Module***
J2	27	N.C.				2nd PHY Gbit*3
J2	28	SD_A_VSEL	SNVS_TAMPER1	O	SD1_VCC	
J2	29	N.C.				2nd PHY Gbit*3
J2	30	SD_A_RST	GPIO1_IO09	O	SD1_VCC	

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	31	N.C.				2nd PHY Gbit*3
J2	32	SD_A_WP	UART1_CTS	I	3,3V	Active low write protect disable
J2	33	N.C.				2nd PHY Gbit*3
J2	34	SD_A_CD	UART1_RTS	I	3,3V	Active low card detect
J2	35	GND				
J2	36	SD_A_CMD	SD1_CMD		SD1_VCC	onboard Pull-Up 100k
J2	37	USB_OTG_VBUS	USB_OTG1_VBUS	I	5,0V	Input; USB Phy voltage supply
J2	38	SD_A_CLK	SD1_CLK		SD1_VCC	
J2	39	USB_OTG_PWRn	SNVS_TAMPER3	O	3,3V	onboard Pull-Up 100k
J2	40	SD_A_DATA0	SD1_DATA0		SD1_VCC	onboard Pull-Up 100k
J2	41	USB_OTG_ID	GPIO1_IO00	I	3,3V	Input
J2	42	SD_A_DATA1	SD1_DATA1		SD1_VCC	
J2	43	USB_OTG_DP	USB_OTG1_DP			
J2	44	SD_A_DATA2	SD1_DATA2		SD1_VCC	
J2	45	USB_OTG_DN	USB_OTG1_DN			
J2	46	SD_A_DATA3	SD1_DATA3		SD1_VCC	
J2	47	GND				
J2	48	VDD_VBAT		I		RTC battery Input
J2	49	N.C.				
J2	50	VDD_SNVS		I		SNVS voltage Input **In HW Revision 1.20 Pin can be powered on Module***
J2	51	N.C.				
J2	52	PowerGood		O	3,3V	PowerGood Signal to enable external power regulators
J2	53	N.C.				
J2	54	RESETINn			VDD_SNVS	Power on reset Input; onboard Pull-up 10k
J2	55	N.C.				For future use
J2	56	PMIC_STBY	CCM_PMIC_STBY_R		3,3V	
J2	57	GND				
J2	58	N.C.				For future use
J2	59	USB_H_VBUS	USB_OTG2_VBUS	I	5,0V	USB Phy voltage supply; Preferred for host
J2	60	N.C.				
J2	61	USB_H_DN	USB_OTG2_DN			90 Ohm differential pair; Preferred for host
J2	62	ADC_H	GPIO1_IO04		3,3V	
J2	63	USB_H_DP	USB_OTG2_DP			90 Ohm differential pair; Preferred for host

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	64	ADC_G	GPIO1_IO02		3,3V	
J2	65	USB_H_PWRn	SNVS_TAMPER2	O	3,3V	onboard Pull-Up 100k
J2	66	ADC_F	GPIO1_IO03		3,3V	
J2	67	AUDIO_A_VCC		I	3V	Noise reduced external power supply for audio codec
J2	68	ADC_E	GPIO1_IO01		3,3V	
J2	69	AUDIO_A_GND		I		Noise reduced external power supply for audio codec
J2	70	N.C.				
J2	71	AUDIO_A_OUT_L	JTAG_TRST*1	O	3,3V	onboard Pull-Up 100k*1
J2	72	BOOTSELn			3,3V	Service jumper; normally left open
J2	73	AUDIO_A_OUT_R		O		
J2	74	GND				
J2	75	AUDIO_A_ MIC		I		
J2	76	AUDIO_A_ HP_L	SNVS_TAMPER9*1	O	3,3V	onboard Pull-Up 2,49k*1
J2	77	AUDIO_A_IN_L				
J2	78	AUDIO_A_ HP_R	SNVS_TAMPER8*1	O	3,3V	onboard Pull-Up 2,49k*1
J2	79	AUDIO_A_IN_R				
J2	80	AUDIO_A_HP_GND		O		Never connect to GND!

Table 1: B2B connector

*1 Option in case Audio Codec isn't mounted

*2 Option only available in case eMMC is mounted

*3 PicoCoreMX6UL only support 100Mbit

*optional

4 Interfaces

4.1 USB Host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports, ESD and EMV protection is required nearby the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	59	USB_H1_VBUS	USB_OTG2_VBUS	I	5,0V	USB Phy voltage supply; Preferred for host
J2	61	USB_H1_DN	USB_OTG2_DN			90 Ohm differential pair; Preferred for host
J2	63	USB_H1_DP	USB_OTG2_DP			90 Ohm differential pair; Preferred for host
J2	65	USB_H1_PWRn	SNVS_TAMPER2	O	3,3V	Power enable; onboard Pull-Up 100k

Table 2: USB Host Interface

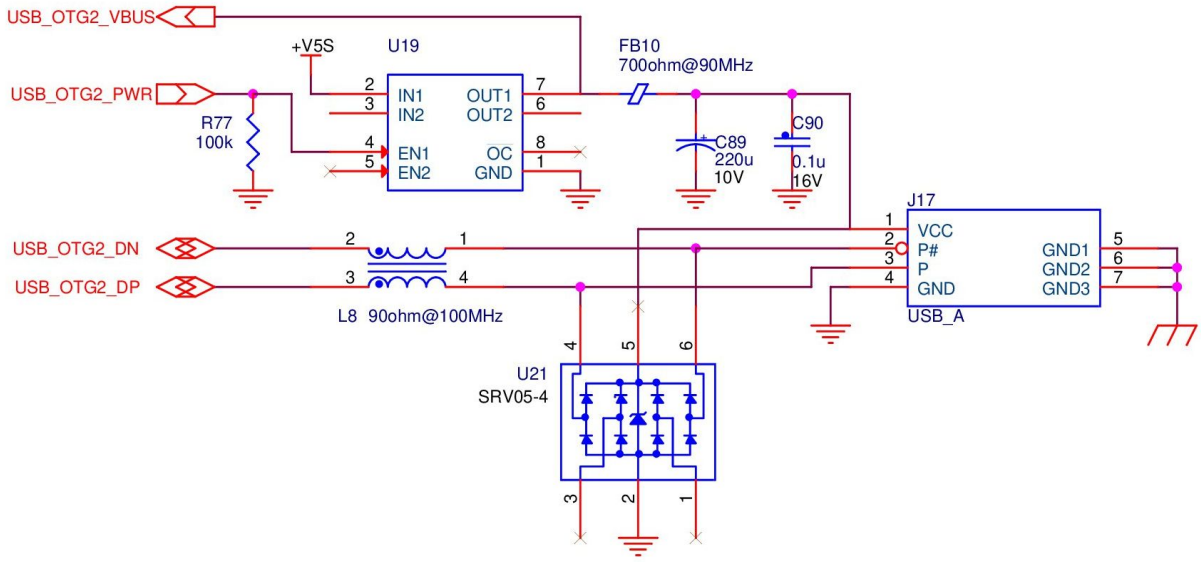

Figure 4: USB Host Full Feature Example

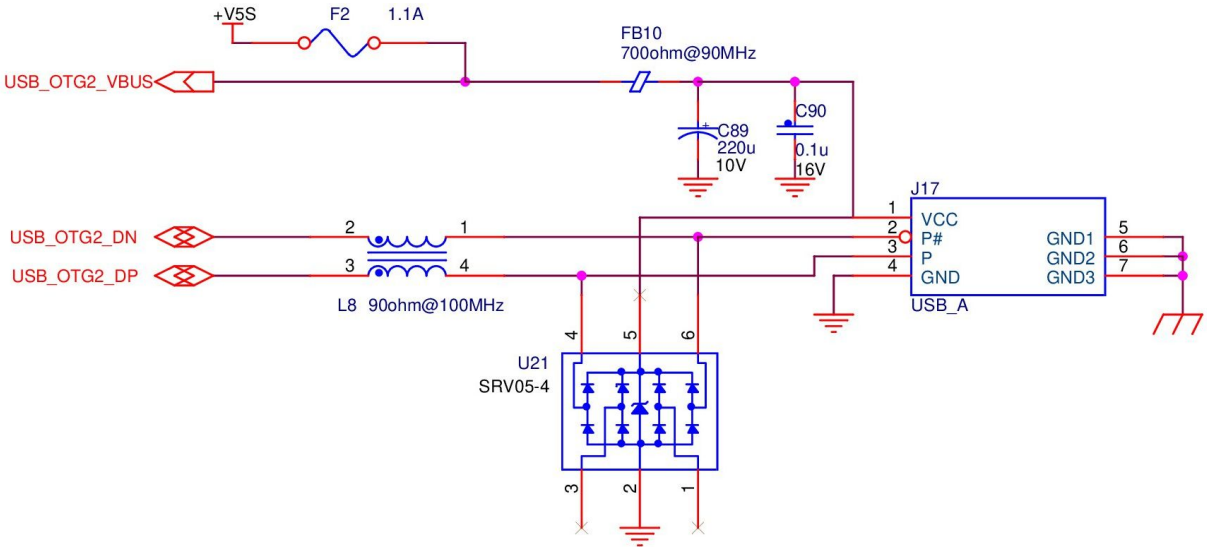

Figure 5: USB Host Basic Feature Example

4.2 USB OTG

The 90 Ohm differential pair of USB signals don't need any termination. For external ports, ESD and EMV protection is required nearby the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	37	USB_OTG1_VBUS	USB_OTG1_VBUS	I	5,0V	Input; USB Phy voltage supply
J2	39	USB_OTG1_PWRn	SNVS_TAMPER3	O	3,3V	onboard Pull-Up 100k
J2	41	USB_OTG1_ID	GPIO1_IO00	I	3,3V	Input
J2	43	USB_OTG1_DP	USB_OTG1_DP			90 Ohm differential pair
J2	45	USB_OTG1_DN	USB_OTG1_DN			

Table 3: USB OTG Interface

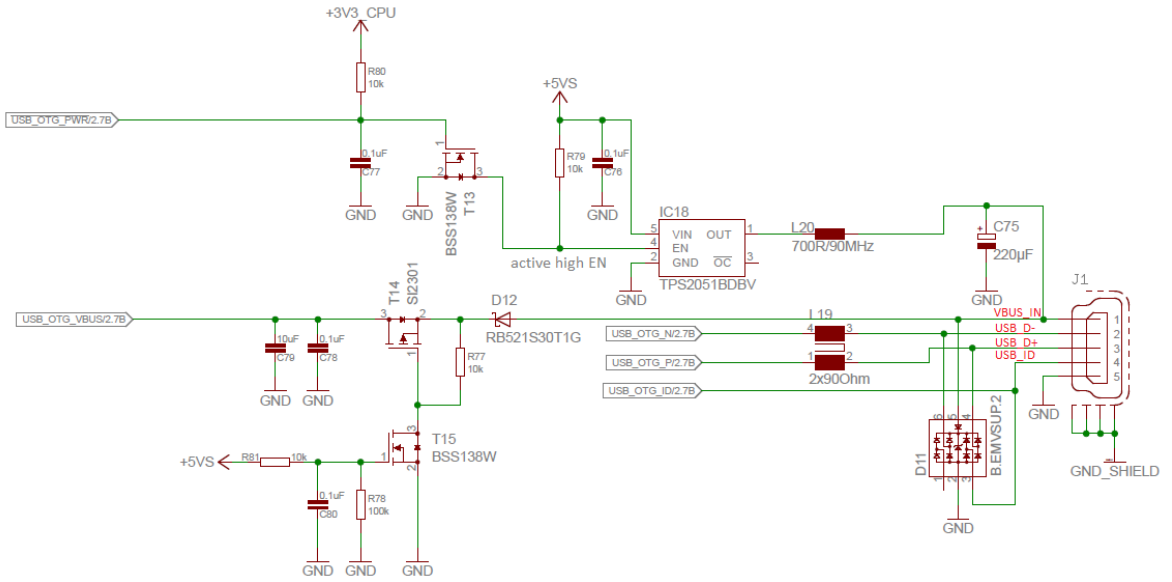

Figure 6: USB OTG full feature example

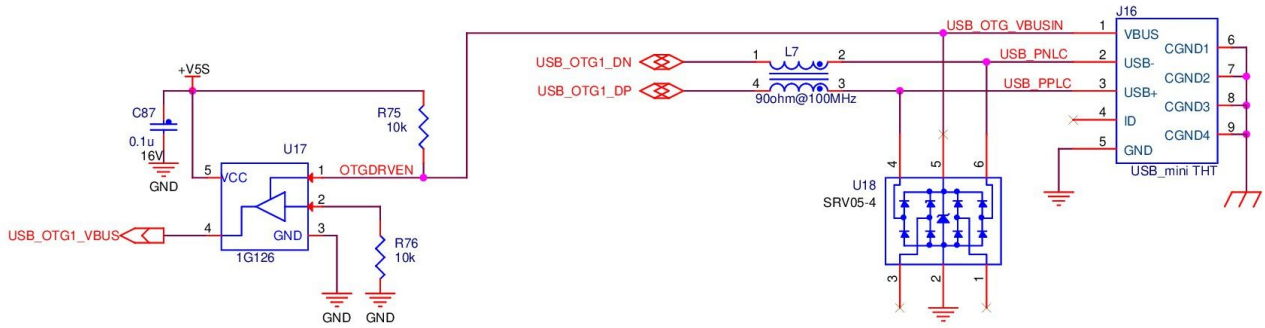

Figure 7: Basic USB Device Example

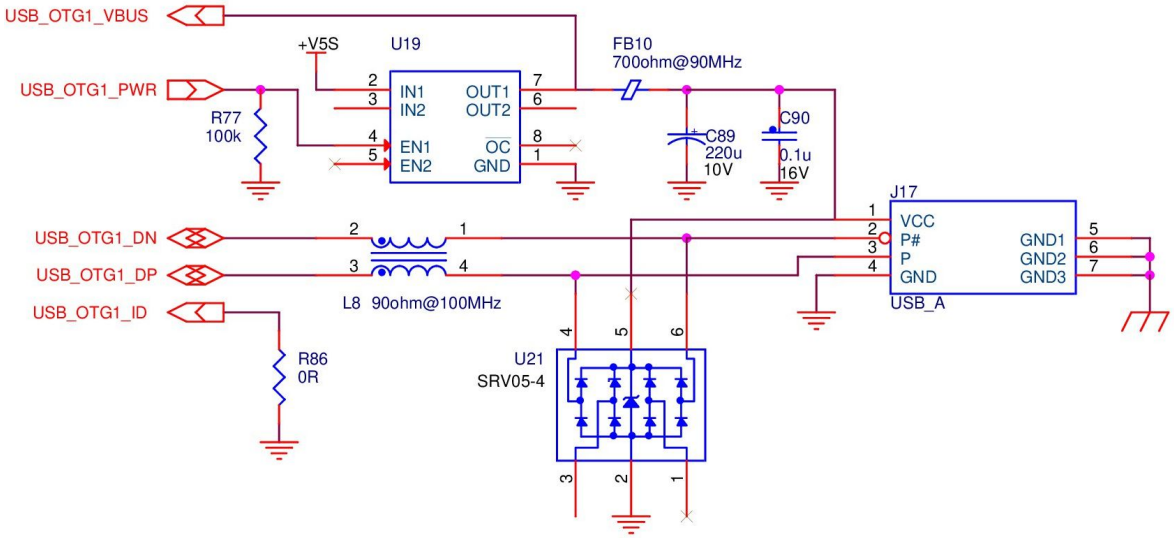

Figure 8: USB OTG Host example

4.3 CAN Bus

The chip does provide the CAN bus transmit and receive TTL signal without any termination. Needs an interface chip to the CAN bus. If not used, please left signals unconnected.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	10	CAN_A_RX	UART2_RTS	I	3,3V	onboard Pull-Up 100k
J1	12	CAN_A_TX	UART2_CTS	O	3,3V	

Table 4: CAN Bus Interface

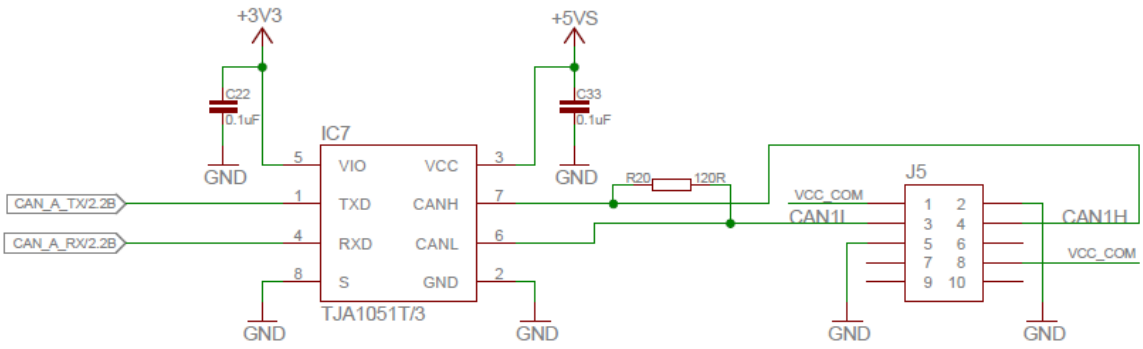

Figure 9: CAN transceiver example

4.4 SD card

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	26	SD_A_VCC	NVCC_SD1	I	1,8V / 3,3V	Power supply in for external SDIO interface
J2	28	SD_A_VSEL	SNVS_TAMPER1	O	SD1_VCC	
J2	30	SD_A_RST	GPIO1_IO09	O	SD1_VCC	
J2	32	SD_A_WP	UART1_CTS	I	3,3V	Active low write protect disable
J2	34	SD_A_CD	UART1_RTS	I	3,3V	Active low card detect
J2	36	SD_A_CMD	SD1_CMD		SD1_VCC	onboard Pull-Up 100k
J2	38	SD_A_CLK	SD1_CLK		SD1_VCC	
J2	40	SD_A_DATA0	SD1_DATA0		SD1_VCC	onboard Pull-Up 100k
J2	42	SD_A_DATA1	SD1_DATA1		SD1_VCC	
J2	44	SD_A_DATA2	SD1_DATA2		SD1_VCC	
J2	46	SD_A_DATA3	SD1_DATA3		SD1_VCC	

Table 5: SD Card Interface

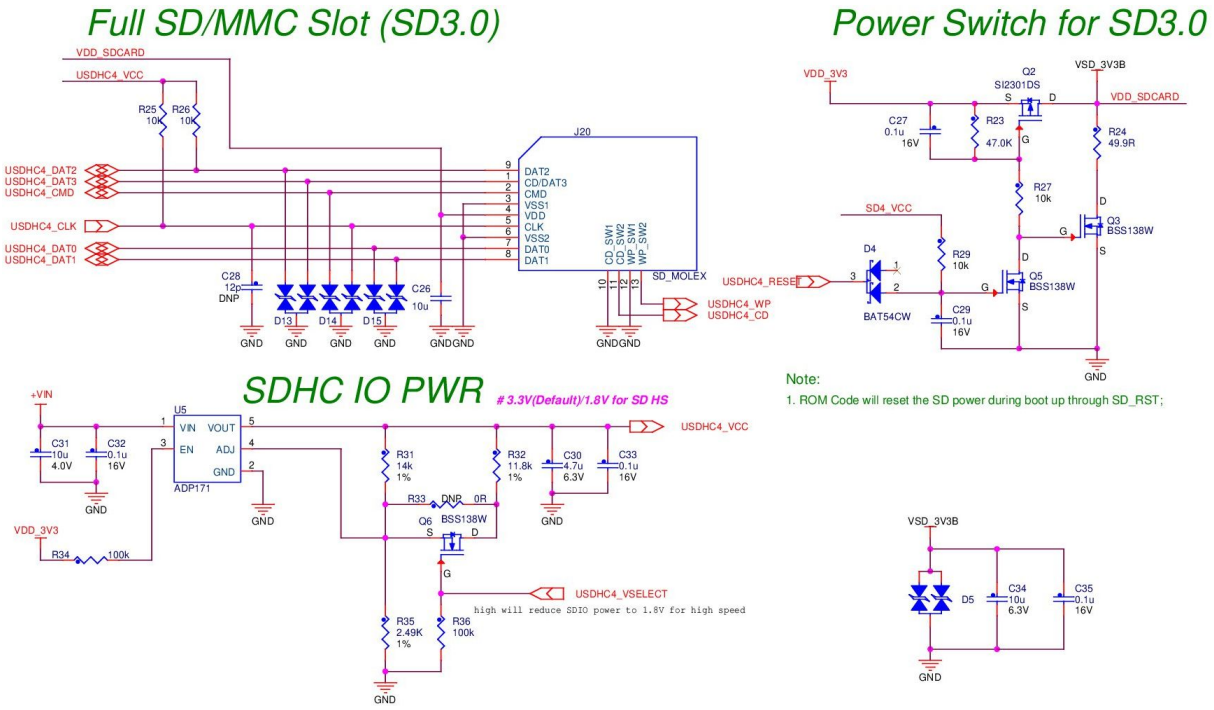

Figure 10: SDHC full feature example

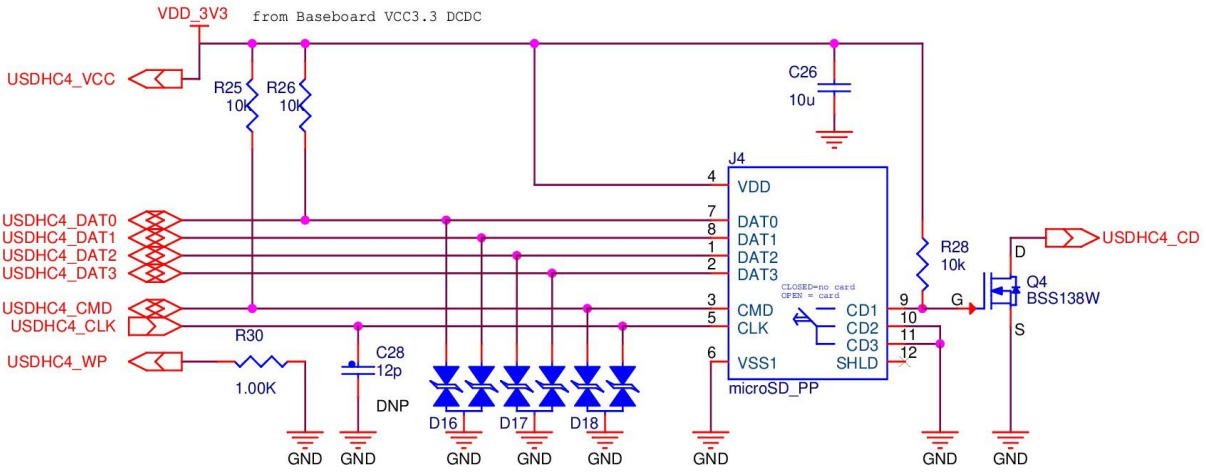

Figure 11: SD basic feature w/o high speed support

4.5 SPI

The module support HS SPI (Serial Peripheral Interface) with 1 chip. All signals are 3.3V compliant. Devices on baseboard with other voltage need a level shifter.

Signals don't have pullups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	14	SPI_A_SS0	UART4_RX_DATA	I	3,3V	
J1	16	SPI_A_MISO	UART5_RX_DATA	I	3,3V	
J1	18	SPI_A_MOSI	UART5_TX_DATA	O	3,3V	
J1	20	SPI_A_SCLK	UART4_TX_DATA	O	3,3V	

Table 6: SPI Interface

4.6 I2C

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	21	I2C_A_SCL	CSI_HSYNC		3,3V	onboard Pull-Up 2,49k
J1	23	I2C_A_SDA	CSI_VSYNC		3,3V	onboard Pull-Up 2,49k
J1	39	I2C_B_IRQ	SNVS_TAMPER0		3,3V	
J1	41	I2C_B_SCL	UART2_TX_DATA		3,3V	onboard Pull-Up 2,49k
J1	43	I2C_B_SDA	UART2_RX_DATA		3,3V	onboard Pull-Up 2,49k

Table 7: I2C A and I2C B Interface

4.7 Serial ports

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	6	UART_A_RXD	UART1_RX_DATA		3,3V	Reserved for A7 debug, onboard Pull-Up 100k
J1	8	UART_A_TXD	UART1_TX_DATA		3,3V	Reserved for A7 debug
J1	5	UART_B_RXD	UART3_RX_DATA		3,3V	onboard Pull-Up 100k
J1	7	UART_B_TXD	UART3_TX_DATA		3,3V	
J1	9	UART_C_CTS	CSI_DATA02		3,3V	
J1	11	UART_C_RTS	CSI_DATA03		3,3V	
J1	13	UART_C_RXD	CSI_DATA01		3,3V	onboard Pull-Up 100k
J1	15	UART_C_TXD	CSI_DATA00		3,3V	
J1	17	UART_D_RXD	CSI_PIXCLK		3,3V	onboard Pull-Up 100k
J1	19	UART_D_TXD	CSI_MCLK		3,3V	

Table 8: UART A/B/C/D Interface

We recommend using UART_A for debugging and service only.

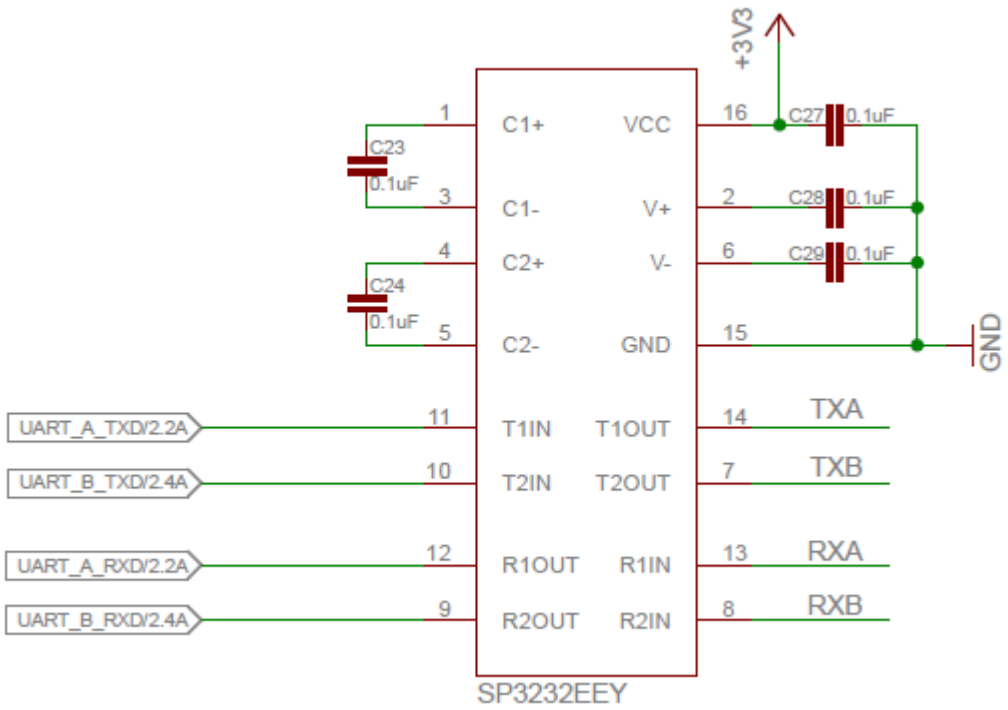

Figure 12: UART transceiver example

4.8 Ethernet

The module supports two 10/100 Mbit LAN interfaces. Two 10Base-T/100Base-TX PHY Micrel KSZ8081RNA are mounted on the module.

	Pin	Signal	Function	I/O	Voltage	Description
J2	1	ETH_A_D1_P	ETH1_TX+	O		1st PHY 100MBit Differential data line
J2	3	ETH_A_D1_N	ETH1_TX-	O		
J2	5	ETH_A_D2_P	ETH1_RX+	I		1st PHY 100MBit Differential data line
J2	7	ETH_A_D2_N	ETH1_RX-	I		
J2	9	ETH_A_D3_P	N.C.	O		1st PHY Gbit*3 Differential data line
J2	11	ETH_A_D3_N	N.C.*1	O		
J2	13	ETH_A_D4_P	N.C.	I		1st PHY 1Gbit*3 Differential data line
J2	15	ETH_A_D4_N	N.C. *1	I		
J2	14	ETH_A_LEDn		O	3,3V	1st PHY Activity LED, ON at LINK, BLINK at traffic
J2	19	ETH_B_D1_P	ETH2_TX+	O		2nd PHY 100MBit Differential data line
J2	21	ETH_B_D1_N	ETH2_TX-	O		
J2	23	ETH_B_D2_P	ETH2_RX+	I		2nd PHY 100MBit Differential data line
J2	25	ETH_B_D2_N	ETH2_RX-	I		
J2	27	ETH_B_D3_P	N.C.	O		2nd PHY Gbit*3 Differential data line
J2	29	ETH_B_D3_N	N.C. *1	O		
J2	31	ETH_B_D4_P	N.C.	I		2nd PHY Gbit*3 Differential data line
J2	33	ETH_B_D4_N	N.C. *1	I		
J2	16	ETH_B_LEDn		O	3,3V	2nd PHY Activity LED, ON at LINK, BLINK at traffic

Table 9: LAN A and LAN B Interface

*1 PicoCoeMX6UL HW Revision 1.00: These signals are wrongly connected to GND. If you connect the signals to be compatible to PicoCoreMX6SX LAN will not work with PicoCoreMX6UL. In case you connect these signals to a GBit LAN transceiver please foresee 0R resistor to open connection. This problem is fixed with HW rev 1.10.

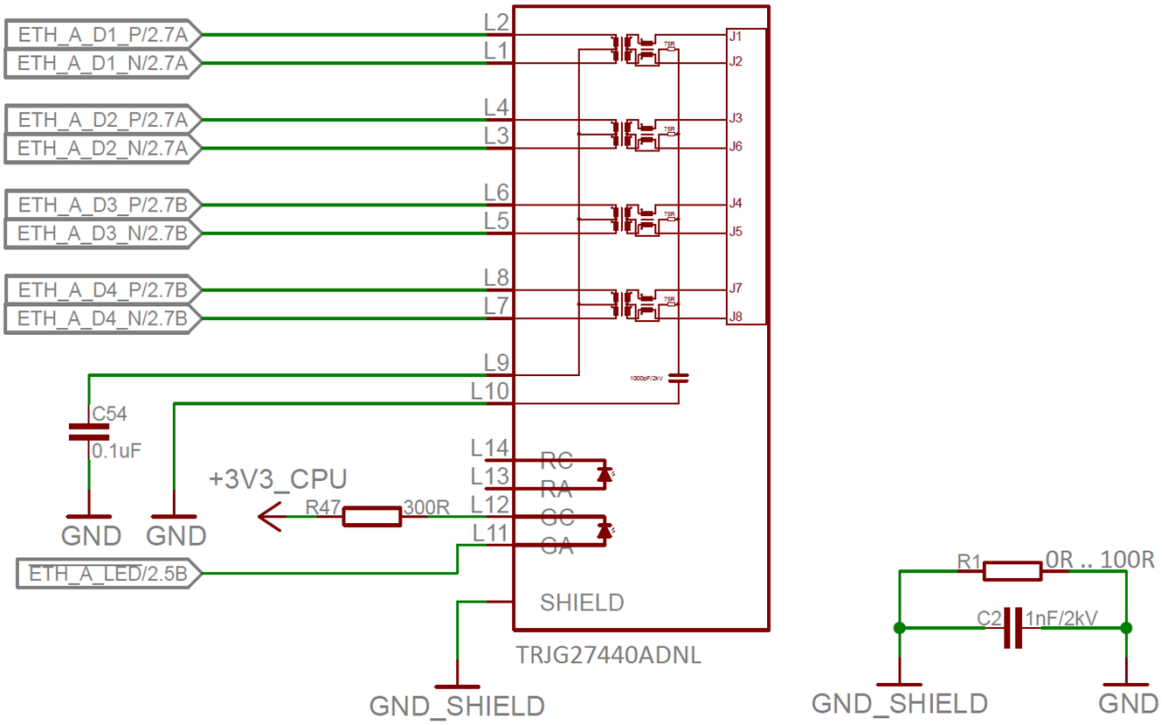

Figure 13: LAN output example

4.9 Audio

The audio codec NXP SGTL5000 is mounted on this module.

	Pin	Signal	I/O	Voltage	Description
J2	67	VCC_AUD	I	3V	Noise reduced external power supply for audio codec
J2	69	GND_AUD	I		Noise reduced external power supply for audio codec
J2	71	LINEOUT_L	O	3,3V	onboard Pull-Up 100k*1
J2	73	LINEOUT_R	O		
J2	75	MIC	I		
J2	76	HP_L	O	3,3V	onboard Pull-Up 2,49k*1
J2	77	LINEIN_L	I		
J2	78	HP_R	O	3,3V	onboard Pull-Up 2,49k*1
J2	79	LINEIN_R	I		
J2	80	HP_GND	O		Never connect to GND!

Table 10: Audio Interface

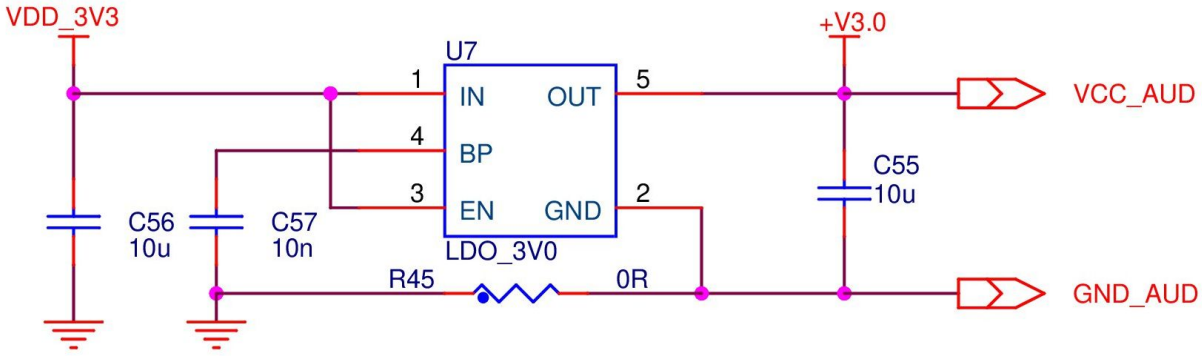

Figure 14: Baseboard LDO power supply for codec analog voltage

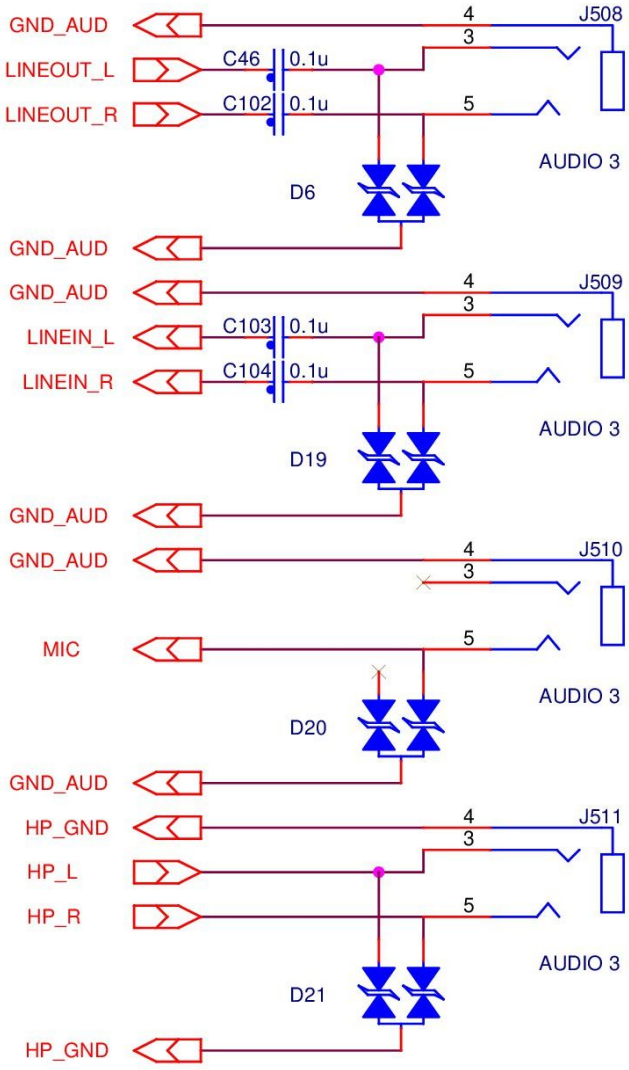

Figure 15 : Audio In and Out

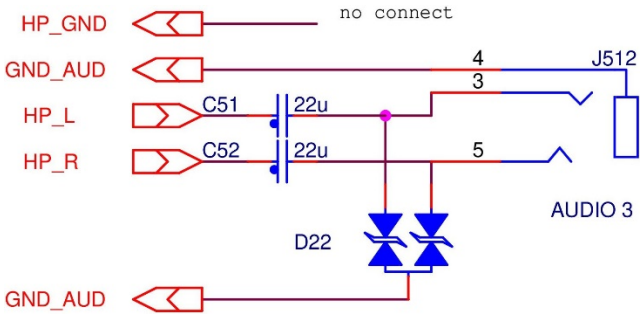

Figure 16 Cap-coupled version of headphone out with GND instead HP_GND

4.10 RGB LCD

	Pin	Signal	CPU Pad	I/O	Voltage	18bit[1]	24bit
J1	47	LCD_R0	LCD_DATA00	O	VCC3.3	n.a.	R0
J1	49	LCD_R1	LCD_DATA01	O	VCC3.3	n.a.	R1
J1	51	LCD_R2	LCD_DATA02	O	VCC3.3	R0	R2
J1	53	LCD_R3	LCD_DATA03	O	VCC3.3	R1	R3
J1	55	LCD_R4	LCD_DATA04	O	VCC3.3	R2	R4
J1	57	LCD_R5	LCD_DATA05	O	VCC3.3	R3	R5
J1	59	LCD_R6	LCD_DATA06	O	VCC3.3	R4	R6
J1	61	LCD_R7	LCD_DATA07	O	VCC3.3	R5	R7
J1	65	LCD_G0	LCD_DATA08	O	VCC3.3	n.a.	G0
J1	67	LCD_G1	LCD_DATA09	O	VCC3.3	n.a.	G1
J1	69	LCD_G2	LCD_DATA10	O	VCC3.3	G0	G2
J1	71	LCD_G3	LCD_DATA11	O	VCC3.3	G1	G3
J1	73	LCD_G4	LCD_DATA12	O	VCC3.3	G2	G4
J1	75	LCD_G5	LCD_DATA13	O	VCC3.3	G3	G5
J1	77	LCD_G6	LCD_DATA14	O	VCC3.3	G4	G6
J1	79	LCD_G7	LCD_DATA15	O	VCC3.3	G5	G7
J1	64	LCD_B0	LCD_DATA16	O	VCC3.3	n.a.	B0
J1	66	LCD_B1	LCD_DATA17	O	VCC3.3	n.a.	B1
J1	68	LCD_B2	LCD_DATA18	O	VCC3.3	G0	B2
J1	70	LCD_B3	LCD_DATA19	O	VCC3.3	G1	B3
J1	72	LCD_B4	LCD_DATA20	O	VCC3.3	G2	B4
J1	74	LCD_B5	LCD_DATA21	O	VCC3.3	G3	B5
J1	76	LCD_B6	LCD_DATA22	O	VCC3.3	G4	B6
J1	78	LCD_B7	LCD_DATA23	O	VCC3.3	G5	B7
J1	56	LCD_DE	LCD_ENABLE	O	VCC3.3		
J1	58	LCD_HSYNC	LCD_HSYNC	O	VCC3.3		
J1	60	LCD_VSYNC	LCD_VSYNC	O	VCC3.3		
J1	50	LCD_PCLK	LCD_CLK	O	VCC3.3		
J1	54	VLCD_EN	LCD_RESET	O	VCC3.3	Preferred as VLCD enable	
J1	48	BKLT_PWM	GPIO1_IO08	O	VCC3.3	Preferred for backlight PWM	

Table 11: Display Interface

Because all signals does work with 3.3V TTL level and high speed, high EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary. Using serial resistors or EMI filter network (e.g. Nexperia IP4254CZ16) is highly recommended. For additional controls use GPIOs and modify the driver.

[1] By default, we use 24 bit output data path also for 18Bit displays. The IOMUX for unused data bits R0/R1, G0/G1 and B0/B1 are NOT configured for LCDIF and therefore can be used for different function.

4.11 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. In addition, a higher voltage as the announced IO power is not allowed.

4.12 ADC

There are 2 12bit ADC converter included in CPU with 4 inputs each. Because the reference voltage is the 3.3V power supply with 5% tolerance, the accuracy is limited. The ADC input signals connect to GPIO1[0:9] CPU pads.

For electrical details please refer the datasheet from NXP.

4.13 JTAG

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	18	JTAG_TCK	JTAG_TCK*1		3,3V	JTAG_TCK
J2	20	JTAG_TMS	JTAG_TMS*1		3,3V	JTAG_TMS
J2	22	JTAG_TDI	JTAG_TDI*1		3,3V	JTAG_TDI
J2	24	JTAG_TDO	JTAG_TDO*1		3,3V	JTAG_TDO

Table 12: JTAG Interface

- If Audio Codec is mounted on PicoCOREMX6UL, JTAG is NOT available
- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.14 Power and Power Control Pins

	Pin	Signal	I/O	Description
J2	2 4 6	VIN (+V5S)	I	Main Power supply input please refer chapter 8 Electrical characteristic
J2	48	VDD_VBAT	I	RTC battery input; tie to VDD_SNVS if you don't need RTC; **don't leave unconnected** please refer chapter 8 Electrical characteristic
J2	50	VDD_SNVS	I	SNVS voltage input; tie to 3.3V. Don't leave unconnected.
J2	52	PowerGood	O	PowerGood Signal to enable external power regulators
J2	26	SD_A_VCC	I	SDHC power input; 3.3V/ 1.8V
J2	37	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	59	USB_H_VBUS	I	USB Phy voltage input; 5V
J2	54	RESETIN	I	Power on reset input; 10k PU
J2	56	PMIC_STBY_REQ	O	

Table 13: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

VDD_SNVS could be powered separately in special secure Non-Volatile Storage schemes. In normal usage just tie to 3.3V.

PowerGood can be used as enable for baseboard power regulators.

RESETIN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On module DCDCs will not get a reset. On power fail VIN has to be switched off and on to avoid latchup effects.

PMIC_STBY_REQ is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

5 Flash

5.1 NAND Flash

By default, boot mode is configured for NAND boot.

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S or TFAT to be robust against power failures

5.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

5.3 I2C EEPROM

This component is optional and not mounted in all configurations. Please contact sales to get more information.

6 RTC

There is a NXP PCF85263ATL or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

The Pin VDD_VBAT must be connected! Don’t leave the pin open! (For HW Revision <1.20).

7 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

8 Electrical characteristic

VIN: 3.8V .. 5.5V

VBAT In for RTC: 2.2 … 3.45V

power consumption

typical current consumption BATT: 0.22 µA

maximum power consumption BATT: 0.6 µA @85°C

Thermal design power (summary all chips)

With 900 MHz 6ULL CPU max. 2.2W @25°C

Power consumption of connected devices like display, USB devices, SD card has to be added for power calculation.

Real power consumption could be much lower depends CPU workload, used graphic interfaces and features and the workload on I/O interfaces.

8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V

Table 14: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VIN	Module main power		3.8	5.5	V
VBAT	RTC power		0.9	5.5	V
USDHC4_VCC	SDHC power		1.65	3.6	
I_{USDHC4}	SDHC controller supply current			25	mA
USB_OTG*_VBUS	USB supply voltage		4.4	5.5	
I_{VBUS}	USB supply current			100	mA
VDD_SNVS_IN	SNVS supply		2.4	3.6	V
OVDD	On module 3.3V DCDC		3.15	3.45	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

Table 15: DC Electrical Characteristics

OVDD = power on pin 3.3V from on module DCDC

9 Thermal Specification

	Min	Typ	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MX6ULL	0		+95	°C
Junction temperature i.MX6ULL (“I”) [2]	-40		+105	°C
Junction to Top of i.MX6ULL (Psi-JT)[3]		2,3		°C/W

[1] Depending on cooling solution. See also: *Power consumption and cooling*

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2. Valid for 14x14mm package.

10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMI Implementation on COM

Like all other COM modules at the market, there is no ESD protection on any signal out from the COM module. ESD protection has to be placed as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **should not exceed the maximum operating temperature of the board**.

The maximum power consumption of the board could be 5.5 Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Dependent from your application and your worst-case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend measuring this with your application. We see values between one and max. 3.5 Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet (VK package starting page 27)

- i.MX6ULL C-Temp CPU datasheet from NXP
- i.MX6ULL I-Temp CPU datasheet from NXP
- AN4579 from NXP: Thermal management guidelines

- AN5337 from NXP: i.MX 6ULL Product Lifetime Usage Estimates
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products will shipping either in trays or in bags.
These modules ship in trays. One tray can hold 10 boards. An empty tray will be used as top cover.

17 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 16: Matrix Code Sticker

18 Appendix

Important Notice

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