Hardware Documentation

armStone™ MX8M
for HW Revision 1.00

Version 002
(2020-09-14)

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About This Document

This document describes how to use the armStone™MX8M board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
07.10.2019	001	All		-	Initial Version	MW
17.07.2020	002	All	A	7	Add ADP-NT24V2	MW

V Version
A,M,R Added, Modified, Removed
Au Author

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1 Block Diagram

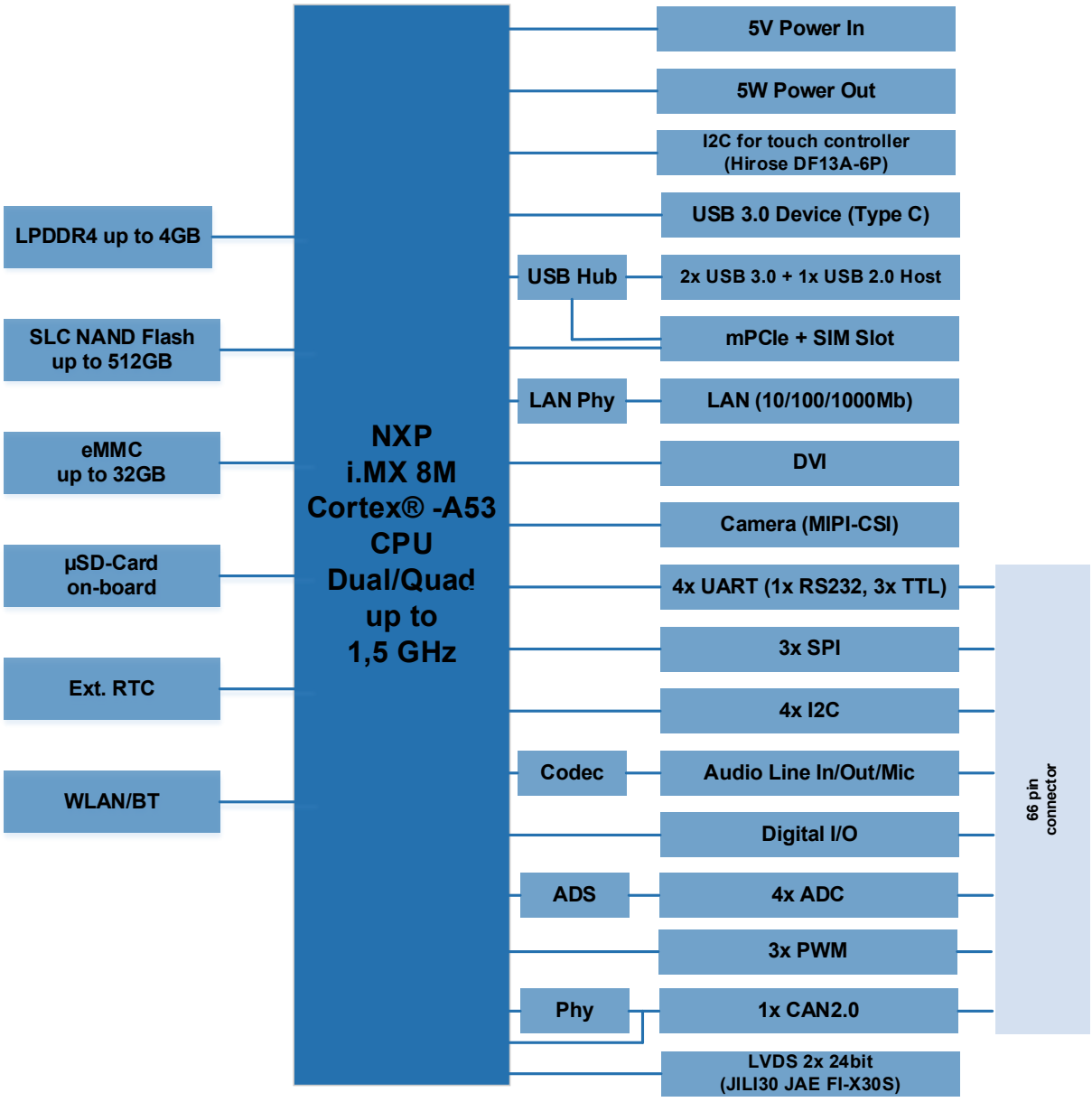


Figure 1: Block Diagram

2 Mechanical Dimension

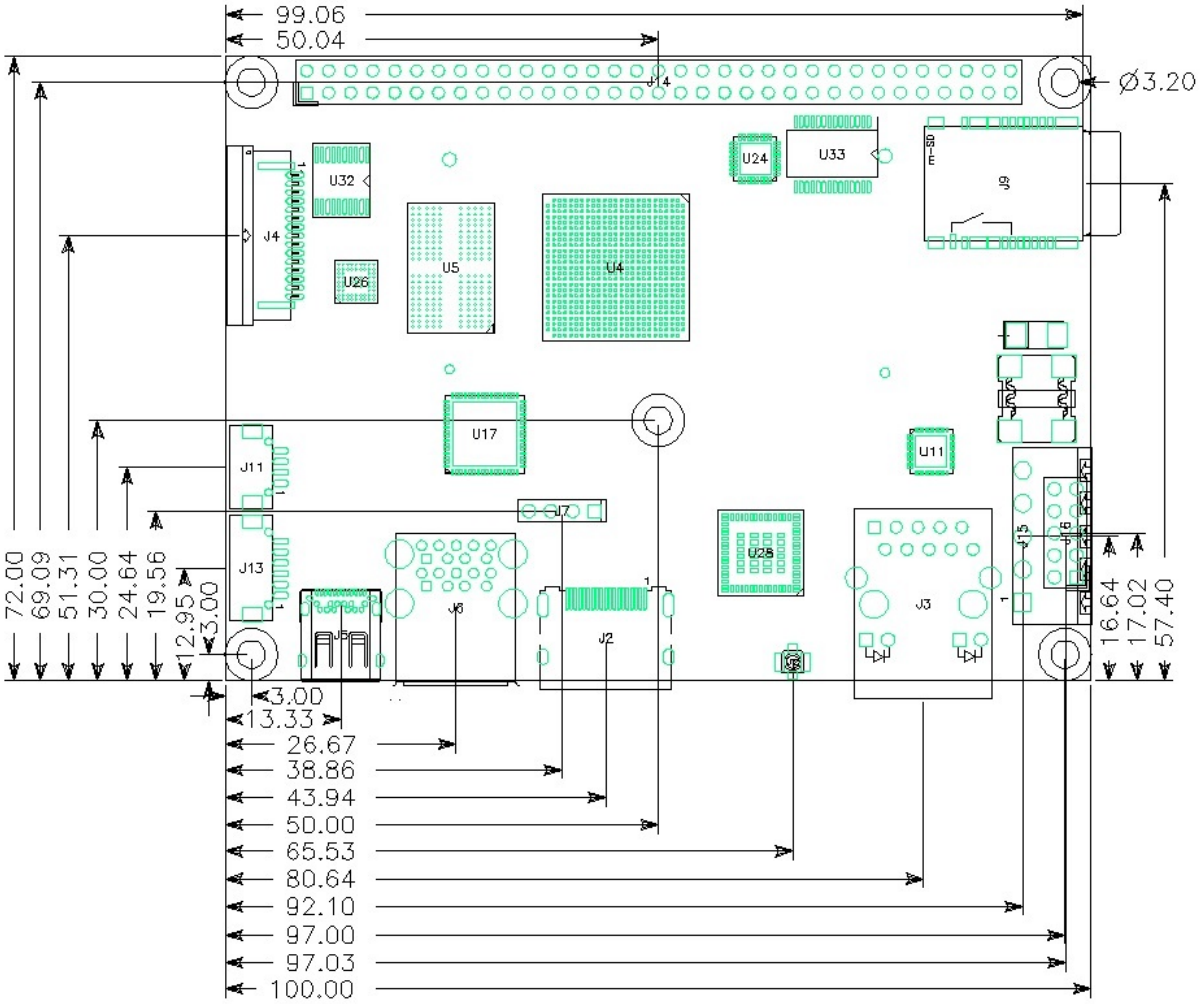


Figure 2: Mechanical Dimension Top

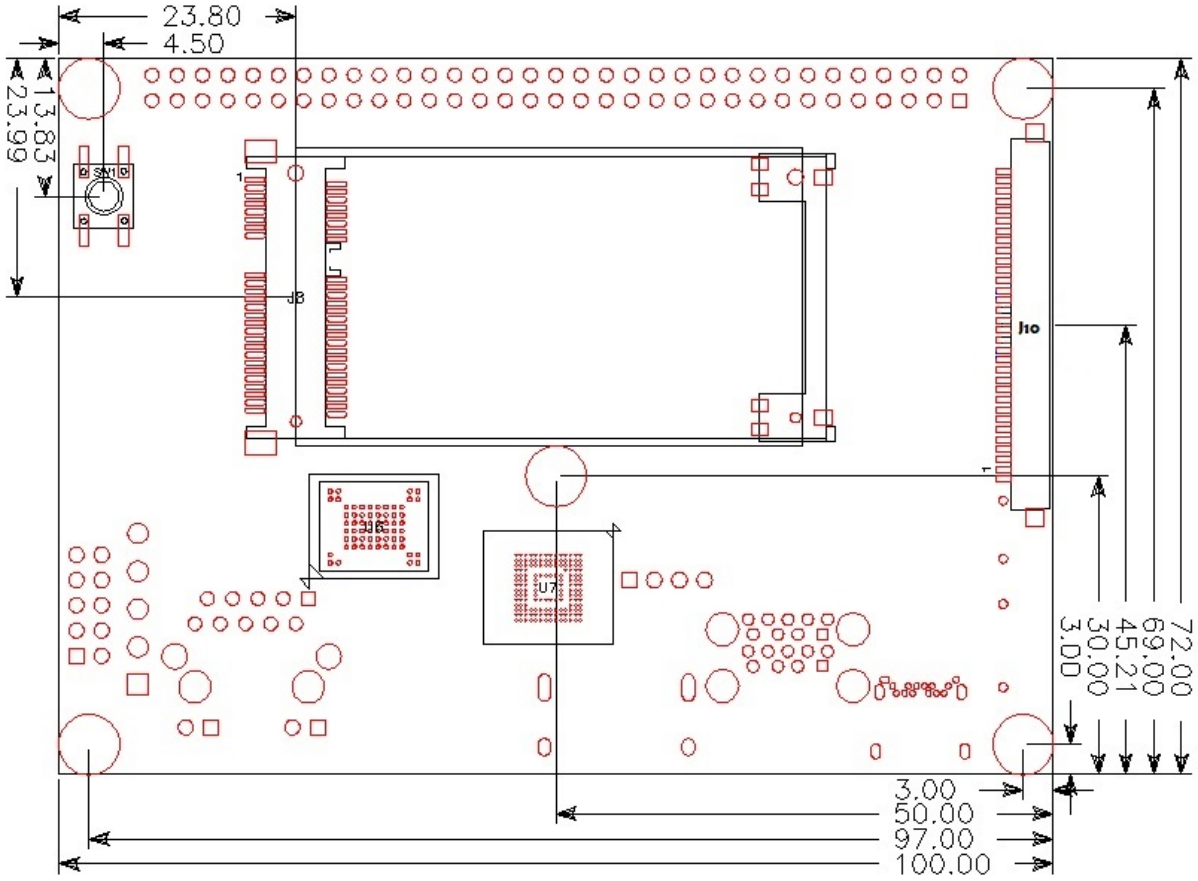


Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	100mm x 72mm
PCB Thickness	1.5mm ± 0.1mm
Height of the parts on the top side	15.5mm
Height of the parts on the bottom side	5.9mm
Weight	55gr.

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 Connectors Layout

All connectors and Pin 1 markers shown in the mechanical dimensions.

	Description	Remarks
J2	HDMI	Top Side, 19 Pins
J3	Ethernet 1xGBit RJ45 With Integrated Magnetics	Top Side, 14 Pins
J4	Camera-Connector	Top Side, 15 Pins
J5	USB-Device, USB Type-C Connector	Top Side, 24 Pins
J6	USB-Host, Stacked USB Type-A Connector	Top Side, 18 Pins
J7	USB-Host, Internal 2.54mm Pitch Connector	Top Side, 4 Pins
J8	Mini-PCE Express Connector	Bottom Side, 52 Pins
J9	MicroSD / MicroSIM Connector	Top Side, 22 Pins
J10	LVDS-Connector	Bottom Side, 30 Pins
J11	Backlight Connector	Top Side, 4 Pins
J12	WLAN IPEX Antenna Connector	Top Side, 2 Pins
J13	Touch Connector	Top Side, 6 Pins
J14	Feature Connector, 2.54mm Pitch Connector	Top Side, 66 Pins
J15	Power Connector	Top Side, 5 Pins
J16	Power Connector, 2.54mm Pitch Connector	Top Side, 10 Pins

Table 2: Connectors Layout

3 Interface and Signal Description

3.1 Power Supply

The armStone board has per default a 5 way connector with 3,81mm pitch for an external DC power supply. The connector is compatible to F&S power supply ADP-NT24V2 (IN 13-36V, OUT 5V+12V)

Connector Base Board: Würth WR-TBL Series 322 – 5- pins

Matching Connector: Würth WR-TBL Series 2109.

Optional a 10 pin connector with 2.54mm pitch can be placed.

J15 Pin	Signal Name	I/O	Remarks
1	NC		
2	VBAT_IN	PWR	Voltage: 2.2V-3.45V (*Optional for external RTC voltage supply)
3	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
4	GND_IN	PWR	
5	+V3.3	OUT	

Table 3: Power J15 Connector Pin Layout

J16 Pin	Signal Name	I/O	Remarks
1	VBAT_IN	PWR	Voltage: 2.2V-3.45V (*Optional for external RTC voltage supply)
2	VBAT_IN	PWR	Voltage: 2.2V-3.45V (*Optional for external RTC voltage supply)
3	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
4	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
5	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
6	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
7	GND_IN	PWR	
8	GND_IN	PWR	
9	GND_IN	PWR	
10	GND_IN	PWR	

Table 4: Power Connector Pin Layout

4 Interfaces

4.1 USB Host

There are 4 USB Host Ports available on the armStoneMX8M. Two of them are on the stacked USB Type-A Connector (USB3.0), one is for internal usage on 4 pins with a pitch of 2.54mm (USB2.0) and the last one, on the MiniPCI Express connector (USB2.0). All 4 ports are provided by an USB3.0 HUB, which is connected to USB2 of the i.MX8M

The USB signals are routed as 90 Ohm differential pairs. ESD and EMV protection is included in PCB design.

J6 Pin	Signal	I/O	Voltage	Description
1	USB_H1_PWR	O	5,0V	Output voltage, switched by USB Switch
2	USB_H1_DN	I/O		90 Ohm differential pair
3	USB_H1_DP	I/O		
4	GND	O		
5	USB_H1_RXN	I		90 Ohm differential pair
6	USB_H1_RXP	I		
7	GND			
8	USB_H1_TXN	O		90 Ohm differential pair
9	USB_H1_TXP	O		
10	USB_H2_PWR	O	5,0V	Output voltage, switched by USB Switch
11	USB_H2_DN	I/O		90 Ohm differential pair
12	USB_H2_DP	I/O		
13	GND	O		
14	USB_H2_RXN	I		90 Ohm differential pair
15	USB_H2_RXP	I		
16	GND			
17	USB_H2_TXN	O		90 Ohm differential pair
18	USB_H2_TXP	O		

Table 5: USB Host Interface (Type-A Connector)

J7 Pin	Signal	I/O	Voltage	Description
1	USB_H3_PWR	O	5,0V	Output voltage, secured by an 1.1A Fuse
2	USB_H3_DN	I/O		90 Ohm differential pair
3	USB_H3_DP	I/O		
4	GND	O		

Table 6: USB Host Interface (Internal Connector)

4.2 USB OTG

The USB OTG Port is realised on a USB Type-C connector with USB3.1 functionality.

The USB signals are routed as 90 Ohm differential pairs. ESD and EMV protection is included in PCB design.

J6 Pin	Signal	I/O	Voltage	Description
A1 B1	GND	PWR		
A2 B2	USB1_TXP	O		90 Ohm differential pair
A3 B3	USB1_TXN	O		
A4 B4	USB1_VBUS	PWR	5V	Input in device mode and output in host mode
A5	USB1_CC1	I		
B5	USB1_CC2	I		
A6 B6	USB1_DP	I/O		90 Ohm differential pair
A7 B7	USB1_DN	I/O		
A8	USB1_SBU1			Not connected
B8	USB1_SBU2			Not connected
A9 B9	USB1_VBUS	PWR		Input in device mode and output in host mode, Shared with A4, B4
A10 B10	USB1_RXN	I		90 Ohm differential pair
A11 B11	USB1_RXP	I		
A12 B12	GND	PWR		

Table 7: USB Host Interface (Type-A Connector)

4.3 Micro SD / Micro SIM card

To access a Micro SD and Micro SIM card there is a dual holder on the armStone.

The SD Card signals are shared with the Wifi module. If Wifi is mounted SD2 is not available.

Connector type: Molex: 1046421610

J9 Pin	Signal	CPU Pad	I/O	Voltage	Description
C1	UIM_VDD	Connected to J8 Pin 8		UIM_VDD	
C2	UIM_RST	Connected to J8 Pin 14		UIM_VDD	
C3	UIM_CLK	Connected to J8 Pin 12		UIM_VDD	
C4	GND				
C5	UIM_VPP	Connected to J8 Pin 16		UIM_VDD	
C6	UIM_I/O	Connected to J8 Pin 10		UIM_VDD	
T1	SD2_DATA2				*
T2	SD2_DATA3				*
T3	SD2_CMD				* 10k Pull-Up
T4	VDD_SD2			1.8V / 3.3V	* Enabled if SD is insert; Can be changed by SD2_VSELECT
T5	SD2_CLK				*
T6	GND				
T7	SD2_DATA0				*
T8	SD2_DATA1				*
SW	SD2_CDn				Inverted with MOSFET; 10k Pull-Up

Table 8: SD Card Interface A

* not available if Wifi is mounted

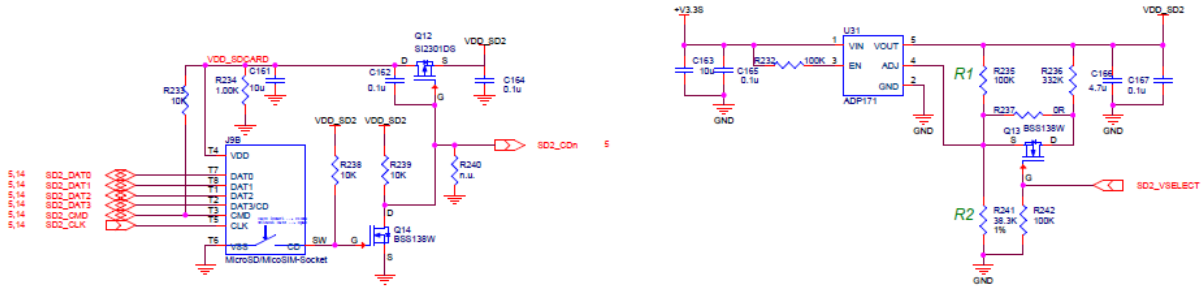


Figure 4: SDHC full feature example

4.4 Feature Connector

The SBC supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

J14 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	VCC3.3	-	PWR		
2	VCC5	-	PWR		
3	XGPIO0 / COL0	SAI1_MCLK		3.3V	4.7k Ω Pull Up
4	XGPIO1 / COL1	SAI1_TXD3 / ECSPI1_SCLK		3.3V	4.7k Ω Pull Up
5	XGPIO2 / COL2	SAI1_TXFS		3.3V	4.7k Ω Pull Up
6	XGPIO3 / COL3	SAI1_TXD4 / ECSPI1_SS0		3.3V	4.7k Ω Pull Up
7	XGPIO4 / COL4	SAI1_TXC		3.3V	4.7k Ω Pull Up
8	XGPIO5 / COL5	SAI1_TXD5 / ECSPI1_MOSI		3.3V	4.7k Ω Pull Up
9	XGPIO6 / COL6	SAI1_TXD0		3.3V	4.7k Ω Pull Up
10	XGPIO7 / COL7	SAI1_TXD6 / ECSPI1_MISO		3.3V	4.7k Ω Pull Up
11	GND	-	PWR		
12	XGPIO8 / I2C4_DAT	I2C4_SDA		3.3V	4.7k Ω Pull Up
13	XGPIO9 / TXD3	UART3_TXD / SAI1_RXD6		3.3V	- / 4.7k Ω Pull Up for SAI1_RXD6
14	XGPIO10 / I2C4_SCL	I2C4_SCL		3.3V	4.7k Ω Pull Up
15	XGPIO11 / RXD3	UART3_RXD / SAI1_RXD7		3.3V	100k Ω Pull Up / 4.7k Ω Pull Up for SAI1_RXD7
16	XGPIO12 / I2CLK / I2C4_IRQ	SAI3_RXC / ECSPI2_MISO*		3.3V	4.7k Ω Pull Up for SAI3_RXC
17	XGPIO13 / I2C4_RST / CTS4	SAI3_RXD / ECSPI2_SS0*		3.3V	4.7k Ω Pull Up for SAI3_RXD
18	XGPIO14 / ROW0 / TXD1	UART1_TXD		3.3V	
19	XGPIO15 / ROW1	SAI1_TXD2		3.3V	4.7k Ω Pull Up
20	XGPIO16 / ROW2 / RXD1	UART1_RXD		3.3V	100k Ω Pull Up
21	XGPIO17 / ROW3	SAI1_RXFS		3.3V	4.7k Ω Pull Up
22	XGPIO18 / ROW4	SAI1_RXC		3.3V	4.7k Ω Pull Up
23	XGPIO19 / ROW5	SAI1_RXD0		3.3V	4.7k Ω Pull Up

24	XGPIO29 / ROW6	SAI1_RXD1		3.3V	4.7k Ω Pull Up
25	XGPIO21 / ROW7	SAI1_RXD2		3.3V	4.7k Ω Pull Up
26	GPIO1	SAI1_TXD1		3.3V	4.7k Ω Pull Up
27	GND	-	PWR		
28	XGPIO22 / PWMOUT0	SPDIF_EXT_CLK		3.3V	4.7k Ω Pull Up
29	XGPIO23 / I2C3_SDA / ADC_IN0	- / I2C3_SDA		3.3V	ADC from ADS1015 / 4.7k Ω Pull Up for I2C3_SDA
30	XGPIO24 / PWMOUT1	SPDIF_RX		3.3V	4.7k Ω Pull Up
31	XGPIO25 / I2C3_SCL / ADC_IN1	- / I2C3_SCL		3.3V	ADC from ADS1015 / 4.7k Ω Pull Up for I2C3_SCL
32	XGPIO26 / PWMOUT2	SPDIF_TX		3.3V	4.7k Ω Pull Up
33	XGPIO27 / I2C3_IRQ / ADC_IN2	- / SAI3_TXD		3.3V	ADC from ADS1015/ 4.7k Ω Pull Up for SAI3_TXD
34	Backlight On	SAI1_RXD5		3.3V	4.7k Ω Pull Down
35	XGPIO28 / I2C3_RST / ADC_IN3	- / SAI3_RXFS		3.3V	ADC from ADS1015/ 4.7k Ω Pull Up for SAI3_RXFS
36	XGPIO29 / RXD4	ECSPI2_SCLK*		3.3V	100k Ω Pull Up
37	GND	-	PWR		
38	XGPIO30 / TXD4	ECSPI2_MOSI*		3.3V	
39	VCC3.3	-	PWR		
40	VCC5	-	PWR		
41	MIC1 (Audio pin 1)	-			From SGTL5000
42	GND	-	PWR		
43	Not connected	-	-		
44	LINEIN_R	-			From SGTL5000
45	LINEOUT_R	-			From SGTL5000
46	GND	-	PWR		
47	GND	-	PWR		

48	LINEIN_L	-			From SGTL5000
49	LINEOUT_L	-			From SGTL5000
50	GND	-	PWR		
51	RESETBTN	-			Leave open if not used
52	VCC3.3	-	PWR		
53	PWRBTN	ONOFF			Leave open if not used
54	Not connected	-	-		
55	RXD2 (RS232)	-			From UART2_RXD via SP3243
56	RTS2 (RS232)	-			From UART4_RXD via SP3243
57	TXD2 (RS232)	-			From UART2_TXD via SP3243
58	CTS2 (RS232)	-			From UART4_TXD via SP3243
59	Not connected	-	-		
60	Not connected	-	-		
61	GND	-	PWR		
62	VCC5 (COM keypin)	-	PWR		
63	CAN1RX / CAN1L	-			From MCP2515 optional with CAN transceiver
64	CAN1TX / CAN1H	-			From MCP2515 optional with CAN transceiver
65	BOOTSEL	-			
66	BOOTSEL	-			

Table 9: Feature Connector

*Only Available if WLAN is not mounted

4.5 Ethernet Interface

The board supports one 10/100/1000 Mbit LAN interfaces. A 10/100/1000 Gigabit PHY Qualcomm AR8035 is mounted on the board.

J3 Pin	Signal	Function	I/O	Voltage	Description
1	GND via 100nF				
2	ETH_A_D1_P		I/O		Gbit Differential data line
3	ETH_A_D1_N		I/O		
4	ETH_A_D2_P		I/O		Gbit Differential data line
5	ETH_A_D2_N		I/O		
6	ETH_A_D3_P		I/O		Gbit Differential data line
7	ETH_A_D3_N		I/O		
8	ETH_A_D4_P		I/O		Gbit Differential data line
9	ETH_A_D4_N		I/O		
10	GND		PWR		
11	3.3V via 300Ω		PWR		
12	LINKLED10_100 & LINKLED_1000		O		Link LED
13	3.3V via 300Ω		PWR		
14	ACTLED		O		Activity LED

Table 10 Ethernet Interface

4.6 PCIE Interface

The board supports one channel PCI Express.

J8 Pin	Signal	I/O	Voltage	Description
1	mPCIE_WAKE	O		
2	3.3V	PWR		
3	Not connected			
4	GND	PWR		
5	Not connected			
6	1.5V	PWR		
7	mPCIE_CLKREQ	O		
8	UIM_PWR	PWR		Connected to J8
9	GND	PWR		
10	UIM_DATA	I/O		Connected to J8
11	mPCIE_CLK_N	I/O		
12	UIM_CLK	O		Connected to J8
13	mPCIE_CLK_P	I/O		
14	UIM_RESET	O		Connected to J8
15	GND	PWR		
16	UIM_VPP	PWR		Connected to J8
17	Not connected			
18	GND	PWR		
19	Not connected			
20	mPCIE_DIS	O		
21	GND	PWR		
22	mPCIE_PERST	O		
23	mPCIE_CRX_N	O		
24	3.3V	PWR		
25	mPCIE_CRX_P	O		
26	GND	PWR		
27	GND	PWR		
28	1.5V	PWR		
29	GND	PWR		
30	I2C_SCL	O		Connected to I2C1_SCL
31	mPCIE_CTX_N	I		
32	I2C_SDA	I/O		Connected to I2C1_SDA
33	mPCIE_CTX_P	I		
34	GND	PWR		
35	GND	PWR		
36	USB_D-	I/O		USB4 from USB Hub
37	GND	PWR		
38	USB_D+	I/O		USB4 from USB Hub
39	3.3V	PWR		

40	GND	PWR		
41	3.3V	PWR		
42	LED D10			Connected to cathode of D10
43	GND	PWR		
44	LED D12			Connected to cathode of D12
45	Not connected			
46	LED D11			Connected to cathode of D11
47	Not connected			
48	1.5V	PWR		
49	Not connected			
50	GND	PWR		
51	Not connected			
52	3.3V	PWR		

Table 11: PCIE Interface

4.7 HDMI Interface

The SBC provides an HDMI / DVI interface with up to 4k resolution. All signals are ESD and EMI protected.

J2 Pin	Signal	I/O	Voltage	Description
1	HDMI_D2+	I/O		
2	GND	PWR		
3	HDMI_D2-	I/O		
4	HDMI_D1+	I/O		
5	GND	PWR		
6	HDMI_D1-	I/O		
7	HDMI_D0+	I/O		
8	GND	PWR		
9	HDMI_D0-	I/O		
10	HDMI_CLK+	I/O		
11	GND	PWR		
12	HDMI_CLK-	I/O		
13	HDMI_CEC	I	5.0V	
14	Not connected			
15	HDMI_I2C_CLK	O	5.0V	
16	HDMI_I2C_DATA	I/O	5.0V	
17	GND	PWR		
18	5.0V	PWR		
19	Hot Plug Detection	I	5.0V	

Table 12: HDMI Interface

4.8 LVDS Interface

The SBC provides two LVDS interfaces with 4 lanes each and a maximum resolution of 1920 x 1200. The LVDS signals are generated by a DSI to LVDS Bridge.

Connector type: ES&S STE-FI-X30S-HF-NPB-TW

J10 Pin	Signal	I/O	Voltage	Description
1	LVDS_A_D0-	O		
2	LVDS_A_D0+	O		
3	LVDS_A_D1-	O		
4	LVDS_A_D1+	O		
5	LVDS_A_D2-	O		
6	LVDS_A_D2+	O		
7	GND	PWR		
8	LVDS_A_CLK-	O		
9	LVDS_A_CLK+	O		
10	LVDS_A_D3-	O		
11	LVDS_A_D3-	O		
12	LVDS_B_D0-	O		
13	LVDS_B_D0+	O		
14	GND	PWR		
15	LVDS_B_D1-	O		
16	LVDS_B_D1+	O		
17	GND	PWR		
18	LVDS_B_D2-	O		
19	LVDS_B_D2+	O		
20	LVDS_B_CLK-	O		
21	LVDS_B_CLK+	O		
22	LVDS_B_D3-	O		
23	LVDS_B_D3+	O		
24	GND	PWR		
25	I2C_SDA	I/O	3,3V	Connect to I2C2_SDA with 4.7k Ω Pull Up
26	I2C_IRQ / VLCDON	I / O	3,3V	Connect to SAI3_MCLK
27	I2C_SCL	O	3,3V	Connect to I2C2_SCL with 4.7k Ω Pull Up
28	VLCD	PWR		3,3V or 5V Output switched by VLCDON
29	VLCD	PWR		
30	VLCD	PWR		

Table 13: LVDS Interface

4.9 Touch Interface

To connect a capacitive Touchpanel via I²C, the SBC offers the I²C Signals on a 6-pin connector.

Connector type: Hirose DF13-6P-1.25H

J13 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	3.3V		PWR		Maximal 50mA Output
2	I2C_SDA	I2C2_SDA	I/O	3.3V	4.7k Ω Pull Up
3	I2C_SCL	I2C2_SCL	O	3.3V	4.7k Ω Pull Up
4	I2C_RST	SAI3_TXC	O	3.3V	4.7k Ω Pull Up
5	I2C_IRQ	SAI3_XTFS	I	3.3V	4.7k Ω Pull Up
6	GND		PWR		

Table 14: Touch Interface

4.10 Backlight Interface

To control the LCD voltage and Backlight, the SBC offers a 4-pin connector with the control pins.

Connector type: Hirose DF13-4P-1.25H

J11 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	VLCD_ON	SAI5_RXD2	O	3.3V	Display on/off 4.7k Ω Pull Down
2	BL_ON	SAI1_RXD5	O	3.3V	Backlight on/off 4.7k Ω Pull Down
3	BL_PWM	SAI5_RXD1	O	3.3V	Backlight Brightness
4	GND		PWR		

Table 15: Backlight Interface

4.10.1 Solution with a single cable with 3 connectors

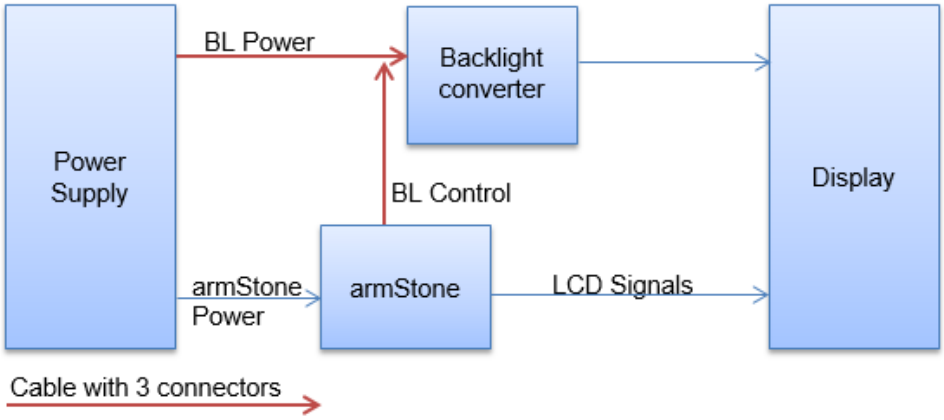


Figure 4: backlight connection with single cable

4.10.2 Solution with 2 cable with 2 connectors each

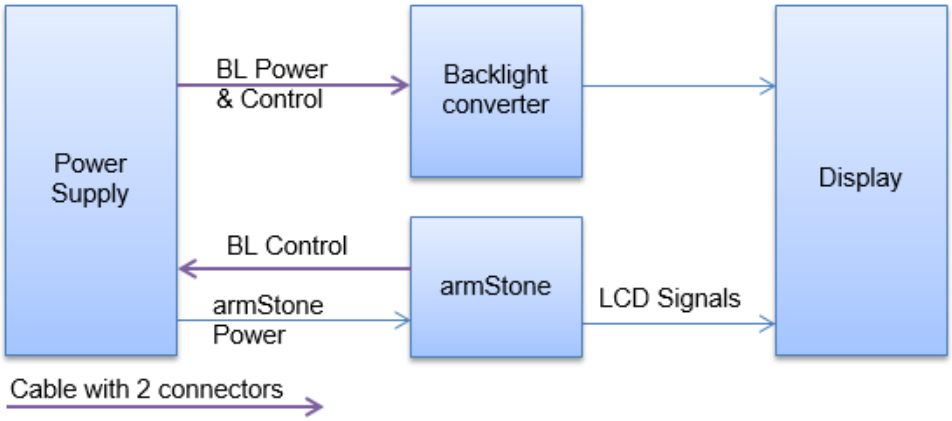


Figure 5: backlight connection with 2 cable

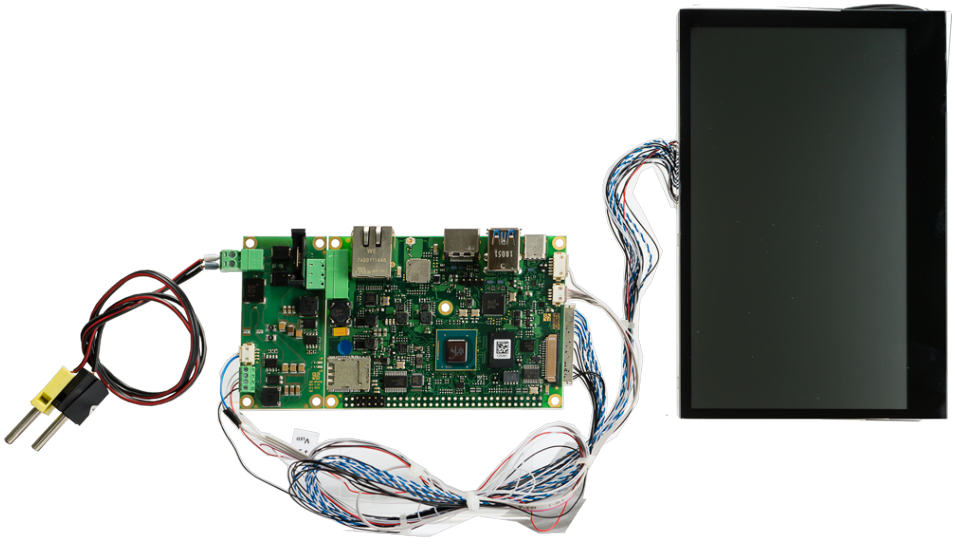


Figure 6: backlight connection with 2 cable

4.11 MIPI CSI Interface

The board supports dual lane MIPI CSI interface.

J4 Pin	Signal	I/O	Voltage	Description
1	GND	PWR		
2	CSI_DATA0_N	I		
3	CSI_DATA0_P	I		
4	GND	PWR		
5	CSI_DATA1_N	I		
6	CSI_DATA1_P	I		
7	GND	PWR		
8	CSI_CLK_N	I		
9	CSI_CLK_P	I		
10	GND	PWR		
11	CAM_PWDN	O	3.3V	Connect to Pad GPIO1_IO10
12	CAM_MCLK	O	3.3V	Generate via 24MHz Oszilator or CPU Pad GPIO1_IO01
13	I2C_SCL	O	3.3V	Connect to I2C1_SCL
14	I2C_SDA	I/O	3.3V	Connect to I2C1_SDA
15	3.3V	PWR		

Table 16: MIPI CSI Interface

4.12 WLAN and Bluetooth Interface (optional)

The armStone™MX8M contains a certified high performance WLAN and Bluetooth module.

The module is based on Cypress's BCM43353 chip.

The module offers:

- IEEE802.11 a/b/g/n/ac
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 4.2
- The module is certified for the following regions: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- BT SIG QDID: 97564

Note: In case WLAN/BT module is mounted UART4 and the external SD card connector are not avilable

4.13 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

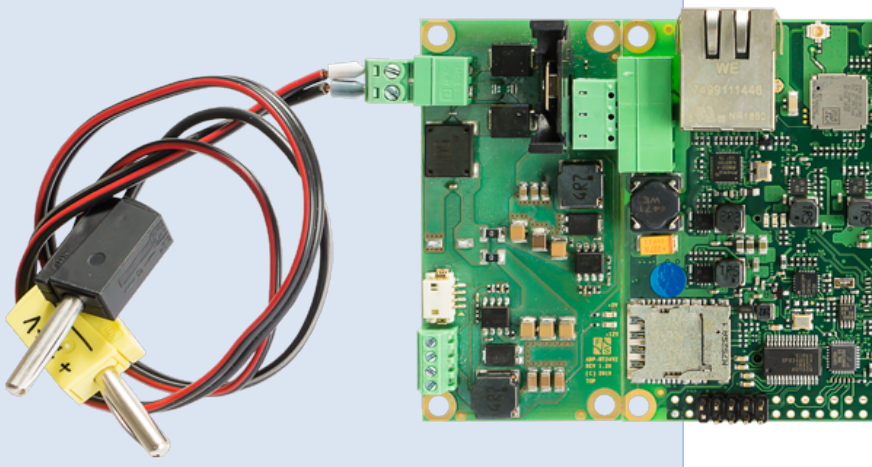
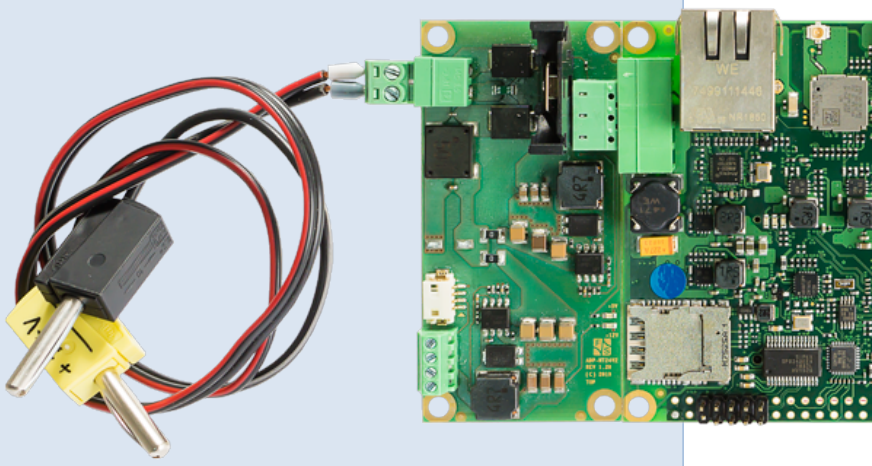
4.14 JTAG

J1 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	3.3V		PWR		
2	JTAG_TMS	JTAG_TMS		3,3V	10k Ω Pull Up
3	GND		PWR		
4	JTAG_TCK	JTAG_TCK		3,3V	10k Ω Pull Down
5	GND		PWR		
6	JTAG_TDO	JTAG_TDO		3,3V	
7	JTAG_nTRST	JTAG_TRST_B		3.3V	10k Ω Pull Up
8	JTAG_TDI	JTAG_TDI		3,3V	10k Ω Pull Up
9	GND		PWR		
10	JTAG_nSRST			3,3V	10k Ω Pull Up

Table 17: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.15 Power and Power Control Pins

J15 Pin	J16 Pin	Signal	I/O	Description
3	3, 4, 5, 6	VIN (+V5S)	I	Main Power supply input please refer chapter 7 ADP-NT24V2 To power the armStoneA9 with 7,5-36V F&S provide ADP-NT24V2:  The extension board is designed to plug it into the power Connector of the armStone. For more information check the F&S website: https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/ Electrical characteristic
4	7, 8, 9, 10	GND	I	Main Power supply Ground input
2	1, 2	VDD_VBAT	I	RTC battery input; tie to 3.0V please refer chapter 7 ADP-NT24V2 To power the armStoneA9 with 7,5-36V F&S provide ADP-NT24V2:  The extension board is designed to plug it into the power Connector of the armStone. For more information check the F&S website: https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/

5	-	3.3V	O	20mA output from on board DCDC powered from VIN

Table 18: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

3.3V is the 3.3V power supply of the board generated form PMIC and powered from VIN. Use as enable for baseboard power regulators.

5 Flash

5.1 NAND Flash

By default, boot mode is configured for NAND boot.

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S or TFAT to be robust against power failures

5.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

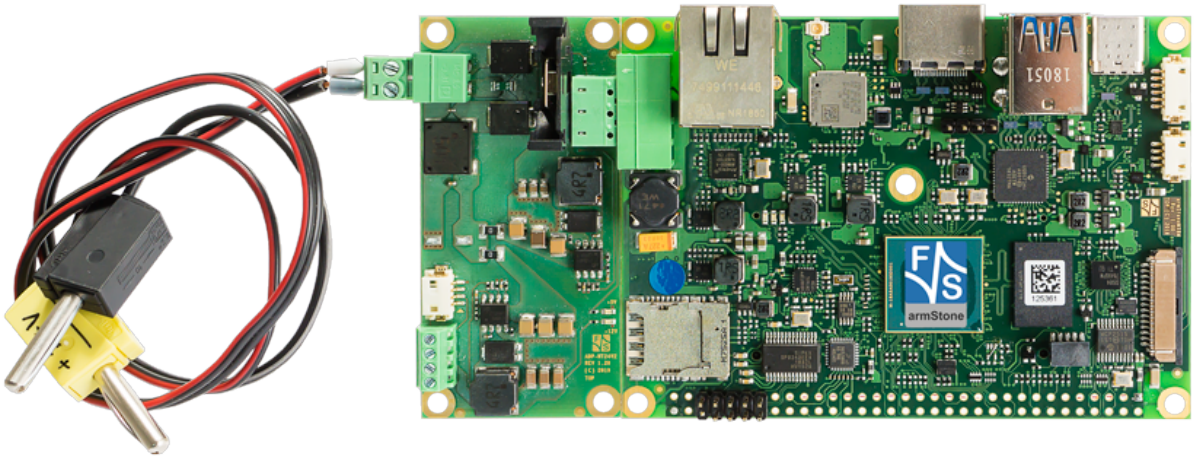
The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 RTC

There is a NXP PCA8565 or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 ADP-NT24V2

To power the armStoneA9 with 7,5-36V F&S provide ADP-NT24V2:



The extension board is designed to plug it into the power Connector of the armStone.

For more information check the F&S website:

https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 19: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VIN	Baord main power		4.5	5.5	V
VBAT	RTC power		1.8	3.5	V
OVDD	On board 3.3V DCDC		3.15	3.45	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V

V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VBAT			0.22	µA

Table 20: DC Electrical Characteristics

OVDD = power on pin 3.3V from on board DCDC

9 Thermal Specification

	Min	Typ	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MX8M	0		+95	°C
Junction temperature i.MX8M (“I”) [2]	-40		+105	°C

[1] Depending on cooling solution. See also: *Power consumption and cooling*

[2] Optional

10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMI implementing on COM

Like all other SBC's at the market there is no ESD protection on any signal out from the SBC. ESD protection hast to place as near as possible to the ESD source - this is every connector with external access. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the board supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the board.

The operating temperature can be measured on the mounting holes on top of the board and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d.** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d.** and **t.b.d.** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The boards are shipped in cartons. One carton can hold 30 boards.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 5: Matrix Code Sticker

18 Appendix

Important Notice

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