Hardware Documentation

PicoCore™MX7ULP
for HW Revision 1.20

Preliminary

Version 003
(2022-05-09)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCore™MX7ULP board with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
23.07.2018	001	All		*	Initial Version	KW
10.09.2019	001	All	M		Changed for Rev1.20	MW
08.06.2020	002	All	M	4.14	Correct information's for VDD_PTE	MW
29.07.2021	003	All	M	4.11	Updated information about network controller	JK

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block Diagram

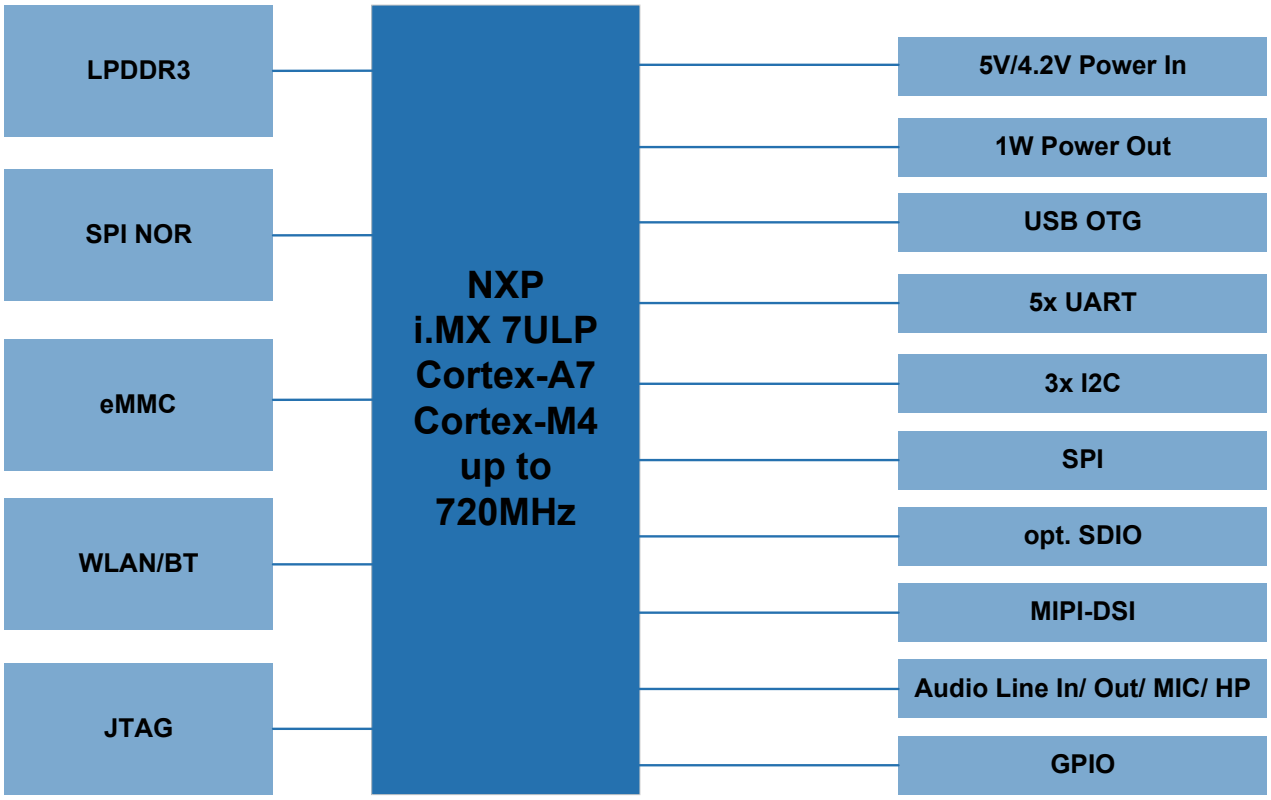

Figure 1: Block Diagram

2 Mechanical Dimension

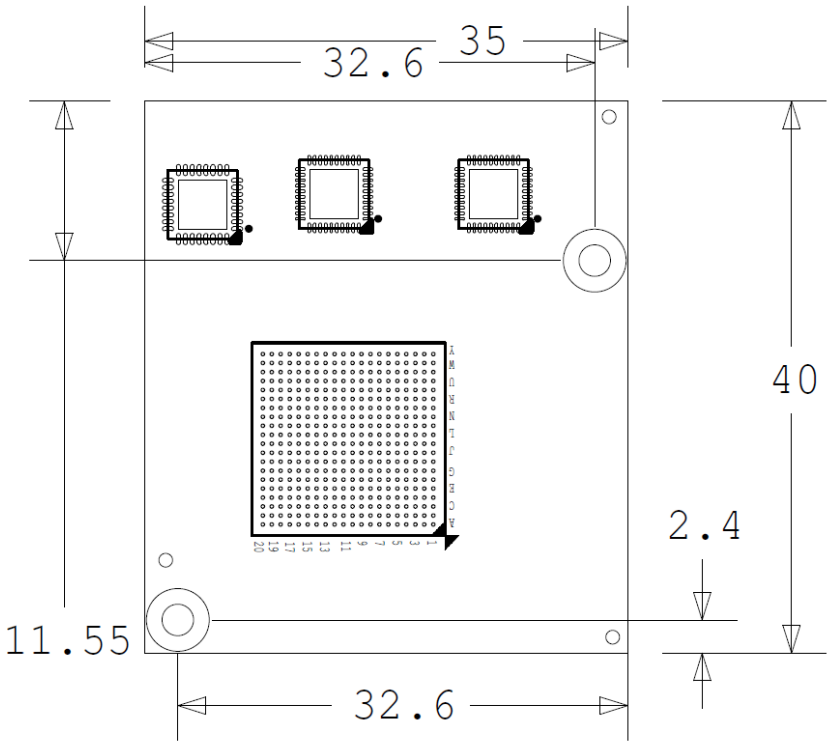

Figure 2: Mechanical Dimensions Top

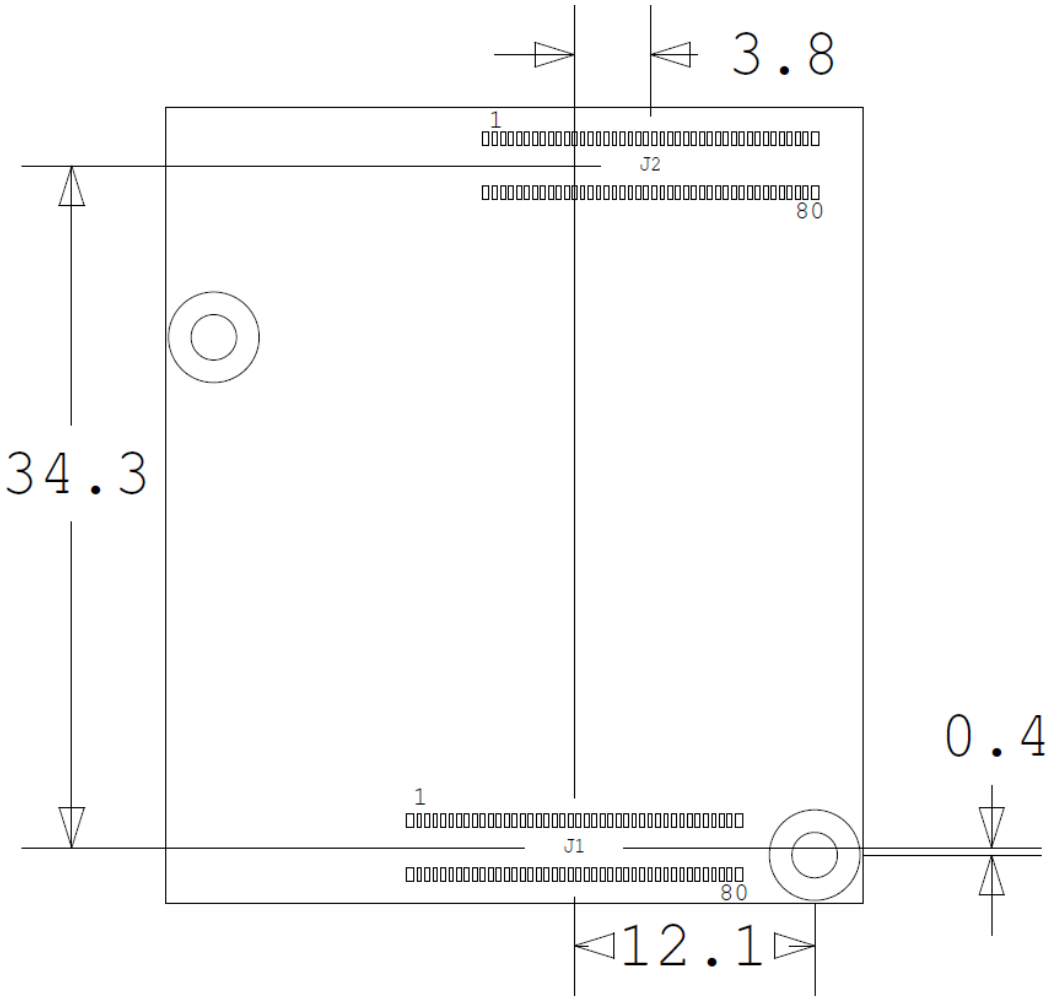

Figure 3: Mechanical Dimensions Bottom

Size:	40mm x 35mm
PCB thickness:	1.2 ± 0.1mm
Height of the parts on the top side:	max.5 mm (except JTAG connector not mounted on mass production)
Height of the parts on the bottom side:	max. 1.4 mm
Weight:	14g

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer from supplier “Würth Elektronik” order number “9774015243R”. You can also order via our web shop.

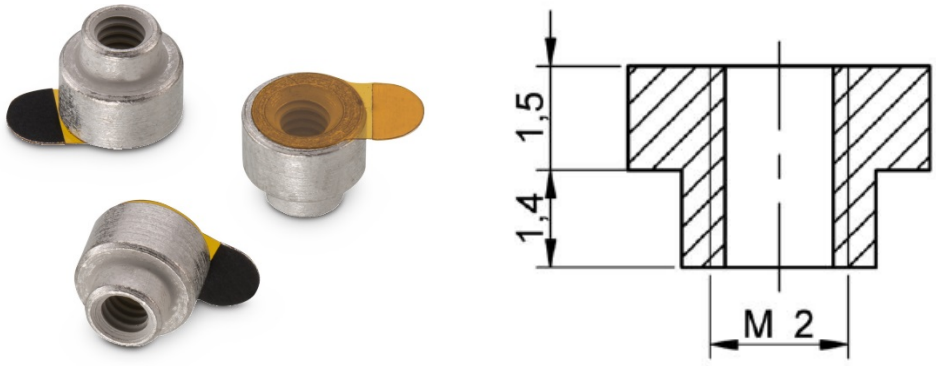

Figure 4: WE SMT Steel Spacer

Data sheet and 3D model (STP) is available on our web side.

3 Interface and Signal Description

3.1 B2B Connector J2 and J3

PicoCoreMX7ULP is using two 80 pin connectors from manufacturer Hirose.
Part number: DF40C-80DP-0.4V (51)
Part number counterpart: DF40C-80DS-0.4V (51)
With this combination, you get minimal stacking height of 1,5mm. Other possible stacking heights by using different counterpart connector are: 2mm, 3mm, 3,5mm and 4mm.
The connector with 1,5mm stacking height is can be ordered via F&S web shop.

J2						
Pin	**Signal**	**CPU Pad**	**I/O**	**Voltage**	**Remarks; onboard pullups**	**Core**
1	GND					
3	JTAG_TRST	PTA30	O	PMC_3V3		M4
5	JTAG_TDO	PTA27	O	PMC_3V3		M4
7	JTAG_TCLK	PTA29	O	PMC_3V3		M4
9	JTAG_TDI	PTA28	I	PMC_3V3		M4
11	JTAG_TMS	PTA26	O	PMC_3V3		M4
13	GND					
15	LPUART0_TX	PTA18	O	PMC_3V3	Predefined as M4 debug	M4
17	LPUART0_RX	PTA19	I	PMC_3V3	Predefined as M4 debug	M4
19	LPUART4_TX	PTC2	O	VDD_1V8	Predefined as A7 debug	A7
21	LPUART4_RX	PTC3	I	VDD_1V8	Predefined as A7 debug	A7
23	GND					
25	PTF0	PTF0	I	PMC_3V3	Predefined as touch controller interrupt input	A7
27	PTC19	PTC19	O	VDD_1V8	Predefined as MIPI_RESET	A7
29	PTF2	PTF2	O	PMC_3V3	Predefined as LED_PWM_EN	A7
31	LPUART6_CTS	PTE8	I	VDD_PTE		A7
33	LPUART6_RTS	PTE9	O	VDD_PTE		A7
35	LPUART6_TX	PTE10	O	VDD_PTE		A7
37	LPUART6_RX	PTE11	I	VDD_PTE		A7
39	PTE12	PTE12	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
41	PTE13	PTE13	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
43	GND					
45	LPUART5_TX	PTC6	O	VDD_1V8		A7
47	LPUART5_RX	PTC7	I	VDD_1V8		A7
49	LPI2C3_SCL	PTB12	O	PMC_1V8		M4
51	LPI2C3_SDA	PTB13	I/O	PMC_1V8		M4
53	GND					
55	VBAT_RTC		I		N.A.*2 revision <= 1.20	
57	LPI2C5_SCL	PTC4	O	VDD_1V8		A7
59	LPI2C5_SDA	PTC5	I/O	VDD_1V8		A7
61	GND					
63	LPI2C0_SCL	PTA16	O	PMC_3V3		M4
65	LPI2C0_SDA	PTA17	I/O	PMC_3V3		M4
67	GND					
69	DAC0_OUT		O			

71	DAC1_OUT		O			
73	GND					
75	Headphone Left		O			
77	Headphone Right		O			
79	Headphone GND		O			
2	GND					
4	SD1_DATA3	PTE4	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
6	SD1_DATA2	PTE5	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
8	SD1_DATA1	PTE0	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
10	SD1_DATA0	PTE1	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
12	SD1_CLK	PTE2	O	VDD_PTE	N.A.*1 if WLAN mounted	A7
14	SD1_CMD	PTE3	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
16	PTE6	PTE6	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
18	PTE7	PTE7	I/O	VDD_PTE	N.A.*1 if WLAN mounted	A7
20	PTF1	PTF1	I/O	PMC_3V3		A7
22	GND					
24	DSI_DATA0_P					
26	DSI_DATA0_N					
28	GND					
30	DSI_CLK_P					
32	DSI_CLK_N					
34	GND					
36	DSI_DATA1_P					
38	DSI_DATA1_N					
40	GND					
42	LPUART2_TX	PTA10	O	PMC_3V3		M4
44	LPUART2_RX	PTA11	I	PMC_3V3		M4
46	LPUART2_RTS	PTA9	O	PMC_3V3		M4
48	LPUART2_CTS	PTA8	I	PMC_3V3		M4
50	GND					
52	PTB9	PTB9	I/O	PMC_1V8		M4
54	LPUART7_TX	PTF14	O	PMC_3V3		A7
56	LPUART7_RX	PTF15	I	PMC_3V3		A7
58	LPI2C7_SDA	PTF13	O	PMC_3V3		A7
60	LPI2C7_SCL	PTF12	I/O	PMC_3V3		A7
62	GND					
64	BOOTSEL		I		Production service only	
66	AGND_AUD					
68	LineOut Left		O			
70	LineOut Right		O			
72	AGND_AUD					
74	LineIn Left		I			
76	LineIn Right		I			
78	AGND_AUD					
80	Mic		I			

J3						
Pin	**CPU signal**		**I/O**	**Voltage**	**Remarks; onboard pullups**	**Core**
1	GND					
3	GND					
5	GND					
7	ONOFF		I			
9	RESET1		O			
11	RESET0		O		This Signal is also driven by PMIC	
13	A7_POW_EN#	PTA25	O	PMC_3V3	A7 power on for power management	M4
15	M4_PER_EN	PTA21	O	PMC_3V3		M4
17	TAMPER		I			
19	GND					
21	GND					
23	VDD_PTE					
25	PMC_3V3					
27	GND					
29	PTA31	PTA31	I/O	PMC_3V3		M4
31	PTA23	PTA23	I/O	PMC_3V3		M4
33	PTA15	PTA15	I/O	PMC_3V3		M4
35	PTA14	PTA14	I/O	PMC_3V3		M4
37	PTA13	PTA13	I/O	PMC_3V3		M4
39	PTA12	PTA12	I/O	PMC_3V3		M4
41	PTA3	PTA3	I/O	PMC_3V3		M4
43	PTA1	PTA1	I/O	PMC_3V3		M4
45	PTA0	PTA0	I/O	PMC_3V3		M4
47	PTB1	PTB1	I/O	PMC_1V8		M4
49	PTB2	PTB2	I/O	PMC_1V8		M4
51	PTB3	PTB3	I/O	PMC_1V8		M4
53	PTB10	PTB10	I/O	PMC_1V8		M4
55	PTB11	PTB11	I/O	PMC_1V8		M4
57	PTB14	PTB14	I/O	PMC_1V8		M4
59	GND					
61	LPSPI3_PCS0	PTF19	O	PMC_3V3		A7
63	LPSPI3_SCK	PTF18	O	PMC_3V3		A7
65	LPSPI3_SOUT	PTF17	O	PMC_3V3		A7
67	LPSPI3_SIN	PTF16	I	PMC_3V3		A7
69	GND					
71	USB0_VBUS_DETECT		I			
73	GND					
75	USB0_DM					
77	USB0_DP					
79	GND					
2	VBAT_4V2					
4	VBAT_4V2					
6	VBAT_4V2					
8	GND					
10	RESETIN		I			

12	THM		I		PMIC	
14	BATT_ADC_IN	PTA20	I/O	PMC_3V3		M4
16	VDD_5V0					
18	VDD_5V0					
20	VDD_5V0					
22	VDD_5V0					
24	GND					
26	GND					
28	PTC9	PTC9	I/O	VDD_1V8		A7
30	PTC11	PTC11	I/O	VDD_1V8		A7
32	PTC12	PTC12	I/O	VDD_1V8		A7
34	PTC8	PTC8	I/O	VDD_1V8		A7
36	PTC14	PTC14	I/O	VDD_1V8		A7
38	PTC15	PTC15	I/O	VDD_1V8		A7
40	PTC16	PTC16	I/O	VDD_1V8		A7
42	PTC17	PTC17	I/O	VDD_1V8		A7
44	PTC18	PTC18	I/O	VDD_1V8		A7
46	GND					
48	PTF11	PTF11	I/O	PMC_3V3		A7
50	PTF10	PTF10	I/O	PMC_3V3		A7
52	PTF9	PTF9	I/O	PMC_3V3		A7
54	PTF8	PTF8	I/O	PMC_3V3		A7
56	PTF7	PTF7	I/O	PMC_3V3		A7
58	PTF6	PTF6	I/O	PMC_3V3		A7
60	PTF5	PTF5	I/O	PMC_3V3		A7
62	PTF4	PTF4	I/O	PMC_3V3		A7
64	PTF3	PTF3	I/O	PMC_3V3		A7
66	GND					
68	HSIC_DATA			VDD_1V2		
70	HSIC_STROBE			VDD_1V2		
72	GND					
74	GND					
76	USB_OTG_PWR_EN	PTE15	I/O	VDD_1V8	P	A7
78	USB_OTG_ID	PTC13	I/O	VDD_1V8		A7
80	GND					

*1 Do not connect this pin in case WLAN/BT module is mounted.

*2 Only available in Revision 1.30 or higher. Leave open in Revision 1.20 or lower.

O 4mA logic output

4 Interfaces

4.1 USB OTG

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

J3				
71	USB0_VBUS_DETECT	I	VBUS_5V	USB Phy voltage supply
76	USB_OTG_PWR_EN	O	VDD_1V8	Power enable
78	USB_OTG_ID	I	VDD_1V8	USB OTG ID signal
75	USB0_DM	I/O		90 Ohm differential pair
77	USB0_DP	I/O		

Table 1: USB OTG Interface

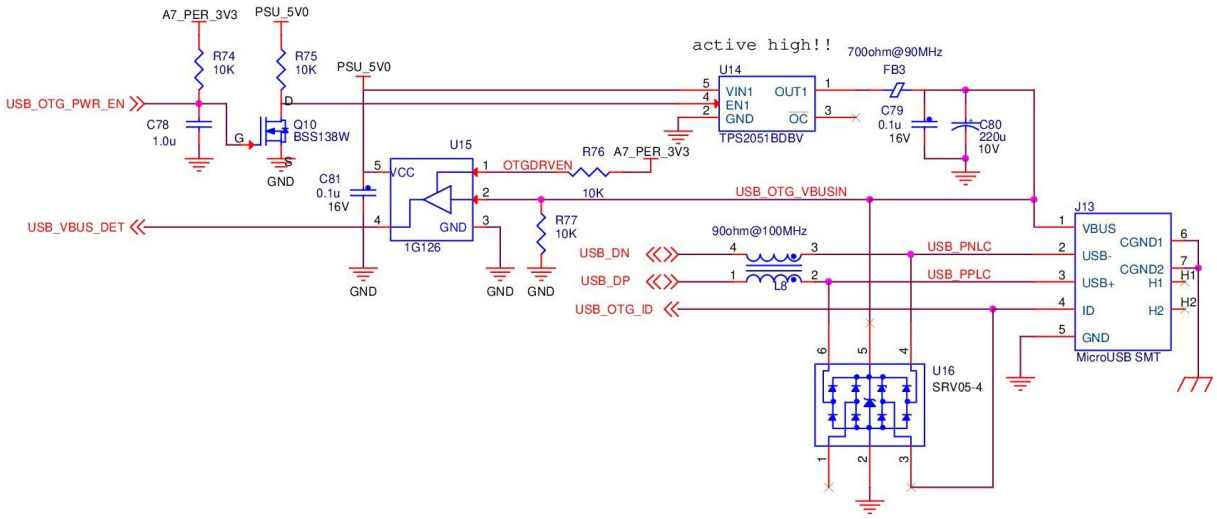

Figure 5: Figure 4: Full Feature USB OTG Port

4.2 SD Card

The interface is supporting a SD card channel**, if the WLAN module is not mounted**. For specification and licensing please refer the website of the SD Association: http://www.sdcard.org.

J2					
J3.23	VDD_PTE	O		3.3V/ 1.8V	Controlled by SW
37	SD1_nRST	O	PTE11	VDD_PTE	
39	SD1_WP	I	PTE12	VDD_PTE	Low active write protect disable
41	SD1_CD	I	PTE13	VDD_PTE	Low active card detect
4	SD1_D3	I/O	PTE4	VDD_PTE	
6	SD1_D2	I/O	PTE5	VDD_PTE	
8	SD1_D1	I/O	PTE0	VDD_PTE	
10	SD1_D0	I/O	PTE1	VDD_PTE	
12	SD1_CLK	O	PTE2	VDD_PTE	
14	SD1_CMD	I/O	PTE3	VDD_PTE	

Table 2: SD Card Interface

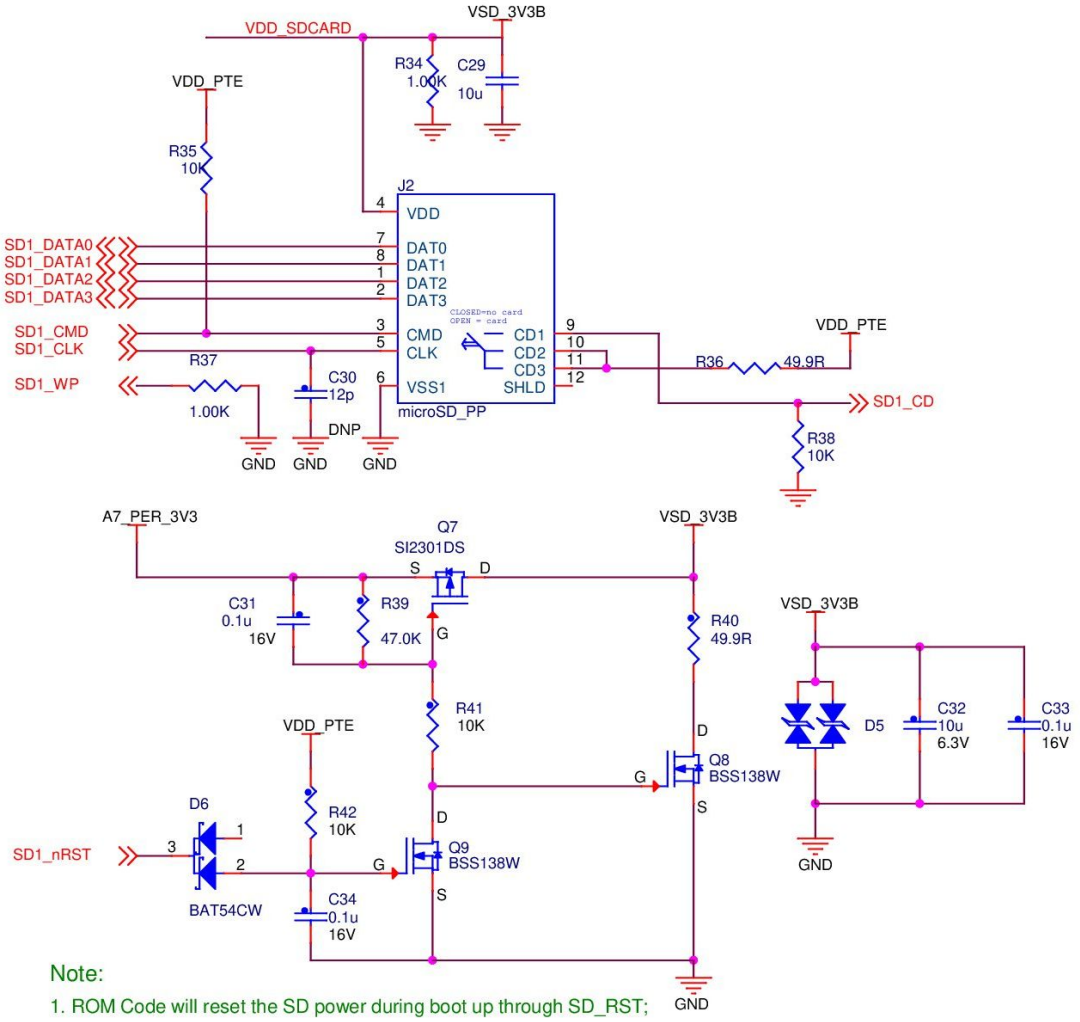

Figure 6: SDHC Full Feature Example

4.3 SPI Interface

The module support HS SPI (Serial Peripheral Interface) with 1 chip. All signals are 3.3V compliant. Devices on baseboard with other voltage need a level shifter.

Signals don't have pullups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

J2				
61	LPSPI3_PCS0	O	PTF19	PMC_3V3
63	LPSPI3_SCK	O	PTF18	PMC_3V3
65	LPSPI3_SOUT	O	PTF17	PMC_3V3
67	LPSPI3_SIN	I	PTF16	PMC_3V3

Table 3: SPI Interface

4.4 I2C Interface

The module supports a I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

J2					
49	LPI2C3_SCL	O	PTB12	PMC_1V8	4.7k PU on module
51	LPI2C3_SDA	I/O	PTB13	PMC_1V8	4.7k PU on module
57	LPI2C5_SCL	O	PTC4	VDD_1V8	4.7k PU on module
59	LPI2C5_SDA	I/O	PTC5	VDD_1V8	4.7k PU on module
63	LPI2C0_SCL	O	PTA16	PMC_3V3	4.7k PU on module, also used to program audio codec
65	LPI2C0_SDA	I/O	PTA17	PMC_3V3	4.7k PU on module, also used to program audio codec
58	LPI2C7_SCL	O	PTF12	PMC_3V3	4.7k PU on module
60	LPI2C7_SDA	I/O	PTF13	PMC_3V3	4.7k PU on module

Table 4: I2C Interfaces

4.5 Serial ports

J2					
15	LPUART0_TX	O	PTA18	PMC_3V3	Predefined as M4 debug
17	LPUART0_RX	I	PTA19	PMC_3V3	Predefined as M4 debug
19	LPUART4_TX	O	PTC2	VDD_1V8	Predefined as A7 debug
21	LPUART4_RX	I	PTC3	VDD_1V8	Predefined as A7 debug
31	LPUART6_CTS	I	PTE8	VDD_PTE	
33	LPUART6_RTS	O	PTE9	VDD_PTE	
35	LPUART6_TX	O	PTE10	VDD_PTE	
37	LPUART6_RX	I	PTE11	VDD_PTE	
45	LPUART5_TX	O	PTC6	VDD_1V8	
47	LPUART5_RX	I	PTC7	VDD_1V8	
54	LPUART7_TX	O	PTF14	PMC_3V3	
56	LPUART7_RX	I	PTF15	PMC_3V3	
42	LPUART2_TX	O	PTA10	PMC_3V3	
44	LPUART2_RX	I	PTA11	PMC_3V3	
46	LPUART2_RTS	O	PTA9	PMC_3V3	
48	LPUART2_CTS	I	PTA8	PMC_3V3	

Table 5: Serial UART Interfaces

We recommend use of UART0 and 4 for debugging and service only.

For UART6 voltage VDD_PTE is used.

Depends used voltage a different transceiver could be required.

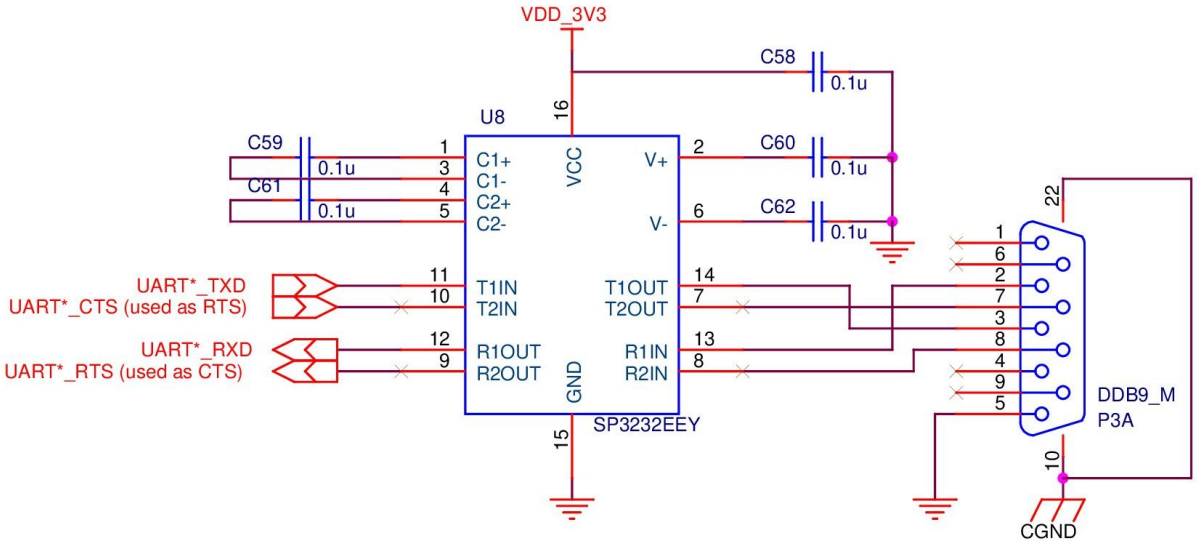

Figure 7: UART Transceiver Example

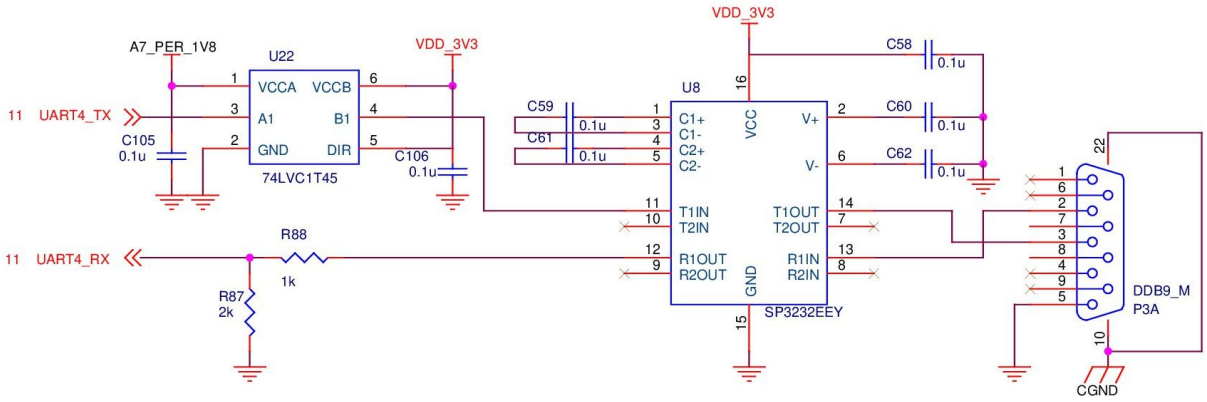

Figure 8: UART transceiver example for 1.8V TTL interface

4.6 GPIO

GPIOs (called PTA, PTB, PTC, PTE and PTF) are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up. On a non-powered board, it is not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

4.7 DAC

CPU includes a 12 bit DAC. Because space limitation it can't work noiseless.

For electrical details please refer the datasheet from NXP.

4.8 PWM

CPU includes 48 PWM (TPM) pins. To check all available Pins for TPM please check the IOMUX Table of NXP.

For electrical details please refer the datasheet from NXP.

4.9 Audio Interface

J2			
J2.66 **J2.72** **J2.78**	AGND_AUD	I	
J2.68	LineOut Left	O	
J2.70	LineOut Right	O	
J2.80	Mic	I	With BIAS
J2.74	LineIn Left	I	
J2.76	LineIn Right	I	
J2.75	Headphone Left	O	
J2.77	Headphone Right	O	
J2.79	Headphone GND	O	Never connect to GND

Table 6: Audio Interface

An NXP SGTL5000 audio codec is used on the module. If you need further details please refer the datasheet of audio codec.

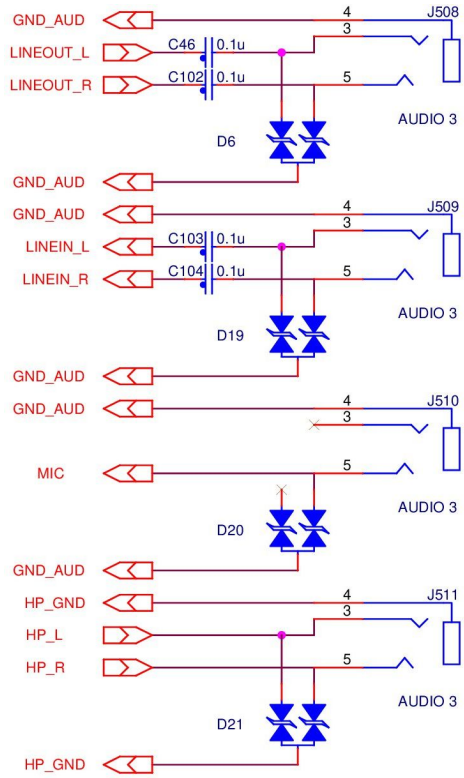

Figure 8 Audio In and Out

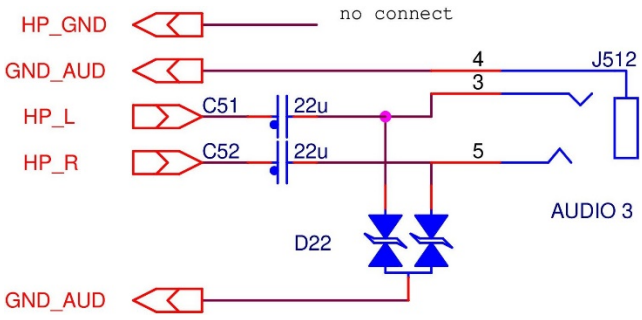

Figure 9: Cap-coupled version of headphone out with GND instead HP_GND

4.10 MIPI DSI Inteface

The module supports dual lane MIPI DSI interface up to 800 Mbps. The schematic of the carrier board shows an implementation of how to convert MIPI DSI to parallel RGB display.

J2	
J2.24	DSI_DATA0_P
J2.26	DSI_DATA0_N
J2.30	DSI_CLK_P
J2.32	DSI_CLK_N
J2.36	DSI_DATA1_P
J2.38	DSI_DATA1_N

Table 7: MIPI DSI Interface

4.11 WLAN and Bluetooth Interface (optional)

The PicoCore™MX7ULP contains a certified high performance WLAN and Bluetooth module. The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan (pre) certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0(supports low Energy).

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: In case WLAN/BT module is mounted external SD card interface is not available.

4.12 JTAG interface

Pin	Signal	CPU Pad	Comment
J2.3	JTAG_TRST	PTA30	JTAG debug port. Connecting with other JTAG devices not allowed!
J2.5	JTAG_TDO	PTA27	
J2.7	JTAG_TCLK	PTA29	
J2.9	JTAG_TDI	PTA28	
J2.11	JTAG_TMS	PTA26	

Table 8: JTAG Interface

For debug only. Leave unconnected, if you don't using JTAG. Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU.

Pins can be used as GPIO.

4.13 Bootselect

If the Software of the Module is crashed and you have to program the Module via USB and the MFG-Tool, you have to connect the BOOTSEL-Pin (J2, Pin 64) to Ground.

If you don't need this function leave the Pin open.

4.14 Power and Power Control Pins

J2/ J3				
J2.2,4,6	VBAT_4V2	I/O		Li cell input and charging output please refer chapter 6 Electrical characteristic
J2.16,18, 20,22	VDD_5V0	I		Main Power supply input please refer chapter 6 Electrical characteristic
J3.25	PMC_3V3	O		3.3V power rail out from PMIC, leave open if not used
J2.55	VBAT_RTC	I		RTC power input. Only available from Revision 1.30
J3.23	VDD_PTE	O		3.3V/ 1.8V SDIO power on module If WLAN is mounted: Fixed 1.8V If WLAN is **not** mounded: Switchable 1.8V / 3.3V
J3.7	ONOFF	I		leave open if not used
J3.9	RESET1	I	PMC_1V8	leave open if not used
J3.11	RESET0	I	PMC_3V3	leave open if not used
J3.13	A7_POW_EN#	O	PMC_3V3	A7 power on for power management to switch on the A7_PER_3V3 power regulator on module and baseboard For 1.8V use a 3.3V to 1.8V regulator, leave open if not used
J3.15	M4_PER_EN	O	PMC_3V3	M4 power on for power management to switch on the M4_PER_3V3 power regulator on baseboard For 1.8V use a 3.3V to 1.8V regulator, leave open if not used
J3.17	TAMPER	I	VBAT_1V8	leave open if not used
J3.10	RESETIN	I	VBAT_4V2	leave open if not used
J3.12	THM	I		Battery thermistor input, leave open if not used

Table 9: Power and Power Control Pins

5 Flash

5.1 QSPI NOR Flash

A 512Mb (64MB) QSPI NOR Flash is mounted on the board.

5.2 eMMC Flash

If mounted an eMMC v4.41 or higher with 4GB or more is mounted from different manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 Electrical characteristic

VBAT_4V2 (supply for Li pack version): 3.8V .. 4.25V

VDD_5V0 (supply for power supply): 4.1V .. 6.0V

Power consumption

Thermal design power (summary all chips)

t.b.d. (CPU values not available yet)

Power consumption of connected devices like display, USB devices, SD card has to be added for power calculation.

Real power consumption could be much lower depends CPU workload, used graphic interfaces and features and the workload on I/O interfaces.

6.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range IO pins	-0.3	VDD+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Output current on PMC_3V3		200	mA

Table 10: maximum ratings

6.2 DC electrical characteristics

Parameter	Description	Condition	Min	Max	Unit
VDD_5V0	Module main power		4.1	6.0	V
VBAT_4V2	Battery power		3.8	4.25	V
VBAT_RTC	RTC power*		2.91	3.21	
USB0_VBUS_DETECT	USB supply voltage		4.2	6.0	
PMC_3V3 VDD_1V8	PMIC on module 3.3V LDO PMIC on module 1.8V LDO		3.15 1.76	3.45 1.85	V
V_{ih}	High Level Input Voltage		0.7*VDD	VDD	V
V_{il}	Low Level Input Voltage		0	0.3*PMC_3V3	V
V_{oh}	High Level Output Voltage	I_{oh}=2.9mA	0.8*VDD		V
V_{ol}	Low Level Output Voltage	I_{ol}=2.9mA		0.2*VDD	V
I_o	Output current IOs			4	mA

Table 11: DC electrical characteristics

PMC_3V3 = power on pin PMC_3V3 from on module PMIC
*Only available from Revision 1.30

7 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

8 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

9 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

10 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be ***t.b.d.*** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. ***t.b.d.*** and ***t.b.d.*** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- CPU datasheet from NXP
- AN4579 from NXP
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

11 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

12 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

13 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 10 boards. An empty tray is used as top cover.

14 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number.
Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

15 Appendix

Important Notice

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