# Hardware Documentation

*PicoCore™MX6SX*
*for HW Revision 1.20*

# Preliminary

Version 002
(2019-10-31)

Elektronik Systeme


Untere Waldplätze 23
D-70569 Stuttgart
Fon: +49(0)711-123722-0
Fax: +49(0)711-123722-99

# About This Document

This document describes how to use the PicoCore™MX6SX board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

# ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

# History

| Date | V | Platform | A,M,R | Chapter | Description | Au |
|---|---|---|---|---|---|---|
| 18.07.2018 | 001 | All | | - | Initial Version | KW |
| 29.10.2019 | 002 | All | M | * | Updated revision | HF |
| 29.10.2019 | 002 | All | A | 2.1 | Description SMT Steel Spacer added | HF |
| 31.10.2019 | 002 | All | M | 3.1 | Inserted new B2B connector.<br>Schematic examples are still preliminary. | HF |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

| | |
|---|---|
| V | Version |
| A,M,R | Added, Modified, Removed |
| Au | Author |

# Table of Contents

# 1 Block diagram

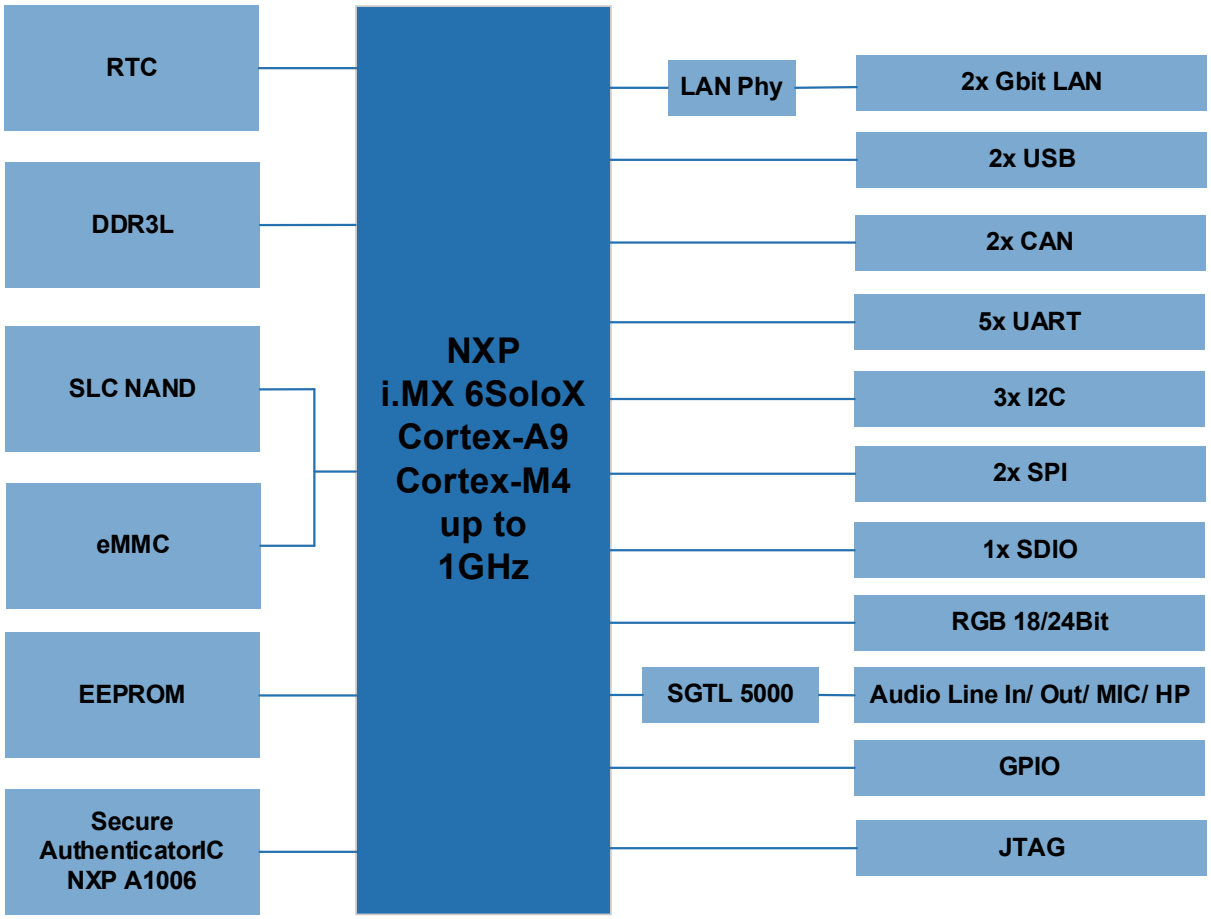


*Figure 1: Block Diagram*

# 2 Mechanical dimension

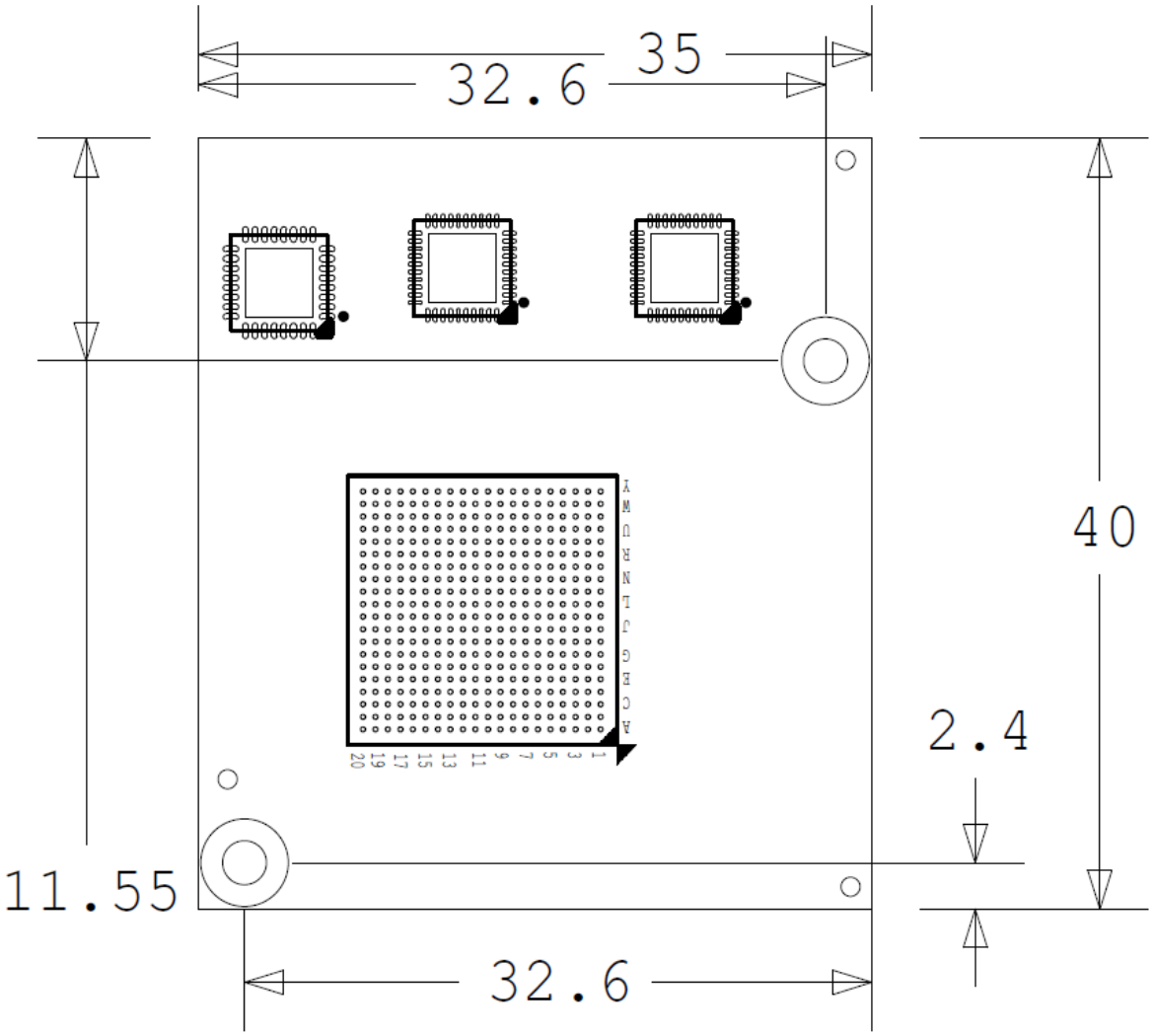


*Figure 2: Mechanical Dimensions Top*

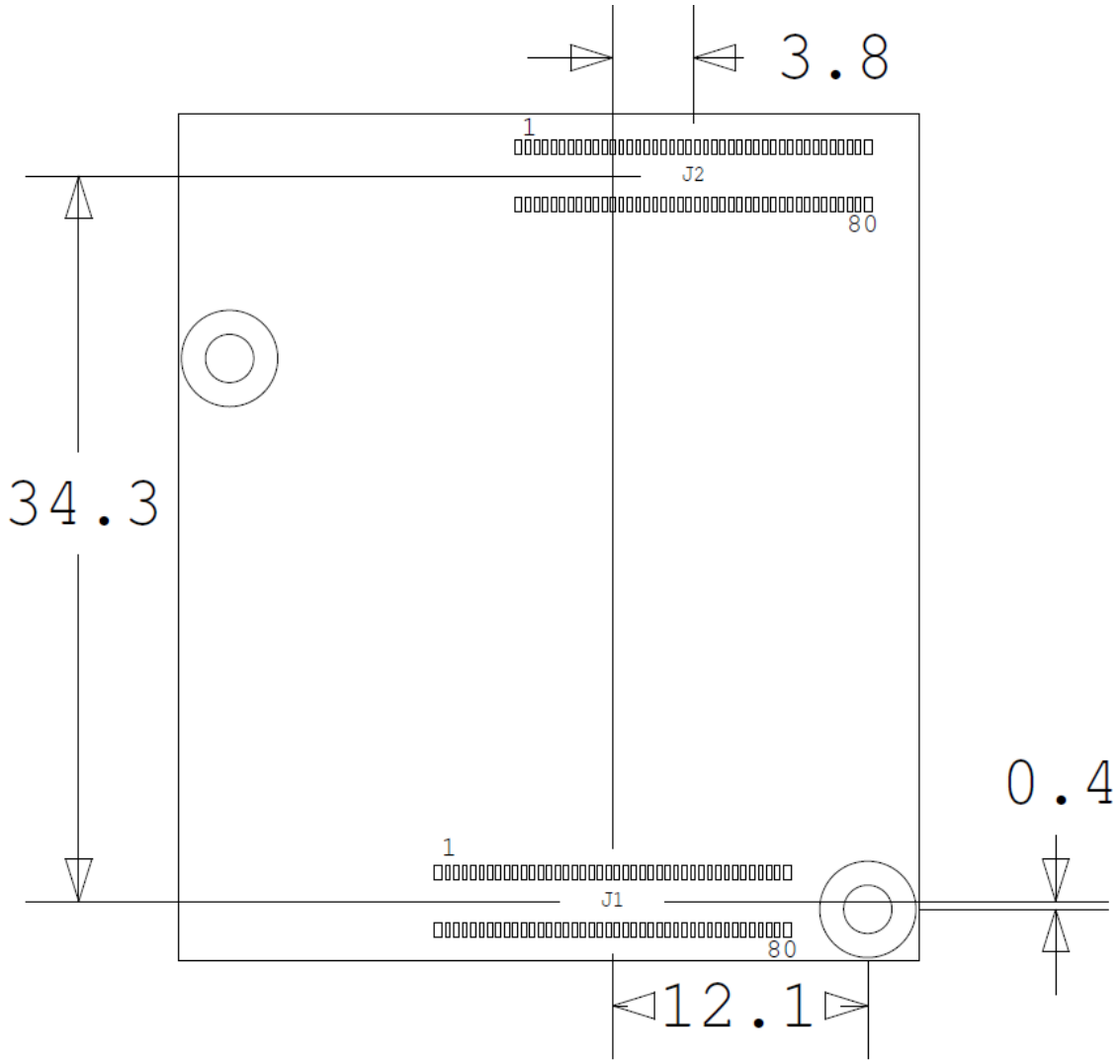


*Figure 3: Mechanical Dimensions Bottom*

| | |
|---|---|
| Size: | 40mm x 35mm |
| PCB thickness: | 1.2 ± 0.1mm |
| Height of the parts on the top side: | max.5 mm (except JTAG connector not mounted on mass production) |
| Height of the parts on the bottom side: | max. 1.4 mm |
| Weight: | 14g |

3D Step model available, please contact support@fs-net.de

## 2.1 SMT Steel Spacer

For mounting, we recommend SMT Steel Spacer from supplier “Würth Elektronik” order number “9774015243R”.

This part is in stock and can be ordered via F&S web shop.

Data sheet and 3D model (STP) is available on our web side.

If you use different stacking high, you have to change the Spacer.

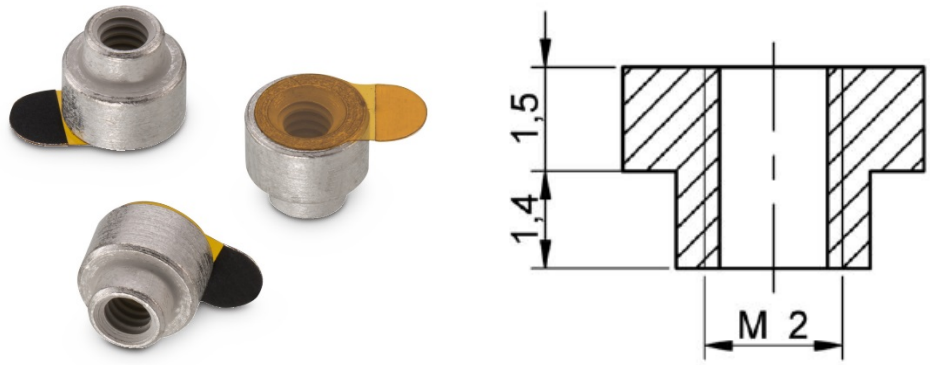


*Figure 4: SMT Steel Spacer*

# 3 Interface and signal description

## 3.1 B2B connectors

PicoCoreMX6SX is using two 80 pin connectors from manufacturer Hirose.
Part number: DF40C-80DP-0.4V
Part number counterpart: DF40C-80DS-0.4V
With this combination, you get minimal stacking height of 1,5mm. Other possible stacking heights by using different counterpart connector are: 2mm, 3mm, 3,5mm and 4mm.
The connector with 1,5mm stacking height is available at F&S and can be ordered via our web shop.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 1 | GPIO_J1_1 | SD4_DATA4 | | SD_A_VCC | |
| **J1** | 3 | GPIO_J1_3 | SD4_DATA6 | | SD_A_VCC | |
| **J1** | 5 | UART_B_RXD | QSPI1B_SCLK | | 3,3V | |
| **J1** | 7 | UART_B_TXD | QSPI1B_S | | 3,3V | |
| **J1** | 9 | UART_C_CTS | SD3_DATA2 | | 3,3V | Use as CTS from external side |
| **J1** | 11 | UART_C_RTS | SD3_CLK | | 3,3V | Use as RTS from external side |
| **J1** | 13 | UART_C_RXD | SD3_DATA3 | I | 3,3V | |
| **J1** | 15 | UART_C_TXD | SD3_CMD | O | 3,3V | |
| **J1** | 17 | UART_D_RXD | GPIO1_IO07 | I | 3,3V | |
| **J1** | 19 | UART_D_TXD | GPIO1_IO06 | O | 3,3V | |
| **J1** | 21 | I2C_A_SCL | SD3_DATA0 | I/O | 3,3V | Ext pull-up needed |
| **J1** | 23 | I2C_A_SDA | SD3_DATA1 | I/O | 3,3V | Ext pull-up needed |
| **J1** | 25 | GPIO_J1_25 | KEY_ROW4 | | 3,3V | |
| **J1** | 27 | GPIO_J1_27 | KEY_ROW3 | | 3,3V | |
| **J1** | 29 | GPIO_J1_29 | KEY_ROW0 | | 3,3V | |
| **J1** | 31 | GPIO_J1_31 | KEY_COL4 | | 3,3V | |
| **J1** | 33 | GPIO_J1_33 | KEY_COL3 | | 3,3V | |
| **J1** | 35 | GPIO_J1_35 | KEY_COL1 | | 3,3V | |
| **J1** | 37 | GPIO_J1_37 | KEY_COL0 | | 3,3V | |
| **J1** | 39 | I2C_B_IRQ | GPIO1_IO08 | | 3,3V | On board pull-up 100k to 3,3V |
| **J1** | 41 | I2C_B_SCL | GPIO1_IO02 | | 3,3V | Ext pull-up needed |
| **J1** | 43 | I2C_B_SDA | GPIO1_IO03 | | 3,3V | Ext pull-up needed |
| **J1** | 45 | GND | | | | |
| **J1** | 47 | LCD_R0 | LCD1_DATA16 | O | 3,3V | |
| **J1** | 49 | LCD_R1 | LCD1_DATA17 | O | 3.,3V | |
| **J1** | 51 | LCD_R2 | LCD1_DATA18 | O | 3.,3V | |
| **J1** | 53 | LCD_R3 | LCD1_DATA19 | O | 3.,3V | |
| **J1** | 55 | LCD_R4 | LCD1_DATA20 | O | 3.,3V | |
| **J1** | 57 | LCD_R5 | LCD1_DATA21 | O | 3.,3V | |
| **J1** | 59 | LCD_R6 | LCD1_DATA22 | O | 3.,3V | |
| **J1** | 61 | LCD_R7 | LCD1_DATA23 | O | 3.,3V | |

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 63 | GND | | | | |
| **J1** | 65 | LCD_G0 | LCD1_DATA08 | | 3.,3V | |
| **J1** | 67 | LCD_G1 | LCD1_DATA09 | | 3.,3V | |
| **J1** | 69 | LCD_G2 | LCD1_DATA10 | | 3.,3V | |
| **J1** | 71 | LCD_G3 | LCD1_DATA11 | | 3.,3V | |
| **J1** | 73 | LCD_G4 | LCD1_DATA12 | | 3.,3V | |
| **J1** | 75 | LCD_G5 | LCD1_DATA13 | | 3.,3V | |
| **J1** | 77 | LCD_G6 | LCD1_DATA14 | | 3.,3V | |
| **J1** | 79 | LCD_G7 | LCD1_DATA15 | | 3.,3V | |
| **J1** | 2 | GPIO_J1_2 | SD4_DATA5 | | SD_A_VCC | |
| **J1** | 4 | GPIO_J1_4 | SD4_DATA7 | | SD_A_VCC | |
| **J1** | 6 | UART_A_RXD | GPIO1_IO05 | | | On board pull-up 100k to 3,3V |
| **J1** | 8 | UART_A_TXD | GPIO1_IO04 | | | |
| **J1** | 10 | CAN_A_RX | SD3_DATA7 | I | 3,3V | |
| **J1** | 12 | CAN_A_TX | SD3_DATA5 | O | 3,3V | |
| **J1** | 14 | SPI_A_SS0 | QSPI1B_DQS | O | 3,3V | |
| **J1** | 16 | SPI_A_MISO | QSPI1A_S | I | 3,3V | |
| **J1** | 18 | SPI_A_MOSI | QSPI1A_DQS | O | 3,3V | |
| **J1** | 20 | SPI_A_SCLK | QSPI1B_S | O | 3,3V | |
| **J1** | 22 | GPIO_J1_22 | QSPI1B_DATA3 | | | |
| **J1** | 24 | GPIO_J1_24 | QSPI1B_DATA2 | | | |
| **J1** | 26 | GPIO_J1_26 | QSPI1B_DATA1 | | | |
| **J1** | 28 | GPIO_J1_28 | QSPI1B_DATA0 | | | |
| **J1** | 30 | GPIO_J1_30 | QSPI1A_S | | | |
| **J1** | 32 | GPIO_J1_32 | QSPI1A_SCLK | | | |
| **J1** | 34 | GPIO_J1_34 | QSPI1A_DATA3 | | | |
| **J1** | 36 | GPIO_J1_36 | QSPI1A_DATA2 | | | |
| **J1** | 38 | GPIO_J1_38 | QSPI1A_DATA1 | | | |
| **J1** | 40 | GPIO_J1_40 | QSPI1A_DATA0 | | | |
| **J1** | 42 | | PMIC_ON_REQ SD3_DATA6 | | VDD_SNVS _IN | Mounting option |
| **J1** | 44 | | ONOFF SD3_DATA4 | | | Mounting option |
| **J1** | 46 | GND | | | | |
| **J1** | 48 | BKLT_PWM | GPIO1_IO11 | O | 3,3V | Preferred for backlight PWM |
| **J1** | 50 | LCD_PCLK | LCD1_CLK | | | |
| **J1** | 52 | GND | | | | |
| **J1** | 54 | VLCD_EN | LCD1_RESET | O | 3,3V | Preferred as VLCD enable |
| **J1** | 56 | DI0_DE | LCD1_ENABLE | O | 3,3V | |
| **J1** | 58 | DI0_HSYNC | LCD1_HSYNC | O | 3,3V | |
| **J1** | 60 | DI0_VSYNC | LCD1_VSYNC | O | 3,3V | |
| **J1** | 62 | GND | | | | |

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 64 | LCD_B0 | LCD1_DATA00 | O | 3,3V | |
| **J1** | 66 | LCD_B1 | LCD1_DATA01 | O | 3,3V | |
| **J1** | 68 | LCD_B2 | LCD1_DATA02 | O | 3,3V | |
| **J1** | 70 | LCD_B3 | LCD1_DATA03 | O | 3,3V | |
| **J1** | 72 | LCD_B4 | LCD1_DATA04 | O | 3,3V | |
| **J1** | 74 | LCD_B5 | LCD1_DATA05 | O | 3,3V | |
| **J1** | 76 | LCD_B6 | LCD1_DATA06 | O | 3,3V | |
| **J1** | 78 | LCD_B7 | LCD1_DATA07 | O | 3,3V | |
| **J1** | 80 | GND | | | | |
| | | | | | | |
| **J2** | 1 | ETH_A_D1+ | | | | 1st PHY 1GBit |
| **J2** | 3 | ETH_A_D1- | | | | 1st PHY 1GBit |
| **J2** | 5 | ETH_A_D2+ | | | | 1st PHY 1GBit |
| **J2** | 7 | ETH_A_D2- | | | | 1st PHY 1GBit |
| **J2** | 9 | ETH_A_D3+ | | | | 1st PHY 1GBit |
| **J2** | 11 | ETH_A_D3- | | | | 1st PHY 1GBit |
| **J2** | 13 | ETH_A_D4+ | | | | 1st PHY 1GBit |
| **J2** | 15 | ETH_A_D4- | | | | 1st PHY 1GBit |
| **J2** | 17 | GND | | | | |
| **J2** | 19 | ETH_B_D1+ | | | | 2nd PHY 1GBit |
| **J2** | 21 | ETH_B_D1- | | | | 2nd PHY 1GBit |
| **J2** | 23 | ETH_B_D2+ | | | | 2nd PHY 1GBit |
| **J2** | 25 | ETH_B_D2- | | | | 2nd PHY 1GBit |
| **J2** | 27 | ETH_B_D3+ | | | | 2nd PHY 1GBit |
| **J2** | 29 | ETH_B_D3- | | | | 2nd PHY 1GBit |
| **J2** | 31 | ETH_B_D4+ | | | | 2nd PHY 1GBit |
| **J2** | 33 | ETH_B_D4- | | | | 2nd PHY 1GBit |
| **J2** | 35 | GND | | | | |
| **J2** | 37 | USB_OTG_VBUS | USB_OTG_VBUS | I | 5,0V | Input; USB Phy voltage supply |
| **J2** | 39 | USB_OTG_PWRn | GPIO1_IO09 | O | 3,3V | On board pull-up 100k to 3,3V |
| **J2** | 41 | USB_OTG_ID | GPIO1_IO10 | I | 3,3V | USB OTG ID signal |
| **J2** | 43 | USB_OTG_DP | USB_OTG1_DP | I/O | | 90 Ohm differential pair |
| **J2** | 45 | USB_OTG_DN | USB_OTG1_DN | I/O | | 90 Ohm differential pair |
| **J2** | 47 | GND | | | | |
| **J2** | 49 | USB_SS_RXN | ADC2_IN1*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 51 | USB_SS_RXP | ADC2_IN0*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 53 | USB_SS_TXN | ADC1_IN1*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 55 | USB_SS_TXP | ADC1_IN0[*3] | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 57 | GND | | | | |
| **J2** | 59 | USB_H_VBUS | USB_OTG2_VBUS | I | 5,0V | USB Phy voltage supply; Preferred for host |
| **J2** | 61 | USB_H_DN | USB_OTG2_DN | | | 90 Ohm differential pair; Preferred for host |
| **J2** | 63 | USB_H_DP | USB_OTG2_DP | | | 90 Ohm differential pair; Preferred for host |
| **J2** | 65 | USB_H_PWRn | GPIO1_IO12 | O | 3,3V | Power enable |
| **J2** | 67 | VCC_AUD | | I | 3,0V | Noise reduced external power supply for audio codec |
| **J2** | 69 | AUDIO_A_GND | | I | | Noise reduced external power supply for audio codec. |
| **J2** | 71 | AUDIO_A_OUT_L | ENET1_CRS[*1] | O | | Line Out Left |
| **J2** | 73 | AUDIO_A_OUT_R | ENET1_TX_CLK[*1] | O | | Line Out Right |
| **J2** | 75 | AUDIO_A_MIC | ENET1_MDIO[*1] | I | | Microphone |
| **J2** | 77 | AUDIO_A_IN_L | ENET1_COL[*1] | I | | Line In Left |
| **J2** | 79 | AUDIO_A_IN_R | ENET1_RX_CLK[*1] | I | | Line In Right |
| **J2** | 2 | +V5S | VIN | I | | Main Power input<br>please refer chapter 0 |
| **J2** | 4 | +V5S | VIN | I | | Main Power input<br>please refer chapter 0 |
| **J2** | 6 | +V5S | VIN | I | | Main Power input<br>please refer chapter 0 |
| **J2** | 8 | GND | | | | |
| **J2** | 10 | GND | | | | |
| **J2** | 12 | GND | | | | |
| **J2** | 14 | ETH_A_LEDn | | O | 3,3V | 1st PHY Activity LED |
| **J2** | 16 | ETH_B_LEDn | | O | 3,3V | 2nd PHY Activity LED |
| **J2** | 18 | JTAG_TCK | JTAG_TCK | | 3,3V | |
| **J2** | 20 | JTAG_TMS | JTAG_TMS | | 3,3V | |
| **J2** | 22 | JTAG_TDI | JTAG_TDI | | 3,3V | |
| **J2** | 24 | JTAG_TDO | JTAG_TDO | | 3,3V | |
| **J2** | 26 | SD_A_VCC | NVCC_SD4 | I | 1,8V/3,3V | Power supply IN for external SDIO interface |
| **J2** | 28 | SD_A_VSEL | KEY_ROW1 | O | 3,3V | Low: 3,3V<br>High: 1,8V |
| **J2** | 30 | SD_A_RST | SD4_RESET | O | SD_A_VCC | |
| **J2** | 32 | SD_A_WP | KEY_ROW2 | I | 3,3V | Active Low=No write protect |
| **J2** | 34 | SD_A_CD | KEY_COL2 | I | 3,3V | |
| **J2** | 36 | SD_A_CMD | SD4_CMD | O | SD_A_VCC | Active low card detect |
| **J2** | 38 | SD_A_CLK | SD4_CLK | O | SD_A_VCC | |

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 40 | SD_A_DAT0 | SD4_DATA0 | I/O | SD_A_VCC | |
| **J2** | 42 | SD_A_DAT1 | SD4_DATA1 | I/O | SD_A_VCC | |
| **J2** | 44 | SD_A_DAT2 | SD4_DATA2 | I/O | SD_A_VCC | |
| **J2** | 46 | SD_A_DAT3 | SD4_DATA3 | I/O | SD_A_VCC | |
| **J2** | 48 | VD_VBAT | | I | | RTC battery Input. See chapter 6. |
| **J2** | 50 | VDD_SNVS | VDD_SNVS_IN | I | | |
| **J2** | 52 | +V3.3_OUT | VCC | O | | 20mA output from on module DCDC powered from VIN |
| **J2** | 54 | RESETINn | | I | VDD_SNVS | Power on reset Input; on board pull-up 10k to 3,3V |
| **J2** | 56 | PMIC_STBY | CCM_PMIC_STBY_R | O | | |
| **J2** | 58 | N.C. | | | | For future use |
| **J2** | 60 | N.C. | | | | For future use |
| **J2** | 62 | USB_TYPEC_VACK | ADC2_IN3*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 64 | USB_SS_SDA | ADC2_IN2*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 66 | USB_SS_SCL | ADC1_IN3*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 68 | USB_SS_INTn | ADC1_IN2*3 | I | | USB 3.0 signals not available<br>ADC is mounting option |
| **J2** | 70 | USB_TYPEC_EN | | | | |
| **J2** | 72 | BOOTSELn | | I | VDD_SNVS | Service jumper; normally left open; on board pull-up 10k to VDD_SNVS |
| **J2** | 74 | GND | | | | |
| **J2** | 76 | AUDIO_A_HP_L | GPIO1_IO00*1 | O | | onboard Pull-Up 4,7k*1 |
| **J2** | 78 | AUDIO_A_HP_R | GPIO1_IO01*1 | O | | onboard Pull-Up 4,7k*1 |
| **J2** | 80 | AUDIO_A_HP_GND | | I | | Noise reduced external power supply for audio codec |

*Table 1: B2B connector*

*1 Option in case Audio Codec isn't mounted

*2 Option only available in case eMMC is mounted

*3 Option

*optional

# 4 Interfaces

## 4.1 ADC

There are two 12bit ADC converter included in CPU with 4 inputs each. Because the reference voltage is the 3.3V power supply with 5% tolerance, the accuracy is limited.

For electrical details please refer the datasheet from NXP.

## 4.2 Audio

The audio codec NXP SGTL5000 is mounted on this module. There is a mounting option to output I2S signals and removing codec.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| J2 | 67 | VCC_AUD | | I | 3,0V | Noise reduced external power supply for audio codec |
| J2 | 69 | AUDIO_A_GND | | I | | Noise reduced external power supply for audio codec. |
| J2 | 71 | AUDIO_A_OUT_L | ENET1_CRS*1 | O | | Line Out Left |
| J2 | 73 | AUDIO_A_OUT_R | ENET1_TX_CLK*1 | O | | Line Out Right |
| J2 | 75 | AUDIO_A_MIC | ENET1_MDIO*1 | I | | Microphone |
| J2 | 77 | AUDIO_A_IN_L | ENET1_COL*1 | I | | Line In Left |
| J2 | 79 | AUDIO_A_IN_R | ENET1_RX_CLK*1 | I | | Line In Right |
| J2 | 76 | AUDIO_A_HP_L | GPIO1_IO00*1 | O | | onboard Pull-Up 4,7k*1 |
| J2 | 78 | AUDIO_A_HP_R | GPIO1_IO01*1 | O | | onboard Pull-Up 4,7k*1 |
| J2 | 80 | AUDIO_A_ HP_GND | | I | | Noise reduced external power supply for audio codec |
| | | | | | | |

*Table 2: Audio Interface*

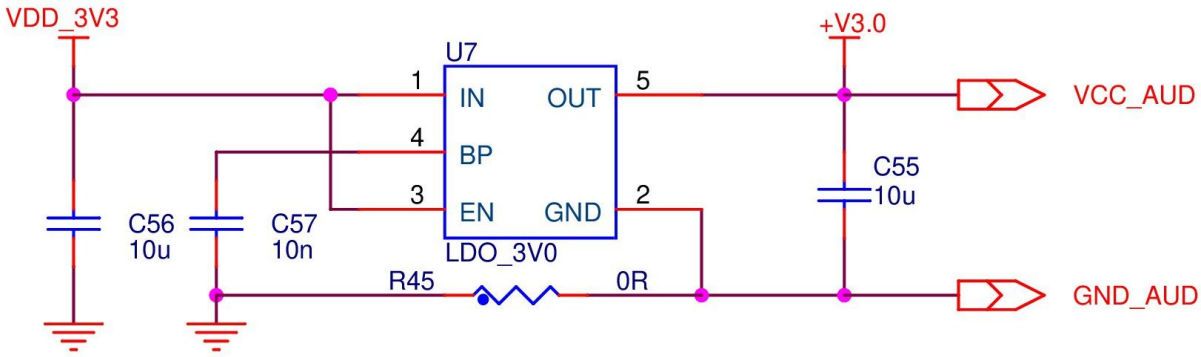


*Figure 5: Baseboard LDO power supply for codec analog voltage*

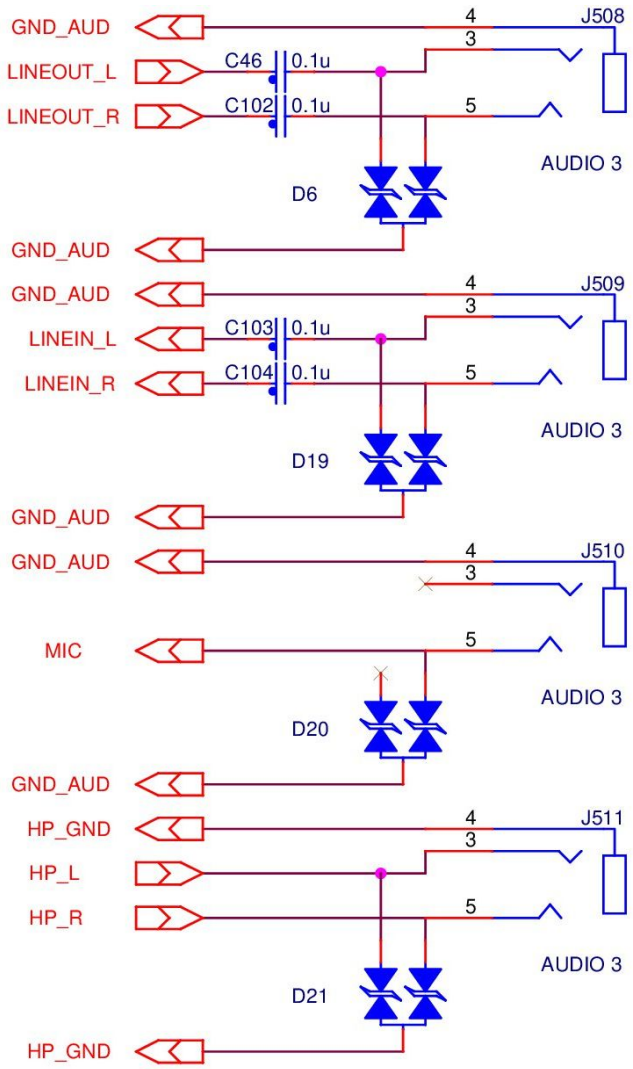


*Figure 6 : Audio In and Out*

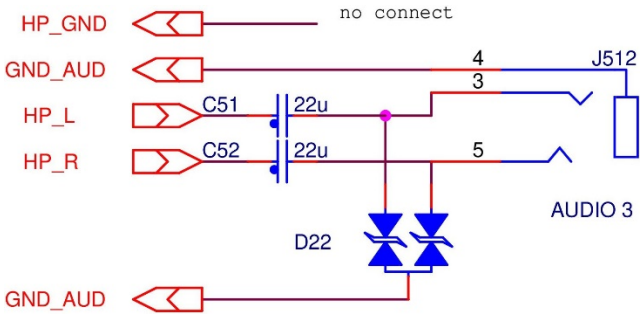


*Figure 7 : C coupled version of headphone out with GND instead HP_GND*

## 4.3 CAN Bus

The chip does provide the CAN bus transmit and receive TTL signal without any termination. Needs an interface chip to the CAN bus. If not used, please left signals unconnected.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 10 | CAN_A_RX | SD3_DATA7 | I | 3,3V | |
| **J1** | 12 | CAN_A_TX | SD3_DATA5 | O | 3,3V | |

*Table 3: CAN Bus Interface*

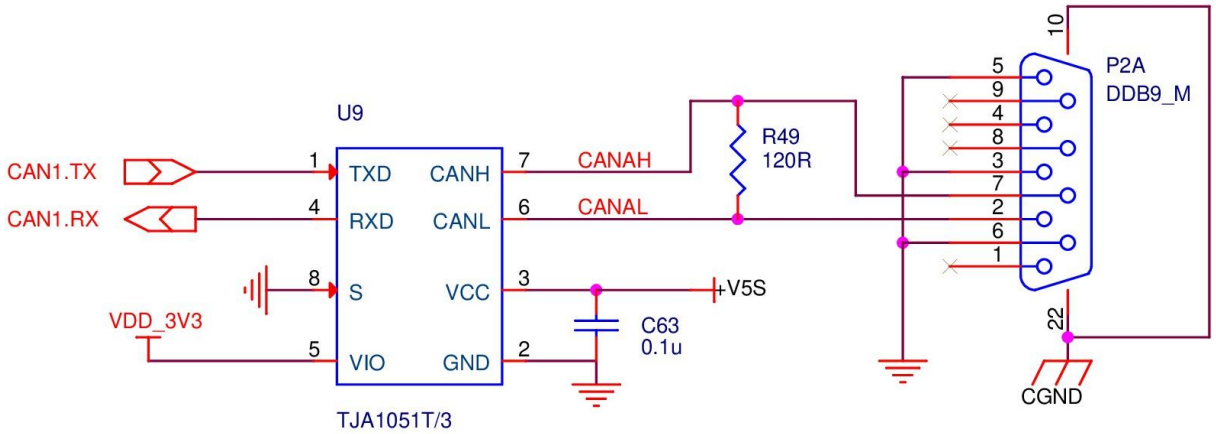


*Figure 8: CAN transceiver example*

## 4.4 Ethernet

The module supports two 10/100/1000 Mbit LAN interfaces. Two PHY AR8035 are mounted on the module.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 1 | ETH_A_D1+ | | | | 1st PHY 1GBit |
| **J2** | 3 | ETH_A_D1- | | | | 1st PHY 1GBit |
| **J2** | 5 | ETH_A_D2+ | | | | 1st PHY 1GBit |
| **J2** | 7 | ETH_A_D2- | | | | 1st PHY 1GBit |
| **J2** | 9 | ETH_A_D3+ | | | | 1st PHY 1GBit |
| **J2** | 11 | ETH_A_D3- | | | | 1st PHY 1GBit |
| **J2** | 13 | ETH_A_D4+ | | | | 1st PHY 1GBit |
| **J2** | 15 | ETH_A_D4- | | | | 1st PHY 1GBit |
| **J2** | 14 | ETH_A_LEDn | | O | 3,3V | 1st PHY Activity LED |
| | | | | | | |
| **J2** | 19 | ETH_B_D1+ | | | | 2nd PHY 1GBit |
| **J2** | 21 | ETH_B_D1- | | | | 2nd PHY 1GBit |
| **J2** | 23 | ETH_B_D2+ | | | | 2nd PHY 1GBit |

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 25 | ETH_B_D2- | | | | 2nd PHY 1GBit |
| **J2** | 27 | ETH_B_D3+ | | | | 2nd PHY 1GBit |
| **J2** | 29 | ETH_B_D3- | | | | 2nd PHY 1GBit |
| **J2** | 31 | ETH_B_D4+ | | | | 2nd PHY 1GBit |
| **J2** | 33 | ETH_B_D4- | | | | 2nd PHY 1GBit |
| | | | | | | |
| **J2** | 16 | ETH_B_LEDn | | O | 3,3V | 2nd PHY Activity LED |

*Table 4: LAN A and LAN B Interface*

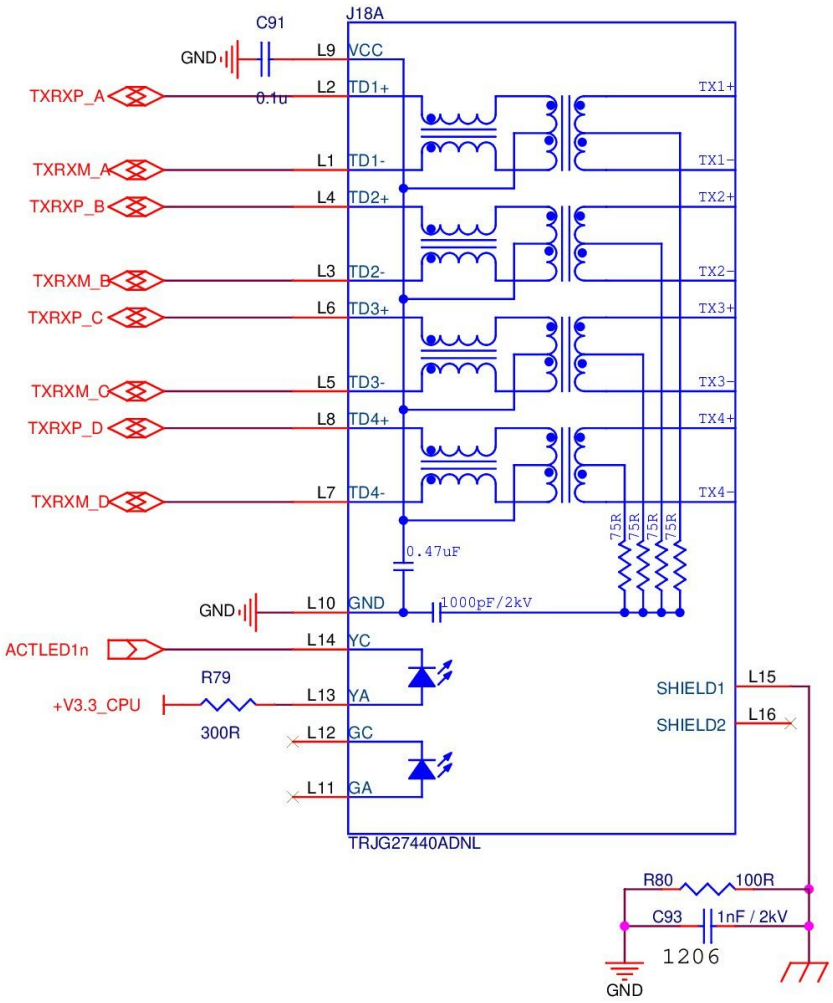


*Figure 9: LAN output example*

## 4.5 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

## 4.6 I2C

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 21 | I2C_A_SCL | SD3_DATA0 | I/O | 3,3V | Ext pull-up needed |
| **J1** | 23 | I2C_A_SDA | SD3_DATA1 | I/O | 3,3V | Ext pull-up needed |
| **J1** | 39 | I2C_B_IRQ | GPIO1_IO08 | | 3,3V | On board pull-up 100k to 3,3V |
| **J1** | 41 | I2C_B_SCL | GPIO1_IO02 | | 3,3V | Ext pull-up needed |
| **J1** | 43 | I2C_B_SDA | GPIO1_IO03 | | 3,3V | Ext pull-up needed |

*Table 5: I2C Interface*

I2Cx.SCL and I2Cx.DAT do not have pullup on module.
4k7 pullup to 3.3V has to be added on baseboard.

## 4.7 JTAG

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 18 | JTAG_TCK | JTAG_TCK | | 3,3V | |
| **J2** | 20 | JTAG_TMS | JTAG_TMS | | 3,3V | |
| **J2** | 22 | JTAG_TDI | JTAG_TDI | | 3,3V | |
| **J2** | 24 | JTAG_TDO | JTAG_TDO | | 3,3V | |
| | | | | | | |

*Table 6: JTAG Interface*

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

## 4.8 SDIO Interfaces

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 26 | SD_A_VCC | NVCC_SD4 | I | 1,8V/3,3V | Power supply IN for external SDIO interface |
| **J2** | 28 | SD_A_VSEL | KEY_ROW1 | O | 3,3V | Low: 3,3V<br>High: 1,8V |
| **J2** | 30 | SD_A_RST | SD4_RESET | O | SD_A_VCC | |
| **J2** | 32 | SD_A_WP | KEY_ROW2 | I | 3,3V | Active Low=No write protect |
| **J2** | 34 | SD_A_CD | KEY_COL2 | I | 3,3V | |
| **J2** | 36 | SD_A_CMD | SD4_CMD | O | SD_A_VCC | Active low card detect |
| **J2** | 38 | SD_A_CLK | SD4_CLK | O | SD_A_VCC | |
| **J2** | 40 | SD_A_DAT0 | SD4_DATA0 | I/O | SD_A_VCC | |
| **J2** | 42 | SD_A_DAT1 | SD4_DATA1 | I/O | SD_A_VCC | |
| **J2** | 44 | SD_A_DAT2 | SD4_DATA2 | I/O | SD_A_VCC | |
| **J2** | 46 | SD_A_DAT3 | SD4_DATA3 | I/O | SD_A_VCC | |

*Table 7: SDIO Interface*

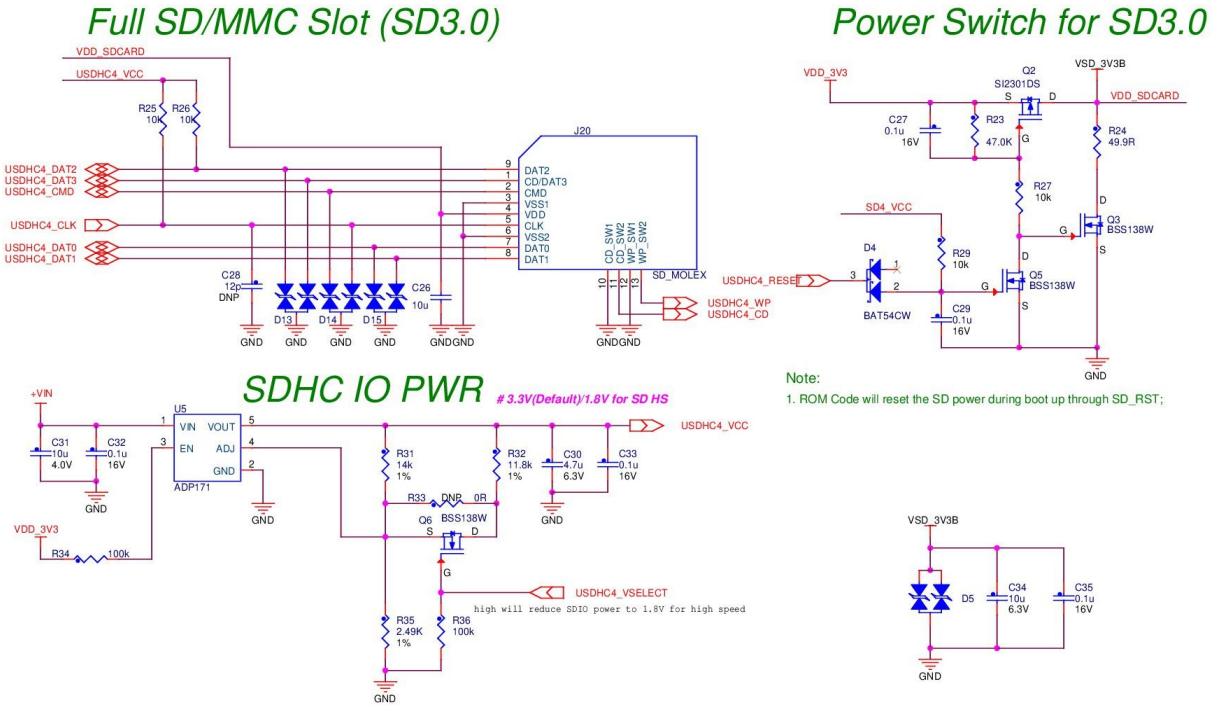


*Figure 10: SDHC full feature example*

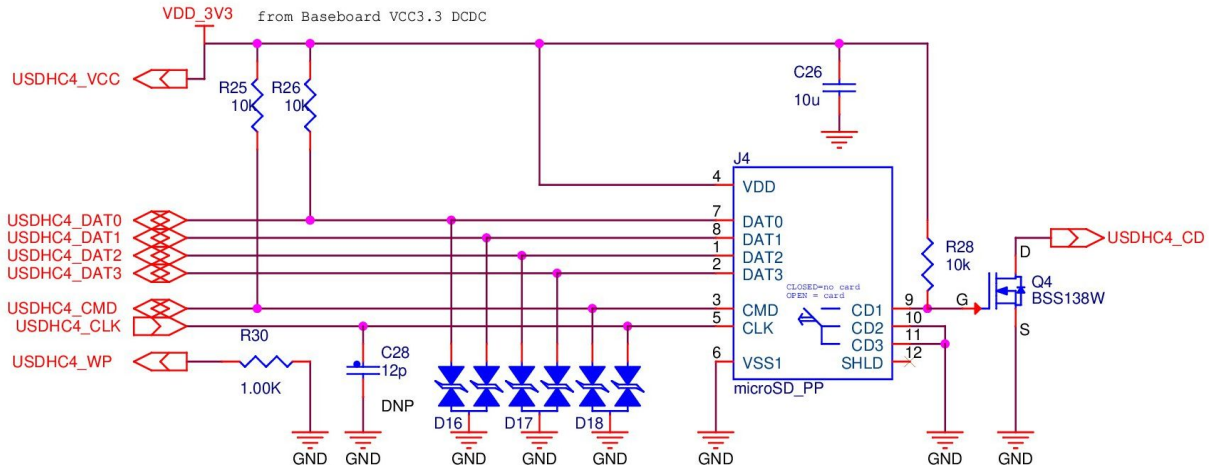


*Figure 11: SD basic feature w/o high speed support*

## 4.9 SPI Interface

The module support HS SPI (Serial Peripheral Interface) with 1 chip. All signals are 3.3V compliant. Devices on baseboard with other voltage need a level shifter.

Signals don't have pullups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 14 | SPI_A_SS0 | QSPI1B_DQS | O | 3,3V | |
| **J1** | 16 | SPI_A_MISO | QSPI1A_S | I | 3,3V | |
| **J1** | 18 | SPI_A_MOSI | QSPI1A_DQS | O | 3,3V | |
| **J1** | 20 | SPI_A_SCLK | QSPI1B_S | O | 3,3V | |

*Table 8: SPI Interface*

## 4.10 Serial Ports (UART)

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J1** | 1 | UART_A_RXD | SD4_DATA4 | I | SD_A_VCC | |
| **J1** | 3 | UART_A_RTS | SD4_DATA6 | I | SD_A_VCC | Use as CTS from external side |
| **J1** | 2 | UART_A_TXD | SD4_DATA5 | O | SD_A_VCC | |
| **J1** | 4 | UART_A_CTS | SD4_DATA7 | O | SD_A_VCC | Use as RTS from external side |
| | | | | | | |
| **J1** | 5 | UART_B_RXD | QSPI1B_SCLK | I | 3,3V | |
| **J1** | 7 | UART_B_TXD | QSPI1B_S | O | 3,3V | |
| | | | | | | |
| **J1** | 9 | UART_C_CTS | SD3_DATA2 | I | 3,3V | Use as CTS from external side |
| **J1** | 11 | UART_C_RTS | SD3_CLK | O | 3,3V | Use as RTS from external side |
| **J1** | 13 | UART_C_RXD | SD3_DATA3 | I | 3,3V | |
| **J1** | 15 | UART_C_TXD | SD3_CMD | O | 3,3V | |
| | | | | | | |
| **J1** | 17 | UART_D_RXD | GPIO1_IO07 | I | 3,3V | |
| **J1** | 19 | UART_D_TXD | GPIO1_IO06 | O | 3,3V | |

*Table 9: UART Interfaces*

We recommend to use UART_B for debugging and service only.

For UART_A voltage SD4_VCC is used. Depending from used voltage a different transceiver is necessary.

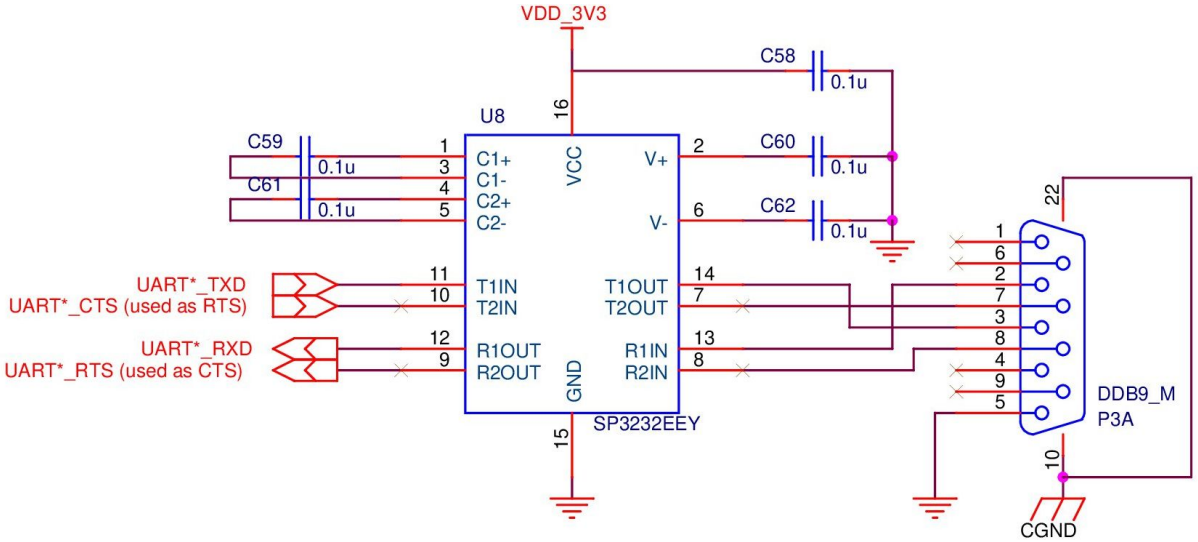


*Figure 12: UART transceiver example*

## 4.11 USB host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 59 | USB_H_VBUS | USB_OTG2_VBUS | I | 5,0V | USB Phy voltage supply; Preferred for host |
| **J2** | 61 | USB_H_DN | USB_OTG2_DN | | | 90 Ohm differential pair; Preferred for host |
| **J2** | 63 | USB_H_DP | USB_OTG2_DP | | | 90 Ohm differential pair; Preferred for host |
| **J2** | 65 | USB_H_PWRn | GPIO1_IO12 | O | 3,3V | Power enable |

*Table 10: USB Host Interface*

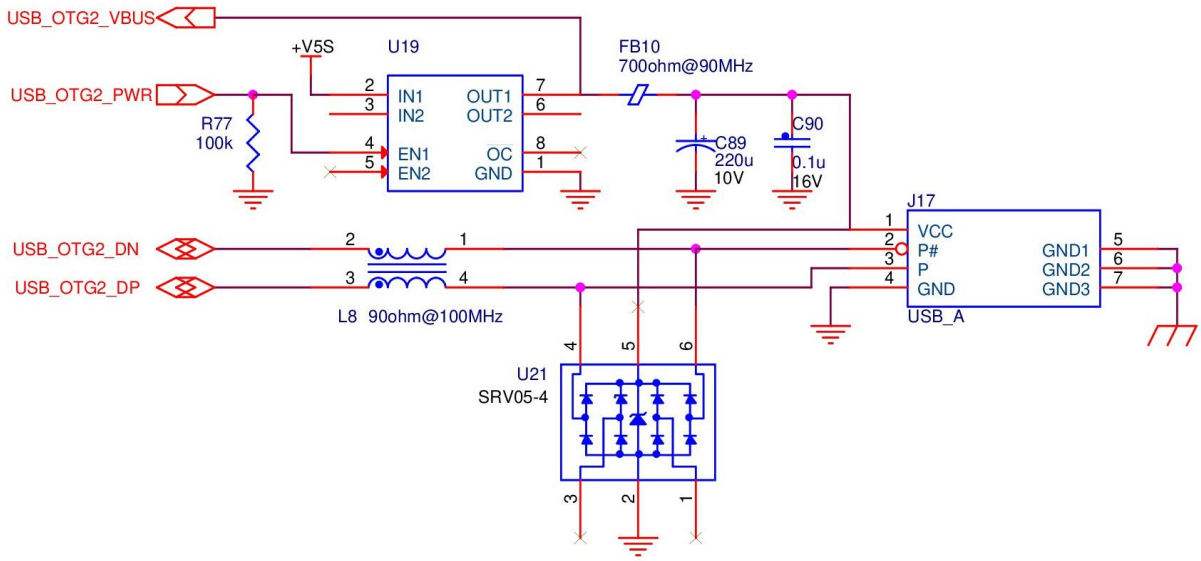


*Figure 13: USB Host Full Feature Example*

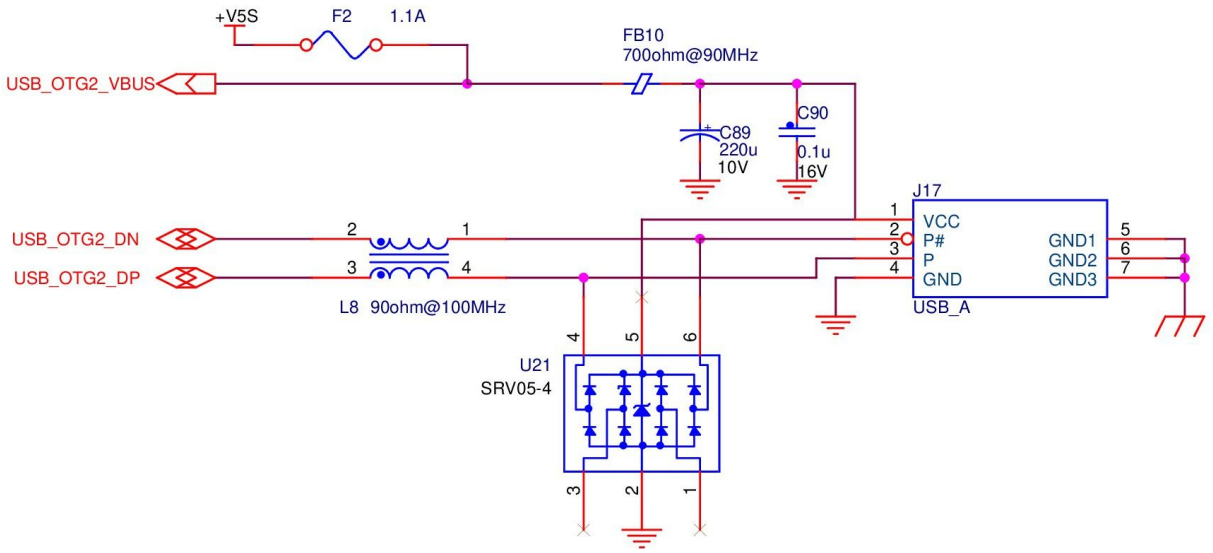


*Figure 14: USB Host Basic Feature Example*

## 4.12 USB OTG

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

| | Pin | Signal | CPU Pad | I/O | Volt | Description |
|---|---|---|---|---|---|---|
| **J2** | 37 | USB_OTG_VBUS | USB_OTG_VBUS | I | 5,0V | Input; USB Phy voltage supply |
| **J2** | 39 | USB_OTG_PWRn | GPIO1_IO09 | O | 3,3V | On board pull-up 100k to 3,3V |
| **J2** | 41 | USB_OTG_ID | GPIO1_IO10 | I | 3,3V | USB OTG ID signal |
| **J2** | 43 | USB_OTG_DP | USB_OTG1_DP | I/O | | 90 Ohm differential pair |
| **J2** | 45 | USB_OTG_DN | USB_OTG1_DN | I/O | | 90 Ohm differential pair |

*Table 11: USB OTG Interface*

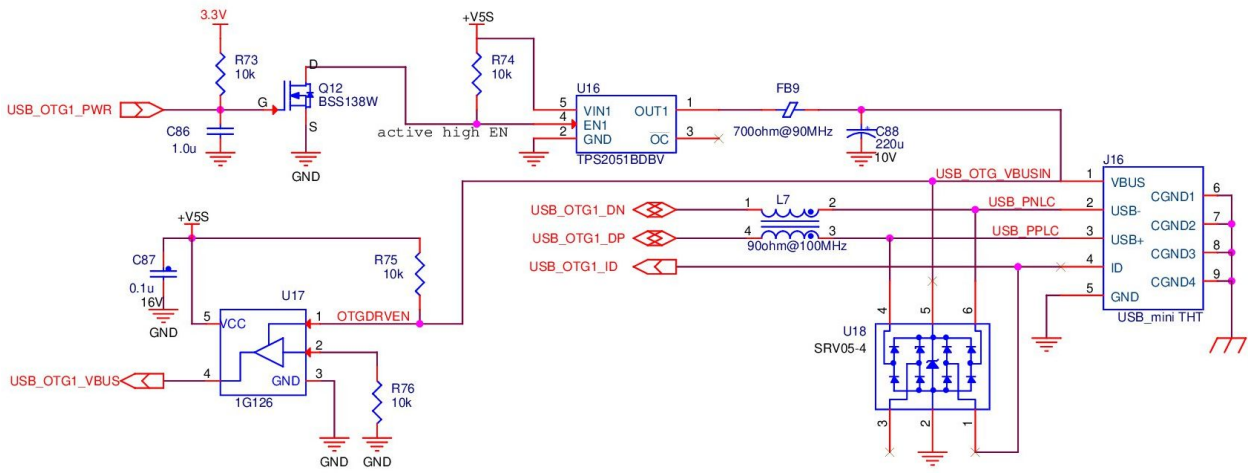


*Figure 15: USB OTG full feature example*

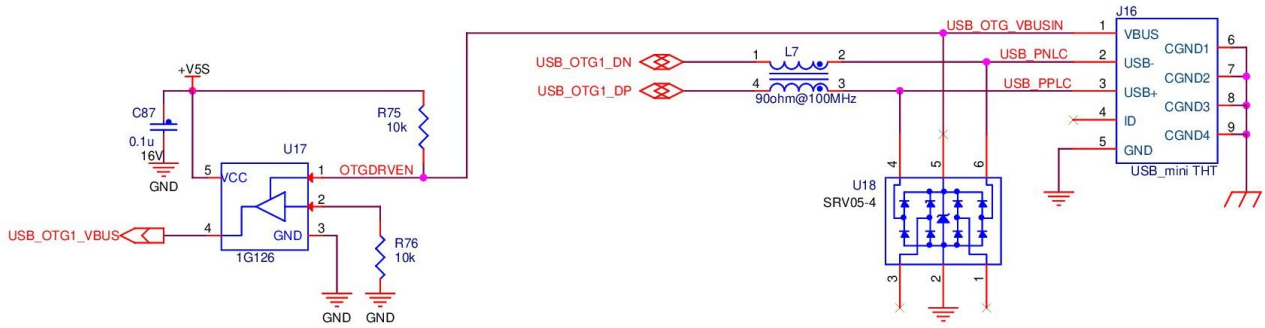


*Figure 16: Basic USB Device Example*

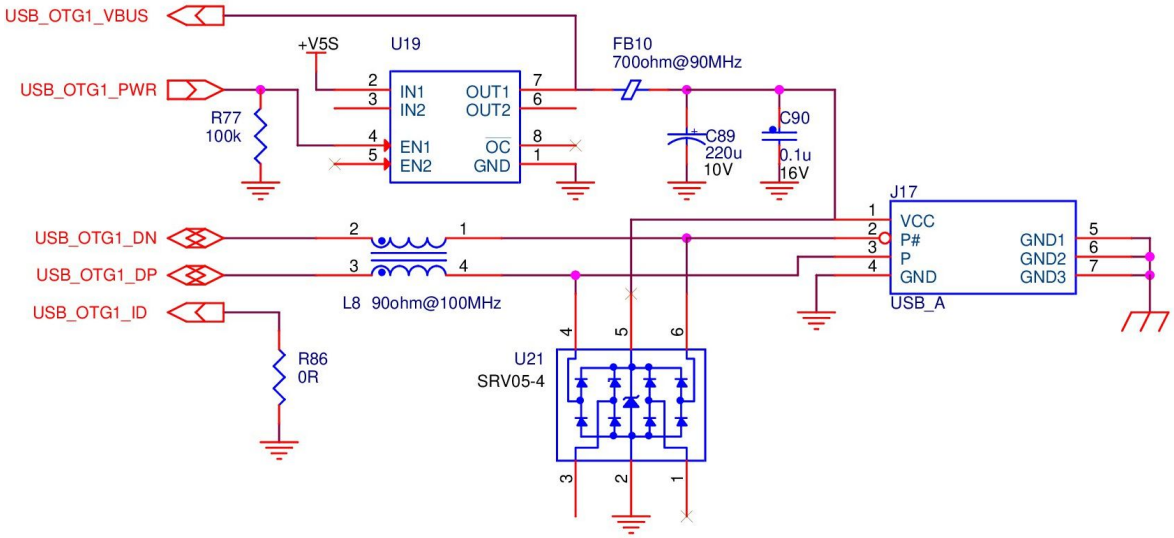


*Figure 17: USB OTG Host example*

## 4.13 RGB LCD

| | Pin | Signal | CPU Pad | I/O | Volt | 18bit[1] | 24bit |
|---|---|---|---|---|---|---|---|
| **J1** | 47 | LCD_R0 | LCD1_DATA16 | O | 3,3V | n.a. | R0 |
| **J1** | 49 | LCD_R1 | LCD1_DATA17 | O | 3.,3V | n.a. | R1 |
| **J1** | 51 | LCD_R2 | LCD1_DATA18 | O | 3.,3V | R0 | R2 |
| **J1** | 53 | LCD_R3 | LCD1_DATA19 | O | 3.,3V | R1 | R3 |
| **J1** | 55 | LCD_R4 | LCD1_DATA20 | O | 3.,3V | R2 | R4 |
| **J1** | 57 | LCD_R5 | LCD1_DATA21 | O | 3.,3V | R3 | R5 |
| **J1** | 59 | LCD_R6 | LCD1_DATA22 | O | 3.,3V | R4 | R6 |
| **J1** | 61 | LCD_R7 | LCD1_DATA23 | O | 3.,3V | R5 | R7 |
| **J1** | 65 | LCD_G0 | LCD1_DATA08 | O | 3.,3V | n.a. | G0 |
| **J1** | 67 | LCD_G1 | LCD1_DATA09 | O | 3.,3V | n.a. | G1 |
| **J1** | 69 | LCD_G2 | LCD1_DATA10 | O | 3.,3V | G0 | G2 |
| **J1** | 71 | LCD_G3 | LCD1_DATA11 | O | 3.,3V | G1 | G3 |
| **J1** | 73 | LCD_G4 | LCD1_DATA12 | O | 3.,3V | G2 | G4 |
| **J1** | 75 | LCD_G5 | LCD1_DATA13 | O | 3.,3V | G3 | G5 |
| **J1** | 77 | LCD_G6 | LCD1_DATA14 | O | 3.,3V | G4 | G6 |
| **J1** | 79 | LCD_G7 | LCD1_DATA15 | O | 3.,3V | G5 | G7 |
| **J1** | 64 | LCD_B0 | LCD1_DATA00 | O | 3,3V | n.a. | B0 |
| **J1** | 66 | LCD_B1 | LCD1_DATA01 | O | 3,3V | n.a. | B1 |
| **J1** | 68 | LCD_B2 | LCD1_DATA02 | O | 3,3V | G0 | B2 |
| **J1** | 70 | LCD_B3 | LCD1_DATA03 | O | 3,3V | G1 | B3 |
| **J1** | 72 | LCD_B4 | LCD1_DATA04 | O | 3,3V | G2 | B4 |
| **J1** | 74 | LCD_B5 | LCD1_DATA05 | O | 3,3V | G3 | B5 |
| **J1** | 76 | LCD_B6 | LCD1_DATA06 | O | 3,3V | G4 | B6 |
| **J1** | 78 | LCD_B7 | LCD1_DATA07 | O | 3,3V | G5 | B7 |
| **J1** | 50 | LCD_PCLK | LCD1_CLK | O | | Pixel clock | |
| **J1** | 56 | DI0_DE | LCD1_ENABLE | O | 3,3V | DE Signal | |
| **J1** | 58 | DI0_HSYNC | LCD1_HSYNC | O | 3,3V | Horizontal sync | |
| **J1** | 60 | DI0_VSYNC | LCD1_VSYNC | O | 3,3V | Vertical sync | |
| **J1** | 48 | BKLT_PWM | GPIO1_IO11 | O | 3,3V | Preferred for backlight PWM | |
| **J1** | 54 | VLCD_EN | LCD1_RESET | O | 3,3V | Preferred as VLCD enable | |

*Table 12: Display Interface*

Because all signals work with 3.3V TTL level and high speed, high EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary. Using serial resistors or EMI filter network (e.g. Nexperia IP4254CZ16) is highly recommended. For additional controls use GPIOs and modify the driver.

[1] By default, we use 24 bit output data path also for 18Bit displays. The IOMUX for unused data bits R0/R1, G0/G1 and B0/B1 are NOT configured for LCDIF and therefore can be used for different function.

## 4.14 Power and power control Pins

| | Pin | Signal | CPU Pad | I/O | Description |
|---|---|---|---|---|---|
| **J2** | 2<br>4<br>6 | +V5S | VIN | I | Main Power input<br>please refer chapter “8 Electrical characteristic” |
| **J2** | 48 | VD_VBAT | | I | RTC battery Input. Tie to to VDD_SNVS if you don’t need RTC; don’t leave unconnected<br>See chapter “6 RTC” and chapter “8 Electrical characteristic” |
| **J2** | 50 | VDD_SNVS | VDD_SNVS_IN | I | SNVS voltage input; tie to 3,3V; don’t leave unconnected |
| **J2** | 52 | +V3.3_OUT | VCC | O | 20mA output from on module DCDC<br>powered from VIN |
| **J2** | 26 | SD_A_VCC | NVCC_SD4 | I | Power supply IN for external SDIO interface: 3,3V or 1,8V. |
| **J2** | 37 | USB_OTG_VBUS | USB_OTG_VBUS | I | Input; USB Phy voltage supply: 5.0V |
| **J2** | 59 | USB_H_VBUS | USB_OTG2_VBUS | I | Input; USB Phy voltage supply; 5.0V |
| | | | | | |
| **J2** | 54 | RESETINn | | I | Power on reset Input;<br>on board pull-up 10k to 3,3V |
| **J2** | 56 | PMIC_STBY | CCM_PMIC_STBY_R | O | |

*Table 13: Power and Power Control*

VDD_SNVS could be powered separately in special secure Non-Volatile Storage schemes. In normal usage just tie to 3.3V.

3.3V_OUT is the DCDC power supply of the module powered from VIN. Use as enable for baseboard power regulators.

RESETIN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On module, DCDCs will not get a reset. On power fail, VIN has to be switched off and on to avoid latchup effects.

PMIC_STBY_REQ is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It is possible to use a supercap instead.

Form following figure shows a possible schematic for the VBAT input. Following components are NOT on PicoCoreMX6SX, you have to put them on your base board.

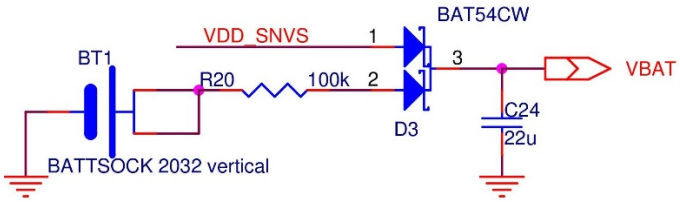


*Figure 18 : VBAT example*

# 5 Flash

## 5.1 NAND Flash

By default, boot mode is configured for NAND boot.

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S or TFAT to be robust against power failures

## 5.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

The eMMC Flash is based on multi level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

## 5.3 I2C EEPROM

| |
|---|
| This component is optional and not mounted in all configurations. Please contact sales to get more information. |

# 6 RTC

There is a NXP PCF85063TP or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

# 7 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP A1006 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

| |
|---|
| This component is optional and not mounted in all configurations. Please contact sales to get more information. |

# 8 Electrical characteristic

VIN: 3.8V .. 5.5V

VBAT In for RTC: 2.2 … 3.45V

power consumption

typical current consumption BATT: 0.22 µA

maximum power consumption BATT: 0.6 µA @85°C

Thermal design power (summary all chips)

With 1GHz SoloX CPU 5.5 Watt @25°C

Maximum output current 3.3V 20 mA

Power consumption of connected devices like display, USB devices, SD card has to be added for power calculation.

Real power consumption could be much lower depends CPU workload, used graphic interfaces and features and the workload on I/O interfaces.

## 8.1 Absolute maximum ratings

| Description | Min | Max | Unit |
|---|---|---|---|
| Input Voltage range 3.3V IO pins | -0.3 | OVDD*+0.3 | V |
| Voltage on any IO with VIN off | | 0.3 | V |
| USB VBUS | -0.3 | 5.6 | V |

*Table 14: Absolute Maximum Ratings*

## 8.2 DC Electrical Characteristics

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| VIN | Module main power | | 3.8 | 5.5 | V |
| VBAT | RTC power | | 0.9 | 5.5 | V |
| USDHC4_VCC | SDHC power | | 1.65 | 3.6 | |
| $I_{USDHC4}$ | SDHC controller supply current | | | 25 | mA |
| USB_OTG*_VBUS | USB supply voltage | | 4.4 | 5.5 | |
| $I_{VBUS}$ | USB supply current | | | 100 | mA |
| VDD_SNVS_IN | SNVS supply | | 2.4 | 3.6 | V |
| OVDD | On module 3.3V DCDC | | 3.15 | 3.45 | V |
| $V_{ih}$ | High Level Input Voltage | | 0.7*OVDD | OVDD | V |
| $V_{il}$ | Low Level Input Voltage | | 0 | 0.3*OVDD | V |
| $V_{oh}$ | High Level Output Voltage | $I_{oh}$=0.1mA | 2.98 | | V |
| $V_{ol}$ | Low Level Output Voltage | $I_{ol}$=0.1mA | | 0.15 | V |
| $I_o$ | Output current IOs | 3.3V | | 5 | mA |

*Table 15: DC electrical characteristics*

*OVDD = power on pin 3.3V from on module DCDC*

# 9 Thermal Specification

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating temperature | 0 | | +70[1] | °C |
| Operating temperature (“I”)[2] | -20 | | +85[1] | °C |
| Junction temperature i.MX6ULL | 0 | | +95 | °C |
| Junction temperature i.MX6ULL (“E”) | -20 | | +105 | °C |
| Junction temperature i.MX6ULL (“I”) [2] | -40 | | +105 | °C |
| Junction to Top of i.MX6ULL (Psi-JT)[3] | | 2,0 | | °C/W |

[1] Depending on cooling solution. See also: *Power consumption and cooling*

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2. Valid for 14x14mm package.

# 10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

# 11 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

# 12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

# 13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be 5.5 Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Dependent from your application and your worst-case scenario, the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. 1 and 3.5 Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

**Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board**.

To calculate your cooling we recommend this helpful literature and the CPU datasheet (VK package starting page 27)

- CPU datasheet from NXP
- AN4579 from NXP
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/

- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

# 14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

# 15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

# 16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 10 boards. An empty tray is used as top cover.

*Figure 19: Packaging in Trays*

# 17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.


*Figure 20: Matrix Code Sticker*

# 18 Appendix

## Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

F&S reserves the right to make changes in its products or product specifications or product documentation with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

F&S makes no warranty or guarantee regarding the suitability of its products for any particular purpose, nor does F&S assume any liability arising out of the documentation or use of any product and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

Products are not designed, intended, or authorized for use as components in systems intended for applications intended to support or sustain life, or for any other application in which the failure of the product from F&S could create a situation where personal injury or death may occur. Should the Buyer purchase or use a F&S product for any such unintended or unauthorized application, the Buyer shall indemnify and hold F&S and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that F&S was negligent regarding the design or manufacture of said product.

Specifications are subject to change without notice.

## Warranty Terms

**Hardware Warranties**
F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S’s sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

**Software Warranties**
Software is provided “AS IS”. F&S makes no warranties, either express or implied, with regard to the software object code or software source code either or with respect to any third party materials or intellectual property obtained from third parties. F&S makes no warranty that the software is useable or fit for any particular purpose. This warranty replaces all other warranties written or unwritten. F&S expressly disclaims any such warranties. In no case shall F&S be liable for any consequential damages.

**Disclaimer of Warranty**
THIS WARRANTY IS MADE IN PLACE OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

**Limitation on Liability**
UNDER NO CIRCUMSTANCES SHALL F&S BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL F&S BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE PRODUCT, THE CUSTOMER APPROVES THAT THE F&S PRODUCT, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS

# 19 Content