Hardware Documentation

PicoCore™RT1
HW Revision 1.00

Preliminary

Version 001
(2019-11-26)

Elektronik Systeme

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About This Document

This document describes how to use the PicoCore™RT1 board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
27.11.19	001	All		-	Initial Version	MD

V	Version
A, M, R	Added, Modified, Removed
Au	Author

Table of Contents

1 Main Features

The following table shows the maximum possible number of each interface. Not all interfaces are available at the same time and depends on the appropriate assembly variant.

Features	Description
CPU	NXP i.MXRT1052
RAM	256Mbit DDR3L SDRAM
Flash	256MB NAND
Display	RGB-LCD
SD-Card	1 x SD Card Slot (external)
Audio	1 x Analog Line in/out, HP, MIC; opt. digital I2S)
Interfaces	1 x Ethernet 10/100Mbit 1 x USB OTG (Host/Device), 1 x USB Host Mode 3 x UART (2 x without CTS/RTS, 1 x with RTS/CTS) 1 x I2C 1 x SPI 2 x CAN2.0

Table 1: Main Features

2 Mechanical Dimensions

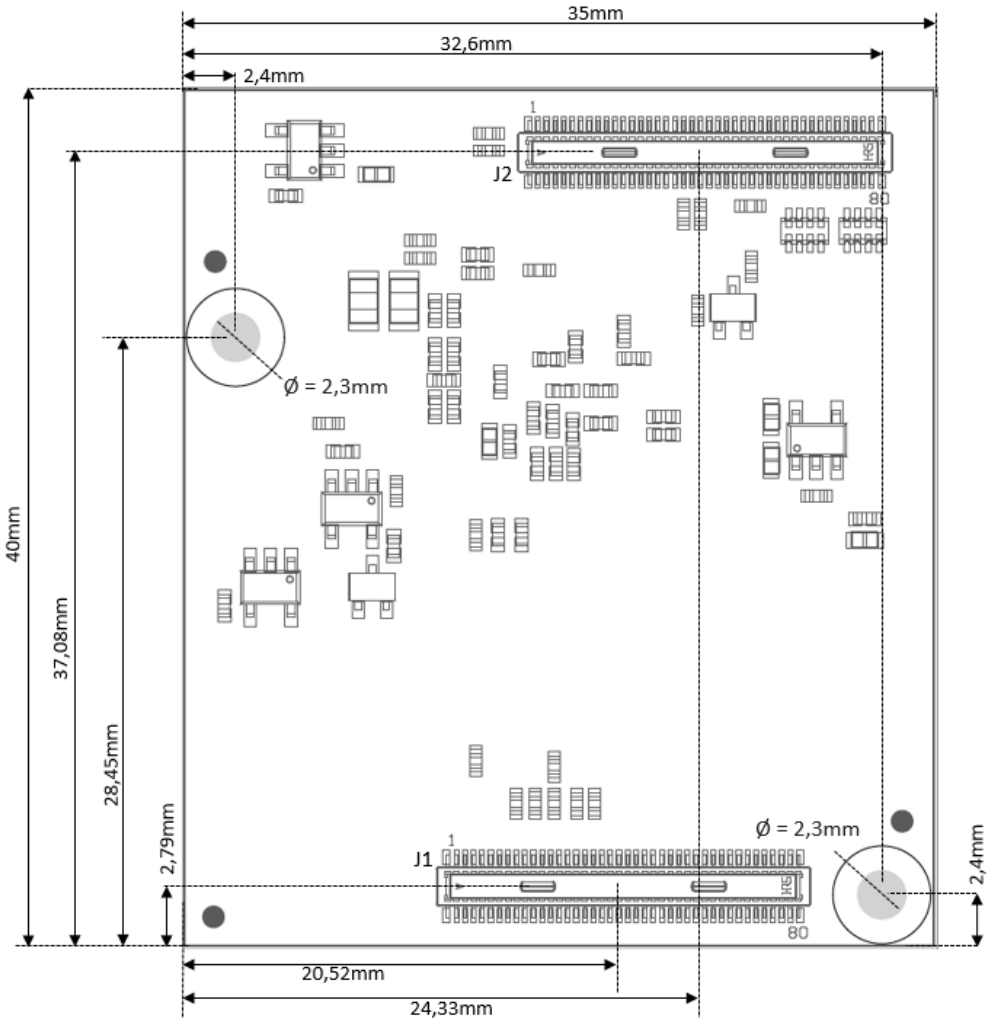

Figure 1: Mechanical Dimensions [mm] (Bottom View)

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ±0.1mm
Height of the parts on the top side	1.1mm
Height of the parts on the bottom side	1.1mm
Weight	7gr

Table 2: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2. 1 SMT Steel Spacer

For mounting, we recommend SMT Steel Spacer from supplier “Würth Elektronik” order number “9774015243R”. This part is in stock and can be ordered via F&S web shop.

If you use different stacking high, you have to change the Spacer.

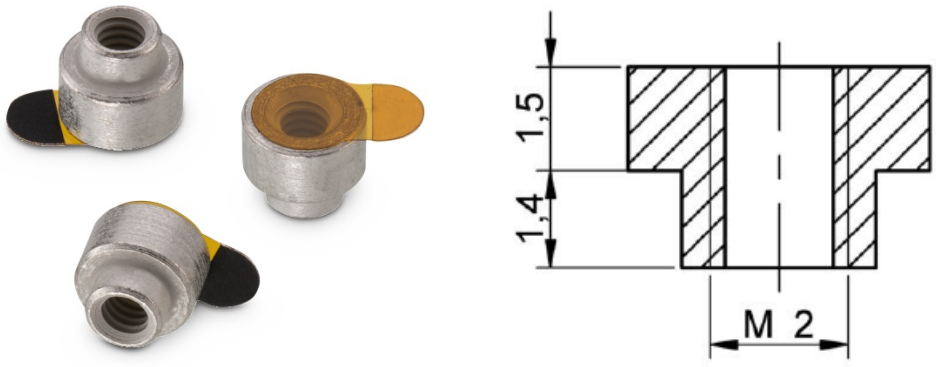

Figure 2: WE SMT Steel Spacer

Data sheet and 3D model (STP) is available on our website.

3 Interface and signal description

3.1 B2B connectors (J1 & J2)

PicoCoreRT1 is using two 80 pin connectors from manufacturer Hirose.
Part number: DF40C-80DP-0.4V
Part number counterpart: DF40C-80DS-0.4V.

With this combination, you get minimal stacking height of 1,5mm. Other possible stacking heights by using different counterpart connector are: 2mm, 3mm, 3,5mm and 4mm. The connector with 1,5mm stacking height is in stock at F&S and can be ordered in F&S web shop.

J1 Pin	Signal Name	i.MXRT1052 Pin	I/O	Voltage	Remarks
1	NC	X	X	X	
2	NC	X	X	X	
3	NC	X	X	X	
4	NC	X	X	X	
5	NC	X	X	X	
6	UART1_RX	UART_A_RXD	I	3.3V	Pulled Up to VDD_3V3 with 10K
7	NC	X	X	X	
8	UART1_TX	UART_A_TXD	O	3.3V	
9	UART2_CTS	UART_C_CTS	O	3.3V	
10	CAN1_RX	CAN_A_RX	I	3.3V	Pulled Up to VDD_3V3 with 100K
11	UART2_RTS	UART_C_RTS	I	3.3V	
12	CAN1_TX	CAN_A_TX	O	3.3V	
13	UART2_RX	UART_C_RXD	I	3.3V	Pulled Up to VDD_3V3 with 10K
14	GPIO5_3	SPI_A_SS0	I/O	3.3V	GPIO, CPU WAKEUP Pin
15	UART2_TX	UART_C_TXD	O	3.3V	
16	SPA1_SDI	SPI_A_MISO	I	3.3V	
17	UART5_RX	UART_D_RXD	I	3.3V	Pulled Up to VDD_3V3 with 100K
18	SPI1_SDO	SPI_A_MOSI	O	3.3V	
19	UART5_TX	UART_D_TXD	O	3.3V	
20	SPI1_SCK	SPI_A_SCLK	O	3.3V	
21	I2C3_SCL	I2C_A_SCL	O	3.3V	Pulled Up to VDD_3V3 with 100K

J1 Pin	Signal Name	i.MXRT1052 Pin	I/O	Voltage	Remarks
22	GPIO1_1	GPIO_J1_22	I/O	3.3V	GPIO
23	I2C3_SDA	I2C_A_SDA	I/O	3.3V	Pulled Up to VDD_3V3 with 2.49K
24	GPIO1_2	GPIO_J1_24	I/O	3.3V	GPIO
25	JTAG_MOD	JTAG_MOD	I/O	3.3V	Pulled Down to GND with 10K
26	GPIO2_1	GPIO_J1_26	I/O	3.3V	***GPIO, Ethernet Interrupt (not connected)***
27	CAN2_RX	GPIO_J1_27	I	3.3V	Pulled Up to VDD_3V3 with 100K
28	NC	X	X	X	
29	GPIO1_3	GPIO_J1_29	I/O	3.3V	
30	NC	X	X	X	
31	NC	X	X	X	
32	NC	X	X	X	
33	CAN2_TX	GPIO_J1_33	O	3.3V	
34	NC	X	X	X	
35	NC	X	X	X	
36	NC	X	X	X	
37	NC	X	X	X	
38	NC	X	X	X	
39	NC	X	X	X	
40	NC	X	X	X	
41	NC	X	X	X	
42	NC	X	X	X	
43	NC	X	X	X	
44	ON/OFF	GPIO_J1_44	I	3.3V	GPIO
45	GND	GND	PWR	GND	
46	GND	GND	PWR	GND	
47	NC	X	X	X	
48	PWM1_A	GPIO_SD_B0_04	O	3.3V	BL_PWM
49	NC	X	X	X	
50	LCDIF_CLK	GPIO_B0_00	I	3.3V	LCD_PCLK
51	NC	X	X	X	
52	GND	GND	PWR	GND	
53	LCDIF_0	GPIO_B0_04	O	3.3V	LCD_R3
54	GPIO3_2	GPIO_SD_B1_05	I	3.3V	VLCD_EN

J1 Pin	Signal Name	i.MXRT1052 Pin	I/O	Voltage	Remarks
55	LCDIF_D1	GPIO_B0_05	O	3.3V	LCD_R4
56	LCDIF_ENABLE	GPIO_B0_01	O	3.3V	LCD_DE
57	LCDIF_D2	GPIO_B0_06	O	3.3V	LCD_R5
58	LCDIF_HSYNC	GPIO_B0_02	O	3.3V	LCD_HSYNC
59	LCDIF_D3	GPIO_B0_07	O	3.3V	LCD_R6
60	LCDIF_VSYNC	GPIO_B0_03	O	3.3V	LCD_VSYNC
61	LCDIF_D4	GPIO_B0_08	O	3.3V	LCD_R7
62	GND	GND	PWR	GND	
63	GND	GND	PWR	GND	
64	NC	X	X	X	
65	NC	X	X	X	
66	NC	X	X	X	
67	NC	X	X	X	
68	NC	X	X	X	
69	LCDIF_D5	GPIO_B0_09	O	3.3V	LCD_G2
70	LCDIF_D11	GPIO_B0_10	O	3.3V	LCD_B3
71	LCDIF_D6	GPIO_B0_11	O	3.3V	LCD_G3
72	LCDIF_D12	GPIO_B0_12	O	3.3V	LCD_B4
73	LCDIF_D7	GPIO_B0_13	O	3.3V	LCD_G4
74	LCDIF_D13	GPIO_B0_14	O	3.3V	LCD_B5
75	LCDIF_D8	GPIO_B0_15	O	3.3V	LCD_G5
76	LCDIF_D14	GPIO_B1_0	O	3.3V	LCD_B6
77	LCDIF_D9	GPIO_B1_1	O	3.3V	LCD_G6
78	LCDIF_D15	GPIO_B1_2	O	3.3V	LCD_B7
79	LCDIF_D10	GPIO_B1_3	O	3.3V	LCD_G7
80	GND	GND	PWR	GND	

Table 3: B2B Connector J1 Pin Layout

J2 Pin	Signal Name	i-MXRT1052 Pin	I/O	Voltage	Remarks
1	ETH_TX+	ETH_A_D1P	I/O	3.3V	
2	+5V	+V5S	PWR	5.0V	Power In
3	ETH_TX-	ETH_A_D1N	I/O	3.3V	
4	+5V	+V5S	PWR	5.0V	Power In
5	ETH_RX+	ETH_A_D2P	I/O	3.3V	
6	+5V	+V5S	PWR	5.0V	Power In
7	ETH_RX-	ETH_A_D2N	I/O	3.3V	
8	GND	GND	PWR	GND	
9	NC	X	X	X	
10	GND	GND	PWR	GND	
11	NC	X	X	X	
12	GND	GND	PWR	GND	
13	NC	X	X	X	
14	ACTLED1n	ETH_A_LED	O	3.3V	Pulled Up to VDD_3V3 with 2.49K
15	NC	X	X	X	
16	NC	X	X	X	
17	GND	GND	PWR	GND	
18	JTAG_TCK	JTAG_TCK	O	3.3V	
19	NC	X	X	X	
20	JTAG_TMS	JTAG_TMS	O	3.3V	
21	NC	X	X	X	
22	JTAG_TDI	JTAG_TDI	I	3.3V	
23	NC	X	X	X	
24	JTAG_TDO	JTAG_TDO	O	3.3V	
25	NC	X	X	X	
26	USDHC2_VCC	SD_A_VCC	PWR	1.8/3.3V	
27	NC	X	X	X	
28	GPIO3_1	SD_A_VSEL	I/O	1.8/3.3V	
29	NC	X	X	X	
30	NC	X	X	X	
31	NC	X	X	X	
32	USDHC2_WP	SD_A_WP	I	1.8/3.3V	
33	NC	X	X	X	

J2 Pin	Signal Name	i-MXRT1052 Pin	I/O	Voltage	Remarks
34	USDHC2_CD	SD_A_CD	I	1.8/3.3V	
35	GND	GND	PWR	GND	
36	USDHC2_CMD	SD_A_CMD	O	1.8/3.3V	Pulled Up to USDHC2_VCC with 100K
37	USB_OTG1_VBUS	USB_OTG_VBUS	PWR I/O	5.0V	Power In (Device Mode), Power Out (Host Mode)
38	USDHC2_CLK	SD_A_CLK	O	1.8/3.3V	
39	USB_OTG1_PWR	USB_OTG_PWR	I	3.3V	Pulled Up to VDD_3V3 with 100K
40	USDHC2_D0	SD_A_DATA0	I/O	1.8/3.3V	Pulled Up to USDHC2_VCC with 100K
41	USB_OTG1_ID	USB_OTG_ID	O	3.3V	
42	USDHC2_D1	SD_A_DATA1	I/O	1.8/3.3V	
43	USB_OTG1_DP	USB_OTG_DP	I/O	3.3V	
44	USDHC2_D2	SD_A_DATA2	I/O	1.8/3.3V	
45	USB_OTG1_DN	USB_OTG_DN	I/O	3.3V	
46	USDHC2_D3	SD_A_DATA3	I/O	1.8/3.3V	
47	GND	GND	PWR	GND	
48	VBAT	VBAT	PWR	3.0V	Power In, 2.2V < VBAT < 3.45V
49	NC	X	X	X	
50	VDD_SNVS	VDD_SNVS_IN	PWR	3.3V	Power In
51	NC	X	X	X	
52	VDD_3V3	+3V3_OUT	PWR	3.3V	Power Out, 20mA max
53	NC	X	X	X	
54	RESETIN	RESETIN	O	3.3V	
55	NC	X	X	X	
56	PMIC_STBY	PMIC_STBY	I	3.3V	
57	GND	GND	PWR	GND	
58	NC	X	X	X	
59	USBH1_VBUS	USB_HOST_VBUS	O	5.0V	USB Host Mode Power Supply
60	NC	X	X	X	
61	USBH1_DN	USB_HOST_DN	I/O		
62	NC	X	X	X	
63	USBH1_DP	USB_HOST_DP	I/O		
64	NC	X	X	X	

J2 Pin	Signal Name	i-MXRT1052 Pin	I/O	Voltage	Remarks
65	VDD_3V3	USB_HOST_PWR	PWR	3.3V	Pulled Up to 3.3V with 10K
66	NC	X	X	X	
67	VCC_AUD	AUDIO_A_VCC	O	3.3V	Power Out
68	NC	X	X	X	
69	GND_AUD	AUDIO_A_GND	PWR	GND	
70	PWM1_B	GPIO_SD_B0_05	I/O	3.3V	
71	LINEOUT_L	AUDIO_A_LOUT_L	O		
72	BOOTSEL	BOOTSEL	I/O		Pulled Up to VDD_SNVS with 10K
73	LINEOUT_R	AUDIO_A_LOUT_R	O		
74	GND	GND	PWR	GND	
75	MIC	AUDIO_A_MIC	I		
76	HP_L	AUDIO_A_HP_L	O		
77	LINEIN_L	AUDIO_A_LIN_L	I		
78	HP_R	AUDIO_A_HP_R	O		
79	LINEIN_R	AUDIO_A_LIN_R	I		
80	HP_GND	AUDIO_A_HP_GND	PWR	GND	

Table 4: B2B Connector J2 Pin Layout

4 Interfaces

4.1 Ethernet

On PicoCore™RT1 board there is an Ethernet connection as a standard. Ethernet TX+/- and RX+/- lines are 100 ±20% Ohm differential pairs to a 1:1/1:1 transformer. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm). The transformer midpoint should be connected to the 3.3V power supply. LED signal is able to drive a 3.3V powered LED with 5mA directly to GND. If Ethernet is not used please leave signals unconnected.

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J2-1	ETH1_TX_P	ETH_A_D1P	I/O	Ethernet1 Transmit+
J2-3	ETH1_TX_N	ETH_A_D1N	I/O	Ethernet1 Transmit-
J2-5	ETH1_RX_P	ETH_A_D2P	I/O	Ethernet1 Receive+
J2-7	ETH1_RX_N	ETH_A_D2N	I/O	Ethernet1 Receive-
J2-14	ACTLED1n	ETH_A_LED	O	Ethernet Indicator LED

Table 5: Ethernet Interface

4.2 USB

PicoCore™RT1 provides 1 USB OTG and 1 USB Host Mode connections. The 90 Ohm differential pair of USB signals do not need any termination. For external ports EMV and ESD protection is required nearby the USB connector on the base board. If the USB port is not used please leave open.

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J2-37	USB_OTG1_VBUS	USB_OTG_VBUS	PWR I/O	USB OTG Supply Voltage (+5V)
J2-39	USB_OTG1_PWR	USB_OTG_PWR	I	USB OTG Power On
J2-41	USB_OTG1_ID	USB_OTG_ID	O	USB OTG ID
J2-43	USB_OTG1_P	USB_OTG_DP	I/O	USB OTG Data+
J2-45	USB_OTG1_N	USB_OTG_DN	I/O	USB OTG Data-
J2-59	USB_H1_N	USB_HOST_DN	I/O	USB Host Mode Data-
J2-61	USB_H1_P	USB_HOST_DP	I/O	USB Host Mode Data+
J2-63	USB_H1_VBUS	USB_HOST_VBUS	O	USB Host Mode Supply Voltage (+5V)
J2-65	VDD_3V3	USB_HOST_PWR	I	Pulled Up with 10K

Table 6: USB Interface

4.3 Serial Interfaces

On PicoCore™RT1 board it is allowed for the users to use these serial interfaces, which are given below. All of these serial Interfaces are 3.3V compliant.

- UART: 2 x UART without RTS/CTS (UART1 and UART5) and 1 x UART with RTS/CTS (UART2)
- I2C: 1 x I2C (I2C3)
- SPI: 1 x SPI (SPI1)
- CAN: 2 x CAN2.0 Bus (CAN1 and CAN2)

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J1-6	UART1_RX	UARTA_RXD	I	UART1 Receive Data
J1-8	UART1_TX	UARTA_TXD	O	UART1 Transmit Data
J1-9	UART2_CTS	UARTC_CTS	I	UART2 Clear to Send
J1-11	UART2_RTS	UARTC_RTS	O	UART2 Request to Send
J1-13	UART2_RX	UARTC_RXD	I	UART2 Receive Data
J1-15	UART2_TX	UARTC_TXD	O	UART2 Transmit Data
J1-17	UART5_RX	UARTD_RXD	I	UART5 Receive Data
J1-19	UART5_TX	UARTD_TXD	O	UART5 Transmit Data

Table 7: Serial Interfaces – UART

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J1-10	CAN1_RX	CAN_A_RX	I	CAN1 Bus Receive Data
J1-12	CAN1_TX	CAN_A_TX	O	CAN1 Bus Transmit Data
J1-21	I2C3_SCL	I2C_A_SCL	O	I2C1 Serial Clock Line
J1-23	I2C_SDA	I2C_A_SDA	I/O	I2C1 Serial Data Line
J1-27	CAN2_RX	GPIO_J1_27	I	CAN2 Bus Receive Data
J1-33	CAN2_TX	GPIO_J1_33	O	CAN2 Bus Transmit Data

Table 8: Serial Interfaces – I2C & CAN

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J1-14	GPIO5_3	SPI_A_SS0	O	SPI1 Slave Select
J1-16	SPI1_SDI	SPI_A_MISO	I	SPI1 Serial Data In (Master In Slave Out)
J1-18	SPI1_SDO	SPI_A_MOSI	O	SPI1 Serial Data Out (Master Out Slave In)
J1-20	SPI1_SCK	SPI_A_SCLK	O	SPI1 Serial Clock

Table 9: Serial Interfaces – SPI

4.4 Audio

PicoCore™RT1 board provides stereo analog input and output lines. SGTL5000 is used for the audio codecs. The module also supports digital audio input and outputs over I2S protocol. For mounting option with I2S codec on baseboard please ask our technical support. To avoid ESD and EMV problems, it is necessary to have a protection on the baseboard.

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J2-67	VCC_AUD	AUDIO_A_VCC	PWR O	Audio VCC (+3.3V)
J2-69	GND_AUD	AUDIO_A_GND	PWR	Audio GND
J2-71	LINOUT_L	AUDIO_A_LOUT_L	O	Analog Stereo Line Out Left
J2-73	LINOUT_R	AUDIO_A_LOUT_R	O	Analog Stereo Line Out Right
J2-75	MIC	AUDIO_A_MIC	I	Mic In
J2-76	HP_L	AUDIO_A_HP_L	O	Headphone Out Left
J2-77	LINEIN_L	AUDIO_A_LIN_L	I	Analog Stereo Line In Left
J2-78	HP_R	AUDIO_A_HP_R	O	Headphone Out Right
J2-79	LINEIN_R	AUDIO_A_LIN_R	I	Analog Stereo Line In Right
J2-80	HP_GND	AUDIO_A_HP_GND	PWR	Headphone GND

Table 10: Audio Interface

Optional it is possible to remove Audio Codec and to use SAI Interface.

Signal Name	I2S Option	i.MXRT1052 Pin	Description
LINEIN_R	SAI1_MCLK	SYS_MCLK	I2S System Master Clock
LINEIN_L	SAI1_BCLK	I2S_SCLK	I2S Serial Clock (Bit Clock)
MIC	SAI1_SYNC	I2S_LRCLK	I2S Left-Right Clock (Frame Sync)
HP_R	SAI1_TX_D0	I2S_DIN	I2S Data In
HP_L	SAI1_RX_D0	I2_DOUT	I2S Data Out

Table 11: Audio Interface I2S Option

4.5 SD Card

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org. Pullups have been integrated on the module. Unused signals should be left unconnected.

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J2-26	USDHC2_VCC	SD_A_VCC	PWR O	SD Card Interface Supply Voltage
J2-32	USDHC2_WP	SD_A_WP	I	SD Card Interface Write Protection
J2-34	USDHC2_CD	SD_A_CD	I	SD Card Interface Card Detect
J2-36	USDHC2_CMD	SD_A_CMD	O	SD Card Interface Command
J2-38	USDHC2_CLK	SD_A_CLK	O	SD Card Interface Clock
J2-40	USDHC2_D0	SD_A_DATA0	I/O	SD Card Interface Data Line 0
J2-42	USDHC2_D1	SD_A_DATA1	I/O	SD Card Interface Data Line 1
J2-44	USDHC2_D2	SD_A_DATA2	I/O	SD Card Interface Data Line 2
J2-46	USDHC2_D3	SD_A_DATA3	I/O	SD Card Interface Data Line 3

Table 12: SD Card

4.6 LCD Interface

All signals are working with 3.3V logic level. For all LCD signals we strictly recommend serial resistors nearby the module connector to reduce EMI.

LCD Interface			
B2B Pin	**Signal Name**	**i.MXRT1052 Pin**	**16-bit**
J1-53	LCD_R3	LCDIF_D0	R0
J1-55	LCD_R4	LCDIF_D1	R1
J1-57	LCD_R5	LCDIF_D2	R2
J1-59	LCD_R6	LCDIF_D3	R3
J1-61	LCD_R7	LCDIF_D4	R4
J1-69	LCD_G2	LCDIF_D5	G0
J1-71	LCD_G3	LCDIF_D6	G1
J1-73	LCD_G4	LCDIF_D7	G2
J1-75	LCD_G5	LCDIF_D8	G3
J1-77	LCD_G6	LCDIF_D9	G4
J1-79	LCD_G7	LCDIF_D10	G5
J1-70	LCD_B3	LCDIF_D11	B0
J1-72	LCD_B4	LCDIF_D12	B1
J1-74	LCD_B5	LCDIF_D13	B2
J1-76	LCD_B6	LCDIF_D14	B3
J1-78	LCD_B7	LCDIF_D15	B4
J1-50	LCD_CLK	LCDIF_CLK	LCD Clock
J1-58	LCD_HSYNC	LCDIF_HSYNC	LCD HSYNC
J1-60	LCD_VSYNC	LCDIF_VSYNC	LCD VSYNC
J1-56	LCD_DE	LCDIF_ENABLE	LCD Enable
J1-48	BL_PWM	PWM1_A	Backlight Control
J1-54	VLCD_EN	GPIO3_2	LCD Power Enable

Table 13: LCD Interface Connection

For 18-bit LCD Displays, please use the connection method which is given below.

- **R5 of LCD Display should be connected to R0 of PicoCoreRT1**
- **B5 of LCD Display should be connected to B0 of PicoCoreRT1**

4.7 JTAG

B2B Pin	Signal Name	i.MXRT1052 Pin	I/O	Description
J2-18	JTAG_TCK	GPIO_AD_B0_07	O	JTAG Test Clock
J2-20	JTAG_TMS	GPIO_AD_B0_06	I/O	JTAG Test Mode Select
J2-22	JTAG_TDI	GPIO_AD_B0_09	I	JTAG Test Data In
J2-24	JTAG_TDO	GPIO_AD_B0_10	O	JTAG Test Data Out
J1-25	JTAG_MOD	GPIO_AD_B0_08	I/O	

Table 14: JTAG Interface

- For debug only
- There is no JTAG Connector on PicoCore™RT1 board. JTAG Connector should be assembled on baseboard.
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.8 Power and Power Control Pins

J3 Pin	Signal Name	I/O	Voltage	Description
2 4 6	+V5	I	5.0V	Main Power Supply Input Please refer Electrical characteristic (Ch6)
9	VBAT	I	3V	RTC Battery Input, leave open if not used Please refer Electrical characteristic (Ch6)
50	VDD_SNVS	I	3.3V	SNVS Voltage Input, 3.3V
52	VDD_3V3	O	3.3V	20mA Output from on module DCDC powered from +5V
26	USDHC2_VCC	I	1.8V/3.3V	SDHC Power Input, 1.8V/3.3V
23	USB_OTG_VBUS	I	5.0V	USB OTG Supply Voltage, 5.0V
59	USB_H1_VBUS	I	5.0V	USB Host Mode Supply Voltage, 5.0V
54	RESETIN	I	3.3V	Power On Reset Input, 10K Pull-Up
56	PMIC_STBY	O	3.3V	
	GND		GND	Connect all GND pins to a GND plane

Table 15: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory.

VDD_SNVS could be powered separately in special secure Non-Volatile Storage schemes. In normal usage just tie to 3.3V.

3.3V is the DCDC power supply of the module powered from +V5. Use as enable for baseboard power regulators.

RESETIN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On module DCDCs will not get a reset. On power fail VIN has to be switched off and on to avoid latch-up effects.

PMIC_STBY is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

5 RTC

There is a NXP PCA8565 or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

6 Electrical characteristic

6.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V

OVDD: On Board VDD +3.3V for PicoCore™RT1

Table 16: Absolute Maximum Ratings

6.2 DC Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{IN}	PicoCore™RT1 Input Supply Voltage	3.8	5.5	V
V_{BAT}	RTC Power Supply	0.9	5.5	V
USB_OTG_VBUS	USB Supply voltage	4.4	5.5	V
I_{VBUS}	USB Supply Current		100	mA
USDHC2_VCC	SDHC Supply Voltage	1.65	3.6	V
I_{USDHC4}	SDHC Control Supply Current		25	mA
VDD_SNVS	SNVS Supply Voltage	2.4	3.3	V
V_{ih}	High Level Input Voltage	0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage	0	0.3*OVDD	V
V_{oh}	High Level Output Voltage (I_{oh}=0.1mA)	OVDD-0.15		V
V_{il}	Low Level Output Voltage (I_{oh}=0.1mA)		0.15	V
I_o	Output Current IO's (V_{GPIO}=3.3V)		5	mA

Table 17: DC Electrical Characteristics

7 Thermal Specification

Parameter	Min	Typ.	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MXRT1052	0		+95	°C
Junction temperature i.MXRT1052 (“I”) [2]	-40		+105	°C
Junction to Top of i.MXRT1052 (Psi-JT)[3]		0,6		°C/W

Table 18: Thermal Specifications

[1] Depending on cooling solution. See also: *Power consumption and cooling*

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2. Valid for 14x14mm package.

8 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

9 ESD and EMI Implementation

Because there is no connector to „out of case" there is no ESD protection for any interface. It needs ESD protection on every connector out of the case on your baseboard. To reduce EMI the PicoCOMA7™ supports Spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

A helpful guide is available from TI; just search for slva680 at ti.com.

10 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

11 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **should not exceed the maximum operating temperature of the board**.

The maximum power consumption of the board could be 5.5 Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Dependent from your application and your worst-case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend measuring this with your application. We see values between one and max. 3.5 Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet (VK package starting page 27)

- i.MX6RT1 C-Temp CPU datasheet from NXP
- i.MX6RT1 I-Temp CPU datasheet from NXP
- AN12170 from NXP: i.MXRT1050 Product Lifetime Usage Estimates
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

12 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

13 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

14 Packaging

All F&S ESD-sensitive products will shipping either in trays or in bags.
These modules ship in trays. One tray can hold 20 boards. An empty tray will be used as top cover.

15 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

16 Appendix

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17 Content