Hardware Documentation

PicoCore™MX6UL100
for HW Revision 1.10

Version 005
(22-08-24)

Elektronik Systeme

Untere Waldplätze 23
D-70569 Stuttgart
+49(0)711-123722-0
www.fs-net.de

About This Document

This document describes how to use the PicoCore™MX6UL100 board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Attention: Please also note the circuit diagram of our Baseboard reference design.

https://fs-net.de/assets/download/docu/PicoCore/PicoCoreBBDSI_eng.pdf

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
11.05.2021	001	All	A	-	Initial Version	MD
07.07.2021	002	All	M A	4.8.1 4.1	Correction on the RGB Pin layout table Important Note for USB Host Data Signals	MD
29.07.2021	003	All	A M A A	- 4.1 4.3 3.1	New Hardware Version 1.10 Problem on USB Host Data signals solved Update on SPI Interface chapter Two New GPIOs	MD
02.11.2021	004	All	M M M M	4.1 4.7 10,14 2.1	USB_HOST_PWR signal name is corrected in table 3 Missing line is added in table 12 Thermal specifications are updated SMT Steel Spacer section is updated	MD
24.08.2022	005	All	M	-	Update to first official version	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

About This Document 2

ESD Requirements 2

History 2

Table of Contents 3

1 Block diagram 5

2 Mechanical Dimension 6

2.1 SMT Steel Spacer 8

3 Interface and signal description 9

3.1 B2B connectors 9

4 Interfaces 17

4.1 USB OTG & Host 17

4.2 SD Card Interface A 19

4.3 SPI Interface 21

4.4 I2C Interface 22

4.5 Serial Interface (UART) 23

4.6 Ethernet 24

4.6.1 Ethernet RMII Interface 24

4.6.2 Ethernet Interface with 1x PHY 26

4.6.3 Ethernet Interface with 2x PHY 27

4.7 Audio 29

4.8 Display 31

4.8.1 18-bit RGB 31

4.8.2 LVDS 32

4.9 CAN Interface 33

4.10 WLAN/BT Interface 33

4.11 GPIOs 34

4.12 JTAG 34

5 Flash 35

5.1 NAND Flash 35

5.2 eMMC 35

5.3 EEPROM 35

6 RTC 36

7 Secure Authenticator IC 36

8 Power and Power Control Contacts 37

9 Electrical characteristic 38

9.1 Absolute maximum ratings 38

9.2 DC Electrical Characteristics 38
10 Thermal Specification 39
11 Review service 40
12 ESD and EMI implementing on COM 40
13 Second Source Rules 40
14 Power Consumption and Cooling 41
15 Storage Conditions 42
16 ROHS and REACH statement 42
17 Packaging 42
18 Matrix Code Sticker 42
19 Appendix 43
Important Notice 43
Warranty Terms 44
20 Content 45

1 Block diagram

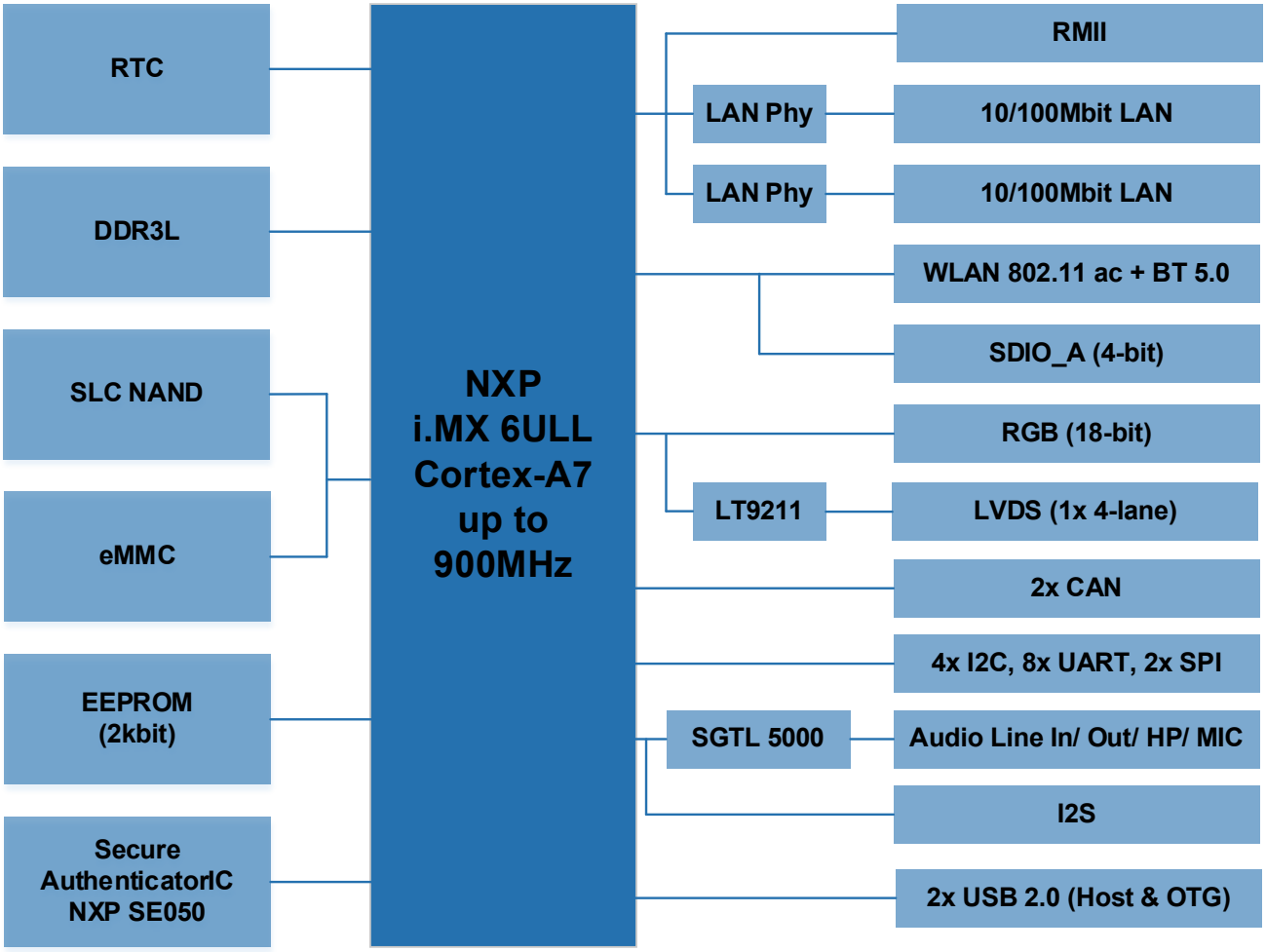
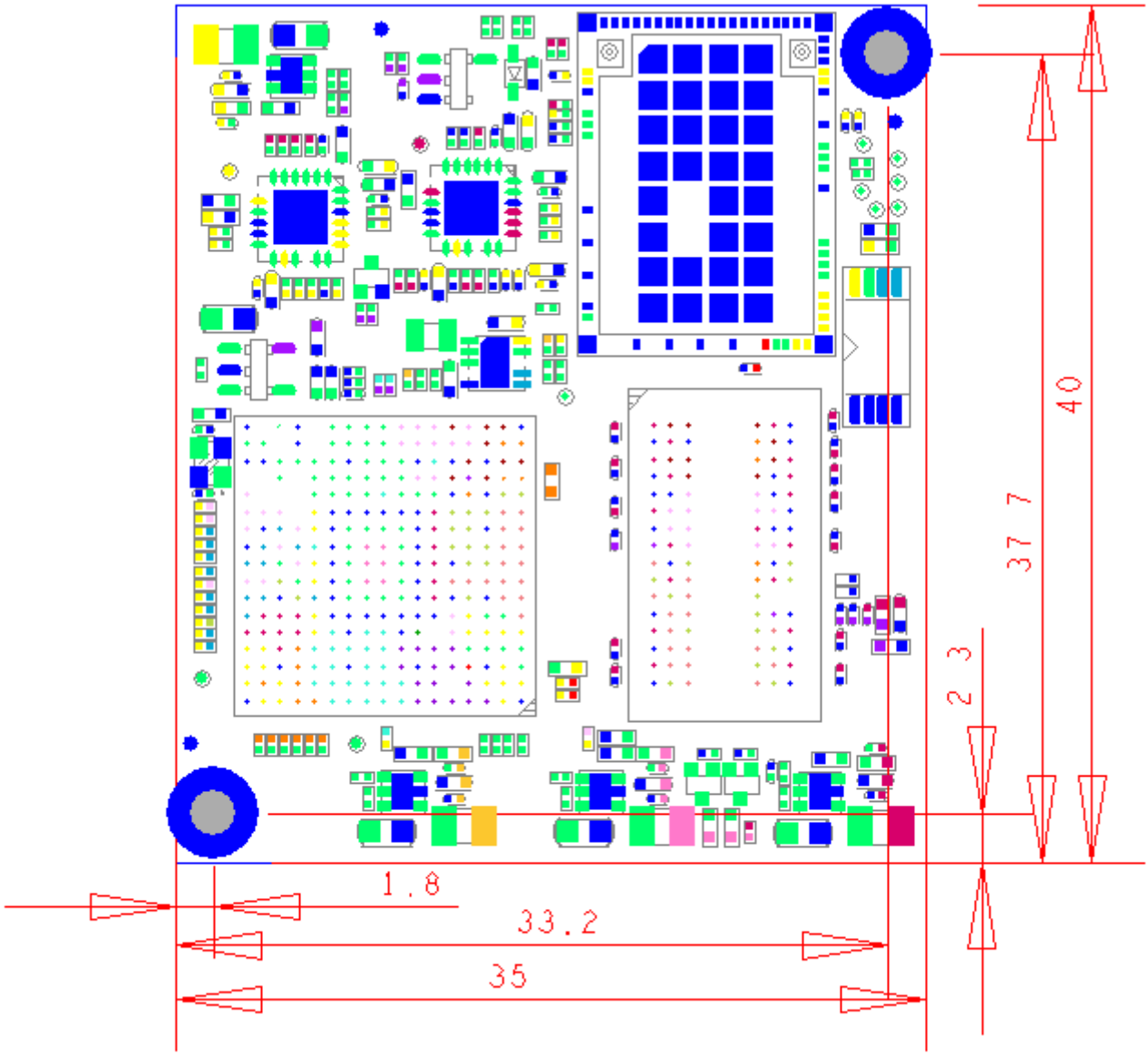


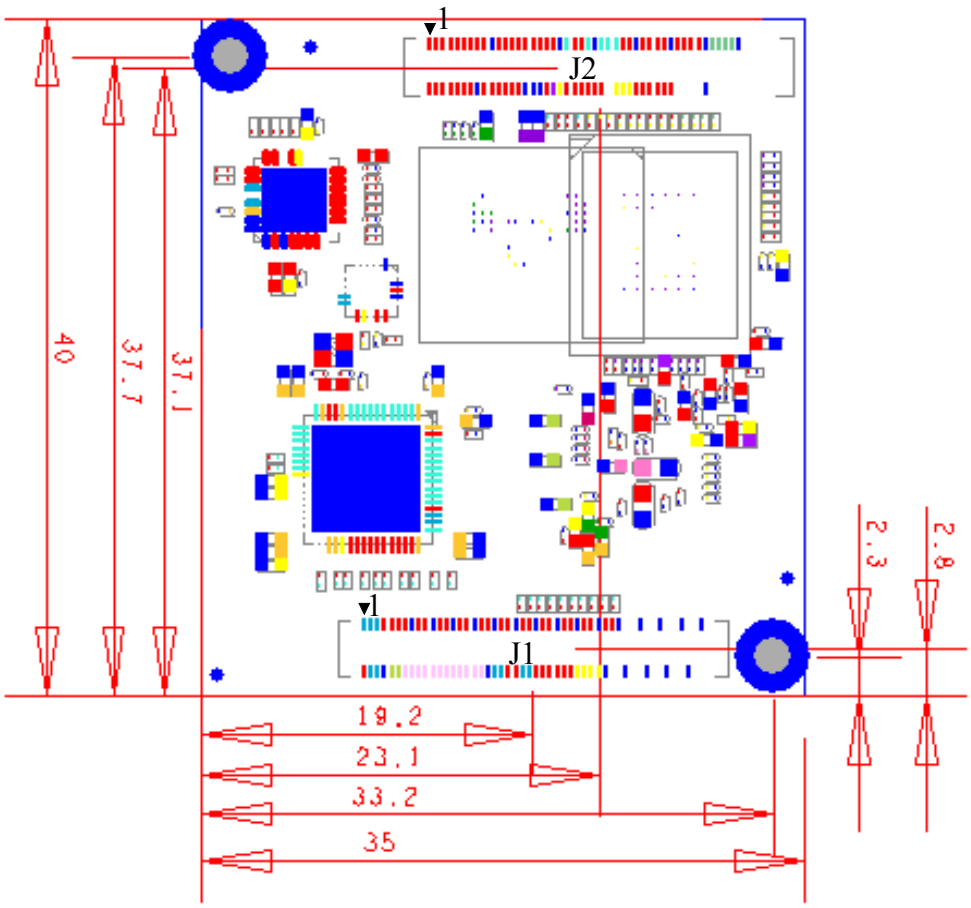
Figure 1: Block Diagram

2 Mechanical Dimension



*All dimensions are in mm

Figure 2: Mechanical Dimension Top



*All dimensions are in mm

Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 3mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer components, order number B.MSCHR.22. This part is in F&S stock and can be ordered via F&S web shop.

The stack height of the space is 1.5mm. If a different stack height is needed, another spacer should be chosen.

Data sheet and 3D model (STP) is available on our website.

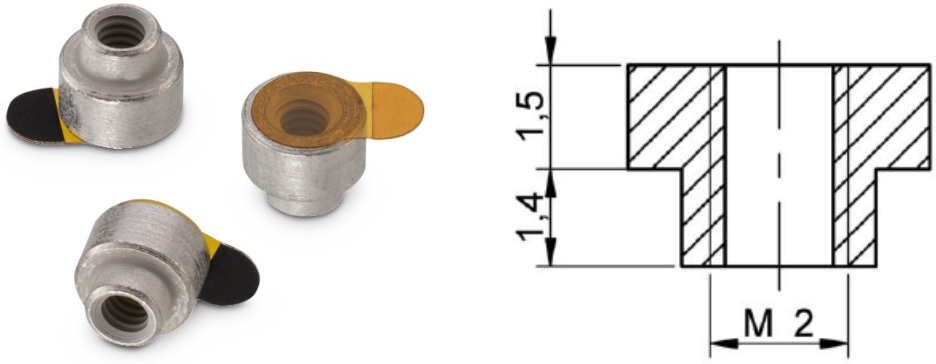


Figure 4: SMT Steel Spacer

3 Interface and signal description

3.1 B2B connectors

PicoCoreMX6UL100 is using two 100 pin connectors from manufacturer Hirose.

Part number: DF40C-100DP-0.4V

Part number counterpart: DF40C-100DS-0.4V

With this combination you get minimal stacking height of 1,5mm. Another possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered in web shop.

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J1	1	I2C_B_IRQ	GPIO_IO01	I	3.3V	I2C_B Interrupt Request
J1	2	GPIO_J1_2	LCD_DATA23	I/O	3.3V	Standard GPIO
J1	3	I2C_B_SCL	UART1_TX_DATA	O	3.3V	I2C_B Serial Clock
J1	4	I2C_A_SCL	UART4_TX_DATA	O	3.3V	I2C_A Serial Clock
J1	5	I2C_B_SDA	UART1_RX_DATA	I/O	3.3V	I2C_B Serial Data
J1	6	I2C_A_SDA	UART4_RX_DATA	I/O	3.3V	I2C_A Serial Data
J1	7	GPIO_J1_7	LCD_DATA22	I/O	3.3V	Standard GPIO
J1	8	GND		PWR	GND	
J1	9	BL_ON	SNVS_TAMPER4	O	3.3V	Backlight enable
J1	10	CAN_A_RX	UART3_RTS	I	3.3V	CAN_A Data Receive
J1	11	BL_PWM	CSI_VSYNC	O	3.3V	Backlight PWM
J1	12	CAN_A_TX	UART3_CTS	O	3.3V	CAN_A Data Transmit
J1	13	VLCD_ON	SNVS_TAMPER5	O	3.3V	VLCD enable
J1	14	UART_A_RTS	UART1_CTS	O	3.3V	UART_A Ready to Send
J1	15	GND		PWR	GND	
J1	16	UART_A_CTS	UART1_RTS	I	3.3V	UART_A Clear to Send
J1	17	DSI_A_CLK_P	MLTXA_M1LCP LCD_DATA05	O O	- 3.3V	LVDS Clock+ LCD Data 5
J1	18	UART_A_RXD	GPIO_IO03	I	3.3V	UART_A Data Receive
J1	19	DSI_A_CLK_N	MLTXA_M1LCN LCD_DATA04	O O	- 3.3V	LVDS Clock- LCD Data 4
J1	20	UART_A_TXD	GPIO_IO02	O	3.3V	UART_A Data Transmit
J1	21	GND		PWR	GND	
J1	22	UART_B_RTS	GPIO_IO09	O	3.3V	UART_B Ready to Send
J1	23	DSI_A_DATA0_P	MLTXA_M3L0P	O	-	LVDS Data 0+

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
			LCD_ENABLE	O	3.3V	LCD Enable
J1	24	UART_B_CTS	GPIO_IO08	I	3.3V	UART_B Clear to Send
J1	25	DSI_A_DATA0_N	MLTXA_M3L0N LCD_CLK	O O	- 3.3V	LVDS Data 0- LCD Clock
J1	26	UART_B_RXD	GPIO_IO05	I	3.3V	UART_B Data Receive
J1	27	GND		PWR	GND	
J1	28	UART_B_TXD	GPIO_IO04	O	3.3V	UART_B Data Transmit
J1	29	DSI_A_DATA1_P	MLTXA_M2L1P LCD_DATA01	O O	- 3.3V	LVDS Data 1+ LCD Data 1
J1	30	UART_C_RXD	UART3_RX_DATA	I	3.3V	UART_C Data Receive
J1	31	DSI_A_DATA1_N	MLTXA_M2L1N LCD_DATA00	O O	- 3.3V	LVDS Data 1- LCD Data 0
J1	32	UART_C_TXD	UART3_TX_DATA	O	3.3V	UART_C Data Transmit
J1	33	GND		PWR	GND	
J1	34	UART_D_RXD	CSI_PIXCLK	I	3.3V	UART_D Data Receive
J1	35	DSI_A_DATA2_P	MLTXA_MCL2P LCD_DATA03	O O	- 3.3V	LVDS Data 2+ LCD Data 3
J1	36	UART_D_TXD	CSI_MCLK	O	3.3V	UART_D Data Transmit
J1	37	DSI_A_DATA2_N	MLTXA_MCL2N LCD_DATA02	O O	- 3.3V	LVDS Data 2- LCD Data 2
J1	38	GND		PWR	GND	
J1	39	GND		PWR	GND	
J1	40	I2C_C_SCL	UART2_TX_DATA	O	3.3V	I2C_C Serial Clock
J1	41	DSI_A_DATA3_P	MLTXA_M0L3P LCD_DATA07	O O	- 3.3V	LVDS Data 3+ LCD Data 7
J1	42	I2C_C_SDA	UART2_RX_DATA	I/O	3.3V	I2C_C Serial Data
J1	43	DSI_A_DATA3_N	MLTXA_M0L3N LCD_DATA06	O O	- 3.3V	LVDS Data 3- LCD Data 6
J1	44	GPIO_J1_44	UART2_CTS	I/O	3.3V	Standard GPIO
J1	45	GND		PWR	GND	
J1	46	GPIO_J1_46	UART2_RTS	I/O	3.3V	Standard GPIO
J1	47	DSI_B_CLK_P	LCD_DATA15	O	3.3V	LCD Data 15
J1	48	I2C_D_SCL	UART5_TX_DATA	O	3.3V	I2C_D Serial Clock
J1	49	DSI_B_CLK_N	LCD_DATA14	O	3.3V	LCD Data 14
J1	50	I2C_D_SDA	UART5_RX_DATA	I/O	3.3V	I2C_D Serial Data

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J1	51	GND		PWR	GND	
J1	52	GPIO_J1_52	LCD_HSYNC	I/O	3.3V	LCD HSYNC [GPIO]
J1	53	DSI_B_DATA0_P	LCD_DATA09	O	3.3V	LCD Data 9
J1	54	GPIO_J1_54	LCD_VSYNC	I/O	3.3V	LCD VSYNC [GPIO]
J1	55	DSI_B_DATA0_N	LCD_DATA08	O	3.3V	LCD Data 8
J1	56	SPI_B_SS0	CSI_DATA_05	I/O	3.3V	SPI_B Slave Select
J1	57	GND		PWR	GND	
J1	58	SPI_B_MISO	CSI_DATA_07	I/O	3.3V	SPI_B Master In Slave Out
J1	59	DSI_B_DATA1_P	LCD_DATA11	O	3.3V	LCD Data 11
J1	60	SPI_B_MOSI	CSI_DATA_06	I/O	3.3V	SPI_B Master Out Slave In
J1	61	DSI_B_DATA1_N	LCD_DATA10	O	3.3V	LCD Data 10
J1	62	SPI_B_SCLK	CSI_DATA_04	I/O	3.3V	SPI_B Serial Clock
J1	63	GND		PWR	GND	
J1	64	SPI_A_SS0	CSI_DATA_01	I/O	3.3V	SPI_A Slave Select
J1	65	DSI_B_DATA2_P	LCD_DATA13	O	3.3V	LCD Data 13
J1	66	SPI_A_MISO	CSI_DATA_03	I/O	3.3V	SPI_A Master In Slave Out
J1	67	DSI_B_DATA2_N	LCD_DATA12	O	3.3V	LCD Data 12
J1	68	SPI_A_MOSI	CSI_DATA_02	I/O	3.3V	SPI_A Master Out Slave In
J1	69	GND		PWR	GND	
J1	70	SPI_A_SCLK	CSI_DATA_00	I/O	3.3V	SPI_A Serial Clock
J1	71	DSI_B_DATA3_P	LCD_DATA17	O	3.3V	LCD Data 17
J1	72	GND		PWR	GND	
J1	73	DSI_B_DATA3_N	LCD_DATA16	O	3.3V	LCD Data 16
J1	74	N.C.	X	X	X	Not Connected
J1	75	GND		PWR	GND	
J1	76	N.C.	X	X	X	Not Connected
J1	77	N.C.	X	X	X	Not Connected
J1	78	GND		PWR	GND	
J1	79	N.C.	X	X	X	Not Connected
J1	80	N.C.	X	X	X	Not Connected
J1	81	GND		PWR	GND	
J1	82	N.C.	X	X	X	Not Connected
J1	83	N.C.	X	X	X	Not Connected
J1	84	GND		PWR	GND	
J1	85	N.C.	X	X	X	Not Connected

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J1	86	N.C.	X	X	X	Not Connected
J1	87	GND		PWR	GND	
J1	88	N.C.	X	X	X	Not Connected
J1	89	N.C.	X	X	X	Not Connected
J1	90	GND		PWR	GND	
J1	91	N.C.	X	X	X	Not Connected
J1	92	N.C.	X	X	X	Not Connected
J1	93	GND		PWR	GND	
J1	94	N.C.	X	X	X	Not Connected
J1	95	N.C.	X	X	X	Not Connected
J1	96	GND		PWR	GND	
J1	97	N.C.	X	X	X	Not Connected
J1	98	N.C.	X	X	X	Not Connected
J1	99	GND		PWR	GND	
J1	100	N.C.	X	X	X	Not Connected
J2	1	ETH_A_D1P	TXP (PHY1) GPIO1_IO07	I/O I/O	3.3V 3.3V	Ethernet A Data1+ ENET_MDC
J2	2	AUDIO_A_VCC		PWR	3V	Audio_A Supply Voltage
J2	3	ETH_A_D1N	TXM (PHY1) GPIO1_IO06	I/O I/O	3.3V 3.3V	Ethernet A Data1- ENET_MDIO
J2	4	AUDIO_A_GND		PWR	GND	Audio_A GND
J2	5	ETH_A_D2P	RXP (PHY1) ENET1_TX_EN	I/O I/O	3.3V 3.3V	Ethernet A Data2+ ENET1 RMII TX Enable
J2	6	AUDIO_A_LOUT_L	LOUT JTAG_TDI	O O	- 3.3V	Audio_A Line-Out left I2S SCLK
J2	7	ETH_A_D2N	RXM (PHY1) N.C.	I/O X	3.3V X	Ethernet A Data2- Not Connected
J2	8	AUDIO_A_LOUT_R	ROUT JTAG_TDO	O O	- 3.3V	Audio_A Line-Out right I2S LRCLK
J2	9	ETH_A_D3P	ENET1_TX_DATA0	I/O	3.3V	ENET1 RMII TX Data0
J2	10	AUDIO_A_MIC	MICIN (Codec) N.C.	I X	- X	Audio_A Microphone-In Not Connected
J2	11	ETH_A_D3N	ENET1_TX_DATA1	I/O	3.3V	ENET1 RMII TX Data1

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J2	12	AUDIO_A_LIN_L	LLINEIN (Codec) JTAG_TMS	I O	- 3.3V	Audio_A Line-In left I2S MCLK
J2	13	ETH_A_D4P	ENET1_TX_CLK	I/O	3.3V	ENET1 RMII TX Clock
J2	14	AUDIO_A_LIN_R	RLINEIN N.C.	I X	- X	Audio_A Line-In right Not Connected
J2	15	ETH_A_D4N	N.C.	X	X	Not Connected
J2	16	GND		PWR	GND	
J2	17	ETH_A_LED	LED0 (PHY1)	O	3.3V	Ethernet A Activity LED
J2	18	AUDIO_A_HP_L	LHPOUT (Codec) JTAG_TRST	O O	- 3.3V	Audio_A Headphone left I2S DOUT
J2	19	GND		PWR	GND	
J2	20	AUDIO_A_HP_R	RHPOUT (Codec) JTAG_TCK	O I	- 3.3V	Audio_A Headphone right I2S_DIN
J2	21	ETH_B_LED	LED0 (PHY2)	O	3.3V	Ethernet B Activity LED
J2	22	AUDIO_A_HP_GND		PWR		Audio_A Headphone GND
J2	23	ETH_B_D1P	TXP (PHY2) ENET1_RX_EN	I/O I/O	1.2V 3.3V	Ethernet B Data1+ ENET1 RMII CRS_DV
J2	24	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	25	ETH_B_D1N	TXM (PHY2) ENET1_RX_ER	I/O I/O	1.2V 3.3V	Ethernet B Data1- ENET1 RMII RX_ER
J2	26	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	27	ETH_B_D2P	RXP (PHY2) ENET1_RX_DATA0	I/O I/O	1.2V 3.3V	Ethernet B Data2+ ENET1 RMII RX Data0
J2	28	VDD_VIN		PWR	5.0V	Supply Voltage Input
J2	29	ETH_B_D2N	RXM (PHY2) ENET1_RX_DATA1	I/O I/O	1.2V 3.3V	Ethernet B Data2- ENET1 RMII RX Data1
J2	30	GND		PWR	GND	
J2	31	ETH_B_D3P	N.C.	X	X	Not Connected
J2	32	GND		PWR	GND	
J2	33	ETH_B_D3N	N.C.	X	X	Not Connected
J2	34	GND		PWR	GND	
J2	35	ETH_B_D4P	SNVS_TAMPER2	I/O	3.3V	ENET PHY Interrupt Request
J2	36	VDD_VBAT		PWR	~3V	RTC battery Input
J2	37	ETH_B_D4N	SNVS_TAMPER0	I/O	3.3V	ENET1 PHY Reset

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J2	38	RESERVED	X	X	X	Please leave this pin open
J2	39	GND		PWR	GND	
J2	40	VDD_3V3		O	3.3V	20mA output from on module DCDC powered from VIN
J2	41	USB_HOST_VBUS	USB_OTG2_VBUS	I	5.0V	USB Host Supply Voltage
J2	42	RESETINN		I	3.3V	Power on reset Input; onboard Pull-up 10k
J2	43	USB_HOST_DP	USB_OTG2_DP	I/O		USB Host Data+
J2	44	PMIC_STBY	CCM_PMIC_STBY_REQ	O	3.3V	PMIC Standby onboard Pull-up 10k
J2	45	USB_HOST_DN	USB_OTG2_DN	I/O		USB Host Data-
J2	46	PMIC_ON_REQ	SNVS_PMIC_ON_REQ	O	3.3V	PMIC On Request
J2	47	USB_HOST_PWR	SNVS_TAMPER8	O	3.3V	USB Host Power Enable
J2	48	ON_OFF		I	3.3V	On/Off Input for CPU
J2	49	GND		PWR	GND	
J2	50	BOOTSEL		I	3.3V	Service jumper; normally left open
J2	51	USB_OTG_VBUS	USB_OTG1_VBUS	I	5.0V	USB OTG Supply Voltage
J2	52	SD_A_VCC		O	1.8V / 3.3V	SD_A Supply Voltage Selectable via Jumper
J2	53	USB_OTG_PWRn	SNVS_TAMPER9	O	3.3V	USB OTG Power Enable
J2	54	RESERVED	X	X	X	Please leave this pin open
J2	55	USB_OTG_ID	GPIO1_IO00	I	3.3V	USB OTG ID
J2	56	SD_A_RST	CSI_DATA06	O	3.3V	SD_A Reset
J2	57	USB_OTG_DP	USB_OTG1_DP	I/O		USB OTG Data+
J2	58	SD_A_WP	CSI_DATA04	O	3.3V	SD_A Write Protect
J2	59	USB_OTG_DN	USB_OTG1_DN	I/O		USB OTG Data-
J2	60	SD_A_CD	CSI_DATA05	I	3.3V	SD_A Card Detect
J2	61	GND		PWR	GND	
J2	62	SD_A_CMD	SD1_CMD	I/O	SD_A_VCC	SD_A Command
J2	63	PWM	CSI_HSYNC	O	3.3V	PWM Output
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	SD_A Clock
J2	65	GPIO_J2_65	LCD_DATA21	I/O	3.3V	Standard GPIO
J2	66	SD_A_DATA0	SD1_DATA0	I/O	SD_A_VCC	SD_A Data0

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J2	67	GPIO_J2_67	LCD_DATA20	I/O	3.3V	Standard GPIO
J2	68	SD_A_DATA1	SD1_DATA1	I/O	SD_A_VCC	SD_A Data1
J2	69	GPIO_J2_69	SNVS_TAMPER1	I/O	3.3V	ENET2 PHY Reset
J2	70	SD_A_DATA2	SD1_DATA2	I/O	SD_A_VCC	SD_A Data2
J2	71	GND		PWR	GND	
J2	72	SD_A_DATA3	SD1_DATA3	I/O	SD_A_VCC	SD_A Data3
J2	73	GPIO_J2_73	ENET2_RX_DATA1	I/O	3.3V	ENET2 RMII RX Data1
J2	74	N.C.	X	X	X	Not Connected
J2	75	GPIO_J2_75	ENET2_RX_DATA0	I/O	3.3V	ENET2 RMII RX Data0
J2	76	N.C.	X	X	X	Not Connected
J2	77	GPIO_J2_77	ENET2_RX_EN	I/O	3.3V	ENET2 RMII CRS_DV
J2	78	N.C.	X	X	X	Not Connected
J2	79	GPIO_J2_79	ENET2_TX_DATA0	I/O	3.3V	ENET2 RMII TX Data0
J2	80	N.C.	X	X	X	Not Connected
J2	81	GND		PWR	GND	
J2	82	GND		PWR	GND	
J2	83	SPI_C_SS0	ENET2_RX_ER	O	3.3V	ENET2 RMII RX_ER SPI_C Slave Select
J2	84	N.C.	X	X	X	Not Connected
J2	85	SPI_C_MISO	ENET2_TX_CLK	I	3.3V	ENET2 RMII TX Clock SPI_C Master In Slave Out
J2	86	N.C.	X	X	X	Not Connected
J2	87	SPI_C_MOSI	ENET2_TX_EN	O	3.3V	ENET2 RMII TX Enable or SPI_C Master Out Slave In
J2	88	N.C.	X	X	X	Not Connected
J2	89	SPI_C_SCLK	ENET2_TX_DATA1	O	3.3V	ENET2 RMII TX Data1 or SPI_C Serial Clock
J2	90	N.C.	X	X	X	Not Connected
J2	91	GND		PWR	GND	
J2	92	N.C.	X	X	X	Not Connected
J2	93	JTAG_TCK	JTAG_TCK	I	3.3V	JTAG Test Clock
J2	94	GPIO_J2_94	LCD_DATA18	I/O	3.3V	Standard GPIO
J2	95	JTAG_TMS	JTAG_TMS	I	3.3V	JTAG Test Mode Select
J2	96	GPIO_J2_96	LCD_DATA19	I/O	3.3V	Standard GPIO
J2	97	JTAG_TDI	JTAG_TDI	I	3.3V	JTAG Test Data In

	Pin	Signal	CPU Pad	I/O	Voltage	Description / Function
J2	98	N.C.	X	X	X	Not Connected
J2	99	JTAG_TDO	JTAG_TDO	O	3.3V	JTAG Test Data Out
J2	100	N.C.	X	X	X	Not Connected

Table 2: B2B connector

4 Interfaces

4.1 USB OTG & Host

PicoCoreMX6UL100 module can support 1x USB HOST (2.0) and 1x USB OTG (2.0).

The 90 Ohm differential pair of USB signals do not need any termination.

For external ports ESD and EMI protection is required nearby the USB connectors.

If the USB OTG will be used in Host Mode, **USB_OTG_ID** Pin must be connected to GND with a resistor. Otherwise it must be directly connected to the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	41	USB_HOST_VBUS	USB_OTG2_VBUS	I	5.0V	Input; USB voltage detection
J2	43	USB_HOST_DP	USB_OTG2_DP	I/O		90 Ohm differential pair
J2	45	USB_HOST_DN	USB_OTG2_DN	I/O		
J2	47	USB_HOST_PWR	SNVS_TAMPER8	O	3.3V	Power enable; onboard pull-up 100k
J2	51	USB_OTG_VBUS	USB_OTG1_VBUS	I	5.0V	Input; USB voltage detection
J2	53	USB_OTG_PWRn	SNVS_TAMPER9	O	3.3V	Power enable; onboard pull-Up 100k
J2	55	USB_OTG_ID	GPIO1_IO00	I	3.3V	
J2	57	USB_OTG_DP	USB_OTG1_DP	I/O		90 Ohm differential pair
J2	59	USB_OTG_DN	USB_OTG1_DN	I/O		

Table 3: USB OTG & Host Interface Connections

Important Note:

On the first revision (Rev. 1.00) of the PicoCoreMX6UL100 module the USB_HOST Data Lanes (USB_HOST_DN and USB_HOST_DP) are swapped and connected incorrectly on the B2B connector. To prevent any potential redesigns in the future, it is highly recommended to cross these signals into correct form on the baseboard with 0R jumper resistors or ferrite beads. So that the baseboard will also be compatible with the corrected redesign of the PicoCore module. Please see figure 6 for the recommended solution.

This problem is corrected on the HW Version 1.10.

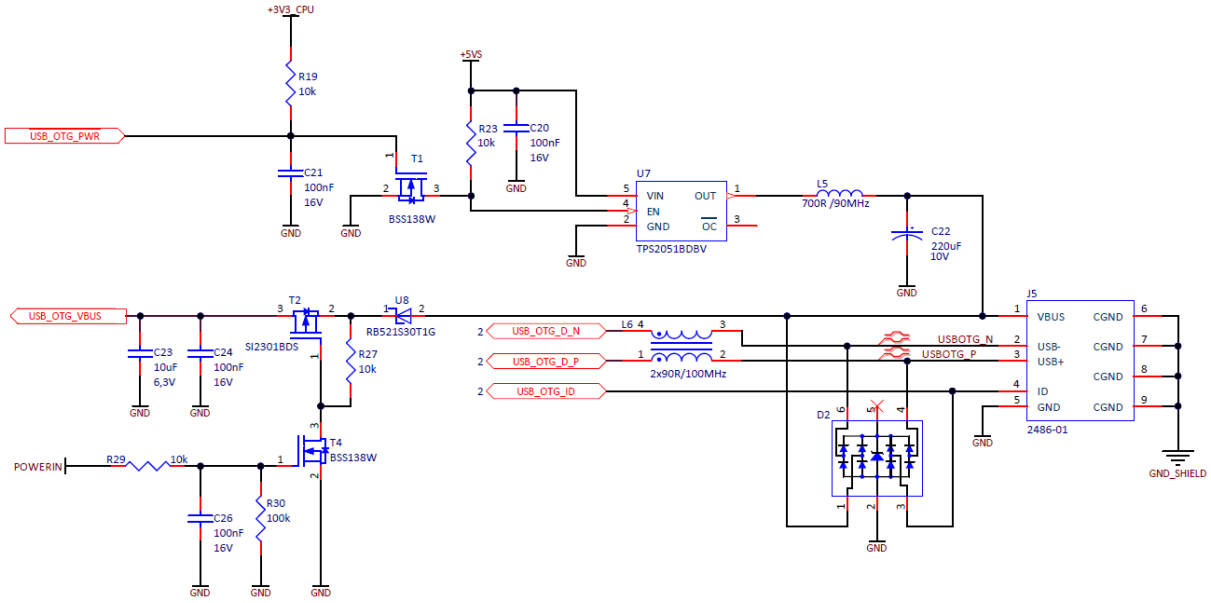


Figure 5: USB OTG example connection

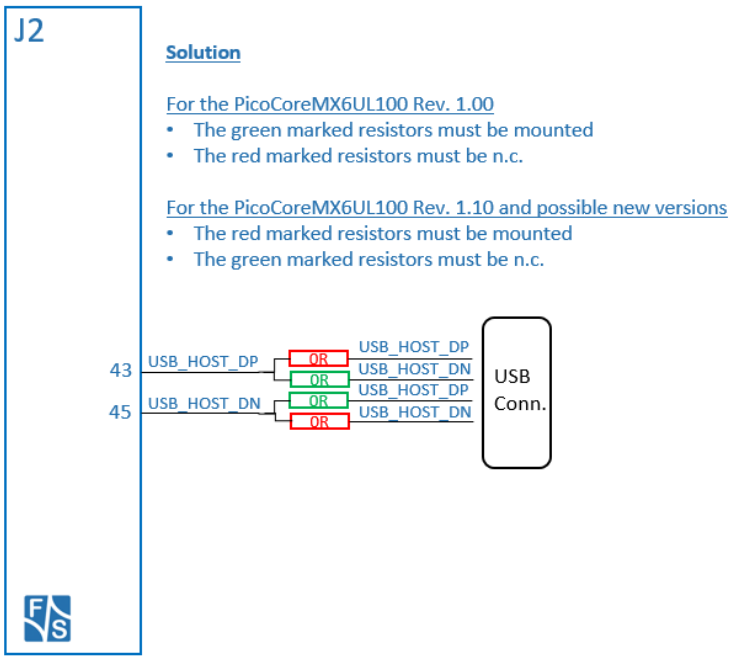


Figure 6: Recommended Solution for swapped USB Data Signals

4.2 SD Card Interface A

This interface supports 4bit SD interface. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

SD_A_VCC can be 1.8V or 3.3V. The voltage level is configured via jumper resistors. In the standard configuration SD_A_VCC comes at 3.3V voltage level.

SD_A Interface is shared with WLAN/BT. If the WLAN/BT Module is mounted, there is no SD Card interface available on module.

Signals *SD_A_RST*, *SD_A_WP* and the *SD_A_CD* are shared with SPI_B Pins. These pins are only available if the WLAN/BT module is not mounted on board.

Please contact us for the right jumper configuration.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J2	52	SD_A_VCC	NVCC_SD1	O	1.8V / 3.3V	Power supply out for external SDIO interface
J2	54	RESERVED	RESERVED	X	X	Please leave this pin open!
J2	56	SD_A_RST	CSI_DATA06	O	3.3V	Active low reset No pull-up/downs on module Shared with SPI_B_MOSI
J2	58	SD_A_WP	CSI_DATA04	I	3.3V	Active low write protect disable No pull-up/downs on module Shared with SPI_B_SCLK
J2	60	SD_A_CD	CSI_DATA05	I	3.3V	Active low card detect No pull-up/downs on module Shared with SPI_B_SS0
J2	62	SD_A_CMD	SD1_CMD	O	SD_A_VCC	onboard Pull-Up 100k
J2	64	SD_A_CLK	SD1_CLK	O	SD_A_VCC	
J2	66	SD_A_DATA 0	SD1_DATA0	I/O	SD_A_VCC	onboard Pull-Up 100k
J2	68	SD_A_DATA 1	SD1_DATA1	I/O	SD_A_VCC	
J2	70	SD_A_DATA 2	SD1_DATA2	I/O	SD_A_VCC	
J2	72	SD_A_DATA 3	SD1_DATA3	I/O	SD_A_VCC	

Table 4: SD Card Interface A

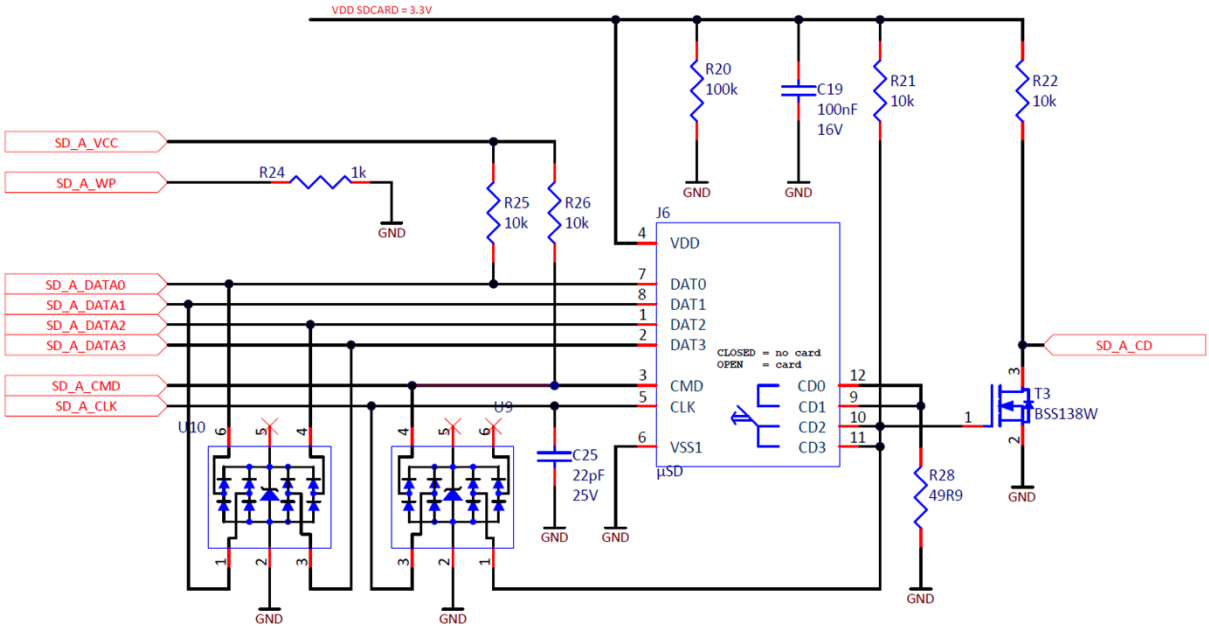


Figure 7: SD Card Connector example connection

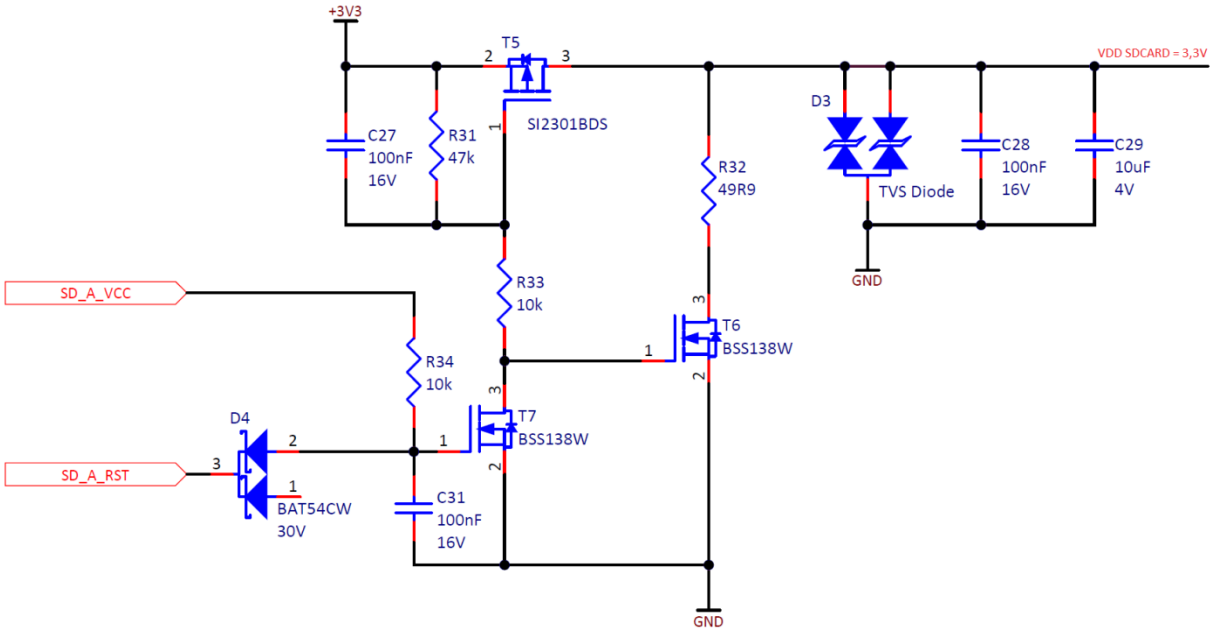


Figure 8: SD_A supply voltage switching circuit

4.3 SPI Interface

The module support Hi-Speed SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage levels need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

Note1:
SPI_B is shared with some of the SD_A signals (SD_A_WP, SD_A_RST and SD_A_CD). If board is configured for SD_A, SPI_B pins have no connection at the B2B connector.
Please contact us for more information.

Note2:
SPI_C is optional with Ethernet B signals. SPI_C Pins can only be used if there is only one Physical Ethernet (Ethernet_A) mounted on the board. Otherwise these pins are used for the Ethernet_B

Please contact us for more information.

	Pin	Signal	CPU Pad	SM*1	MM*1	Voltage	Remarks
SPI_A							
J1	64	SPI_A_SS0	CSI_DATA01	I	O	3.3V	ECSPI2_SS0
J1	66	SPI_A_MISO	CSI_DATA03	O	I	3.3V	ECSPI2_MISO
J1	68	SPI_A_MOSI	CSI_DATA02	I	O	3.3V	ECSPI2_MOSI
J1	70	SPI_A_SCLK	CSI_DATA00	I	O	3.3V	ECSPI2_SCLK
SPI_B							
J1	56	SPI_B_SS0	CSI_DATA05	I	O	3.3V	ECSPI1_SS0
J1	58	SPI_B_MISO	CSI_DATA07	O	I	3.3V	ECSPI1_MISO
J1	60	SPI_B_MOSI	CSI_DATA06	I	O	3.3V	ECSPI1_MOSI
J1	62	SPI_B_SCLK	CSI_DATA04	I	O	3.3V	ECSPI1_SCLK
SPI_C							
J2	83	SPI_C_SS0	ENET2_RX_ER	I	O	3.3V	ECSPI4_SS0
J2	85	SPI_C_MISO	ENET2_TX_CLK	O	I	3.3V	ECSPI4_MISO
J2	87	SPI_C_MOSI	ENET2_TX_EN	I	O	3.3V	ECSPI4_MOSI
J2	89	SPI_C_SCLK	ENET2_TX_DATA1	I	O	3.3V	ECSPI4_SCLK

Table 5: SPI Interface Signals

*1 SM: PicoCore is Slave; MM: PicoCore is Master

4.4 I2C Interface

The module supports up to four I2C interfaces. Devices on baseboard with other voltage levels need a level shifter.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

Note:
I2C_D is used to control several peripherals on module (i.e. RTC, Audio Codec, Security Chip…).
Therefore it's not possible to use this contacts as GPIO or any other function.
For I2C_D, PicoCore™ is always the bus master.
Please use I2C_A/B/C before using I2C_D.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
I2C_A (I2C1)						
J1	4	I2C_A_SCL	UART4_TX_DATA	O	3.3V	onboard pull-up 2.49k
J1	6	I2C_A_SDA	UART4_RX_DATA	I/O	3.3V	onboard pull-up 2.49k
I2C_B (I2C3)						
J1	3	I2C_B_SCL	UART1_TX_DATA	O	3.3V	onboard pull-up 2.49k
J1	5	I2C_B_SDA	UART1_RX_DATA	I/O	3.3V	onboard pull-up 2.49k
J1	1	I2C_B_IRQ	GPIO1_IO01	I	3.3V	
I2C_C (I2C4)						
J1	40	I2C_C_SCL	UART2_TX_DATA	O	3.3V	onboard pull-up 2.49k
J1	42	I2C_C_SDA	UART2_RX_DATA	I/O	3.3V	onboard pull-up 2.49k
I2C_D (I2C2)						
J1	48	I2C_D_SCL	UART5_TX_DATA	O	3.3V	onboard pull-up 2.49k
J1	50	I2C_D_SDA	UART5_RX_DATA	I/O	3.3V	onboard pull-up 2.49k

Table 6: I2C Interface Signals

4.5 Serial Interface (UART)

PicoCoreMX6UL100 module provides 4 UART channels (2x UART with flow control signals RTS and CTS, 2x standard RX and TX).

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
UART_A (UART1) – Debug Port						
J1	14	UART_A_RTS	UART1_CTS	O	3.3V	
J1	16	UART_A_CTS	UART1_RTS	I	3.3V	
J1	18	UART_A_RXD	GPIO1_IO03	I	3.3V	onboard pull-up 100k
J1	20	UART_A_TXD	GPIO1_IO02	O	3.3V	
UART_B (UART5)						
J1	22	UART_B_RTS	GPIO1_IO09	O	3.3V	
J1	24	UART_B_CTS	GPIO1_IO08	I	3.3V	
J1	26	UART_B_RXD	GPIO1_IO05	I	3.3V	onboard pull-up 100k
J1	28	UART_B_TXD	GPIO1_IO04	O	3.3V	
UART_C (UART3)						
J1	30	UART_C_RXD	UART3_RX_DATA	I	3.3V	onboard pull-up 100k
J1	32	UART_C_TXD	UART3_TX_DATA	O	3.3V	
UART_D (UART6)						
J1	34	UART_D_RXD	CSI_PIXCLK	I	3.3V	onboard pull-up 100k
J1	36	UART_D_TXD	CSI_MCLK	O	3.3V	

Table 7: UART A/B/C/D Interface Signals

4.6 Ethernet

On the PicoCoreMX6UL100 module there are three options for the Ethernet interface. There is an assembly option to select between RMII Interface or up to 2x 10/100Mbit LAN.

4.6.1 Ethernet RMII Interface

Without Ethernet PHYs: The module supports two RMII interfaces. The RMII signals can be reached from the B2B Connector. In this case an external PHY or a switch is necessary on the carrier board. RMII pins can also be used as GPIOs.

ENET_MDIO and ENET_MDC can be used for both RMII interfaces.

ETH_A_LED Pin is used for the Bluetooth Activity LED and ETH_B_LED is used for WLAN Activity LED (In case of WLAN module is mounted and the PHYs are not).

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
RMII1						
J2	1	ETH_A_D1_P	GPIO1_IO07	O	3.3V	ENET_MDC
J2	3	ETH_A_D1_N	GPIO1_IO06	I/O	3.3V	ENET_MDIO onboard pull-up 1.5k
J2	5	ETH_A_D2_P	ENET1_TX_EN	O	3.3V	RMII1_TXEN
J2	7	ETH_A_D2_N	N.C.	X	X	Not Connected
J2	9	ETH_A_D3_P	ENET1_TX_DATA0	O	3.3V	RMII1_TXD0
J2	11	ETH_A_D3_N	ENET1_TX_DATA1	O	3.3V	RMII1_TXD1
J2	13	ETH_A_D4_P	ENET1_TX_CLK	O	3.3V	RMII1_TXCLK
J2	15	ETH_A_D4_N	N.C.	X	X	Not Connected
J2	17	ETH_A_LED	BT_LED (WLAN Module)	O	3.3V	BT_LED
J2	21	ETH_B_LED	WLAN_LED (WLAN Module)	O	3.3V	WLAN_LED
J2	23	ETH_B_D1_P	ENET1_RX_EN	I	3.3V	RMII1_CRS_DV
J2	25	ETH_B_D1_N	ENET1_RX_ER	I	3.3V	RMII1_RXER
J2	27	ETH_B_D2_P	ENET1_RX_DATA0	I	3.3V	RMII1_RXD0
J2	29	ETH_B_D2_N	ENET1_RX_DATA1	I	3.3V	RMII1_RXD1
J2	31	ETH_B_D3_P	N.C.	X	X	Not Connected
J2	33	ETH_B_D3_N	N.C.	X	X	Not Connected
J2	35	ETH_B_D4_P	SNVS_TAMPER2	I	3.3V	ETH_PHY_IRQ
J2	37	ETH_B_D4_N	SNVS_TAMPER0	O	3.3V	ETH1_PHY_RESET
RMII2						
J2	69	GPIO_J2_69	SNVS_TAMPER1	O	3.3V	ETH2_PHY_RESET
J2	73	GPIO_J2_73	ENET2_RX_DATA1	I	3.3V	RMII2_RXD1
J2	75	GPIO_J2_75	ENET2_RX_DATA0	I	3.3V	RMII2_RXD0
J2	77	GPIO_J2_77	ENET2_RX_EN	I	3.3V	RMII2_CRS_DV
J2	79	GPIO_J2_79	ENET2_TX_DATA0	O	3.3V	RMII2_TXD0
J2	83	SPI_C_SS0	ENET2_RX_ER	I	3.3V	RMII2_RXER
J2	85	SPI_C_MISO	ENET2_TX_CLK	O	3.3V	RMII2_TXCLK
J2	87	SPI_C_MOSI	ENET2_TX_EN	O	3.3V	RMII2_TXEN
J2	89	SPI_C_SCLK	ENET2_TX_DATA1	O	3.3V	RMII2_TXD1

Table 8: Ethernet Interface RMII Signals

4.6.2 Ethernet Interface with 1x PHY

The PicoCoreMX6UL100 can support up to two 10/100Mbit LAN Interfaces via Ethernet PHYs (KSZ8081) on module.

Ethernet data signals are connected as 100-Ohm differential pairs.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
Option1: 1x 10/100Mbit Ethernet						
J2	1	ETH_A_D1_P	TXP (PHY_1)	I/O	1.2V	Ethernet A Data 1+
J2	3	ETH_A_D1_N	TXM (PHY_1)	I/O	1.2V	Ethernet A Data 1-
J2	5	ETH_A_D2_P	RXP (PHY_1)	I/O	1.2V	Ethernet A Data 2+
J2	7	ETH_A_D2_N	RXM (PHY_1)	I/O	1.2V	Ethernet A Data 2-
J2	9	ETH_A_D3_P	N.C.	X	X	Not Connected
J2	11	ETH_A_D3_N	N.C.	X	X	Not Connected
J2	13	ETH_A_D4_P	N.C.	X	X	Not Connected
J2	15	ETH_A_D4_N	N.C.	X	X	Not Connected
J2	17	ETH_A_LED	LED0 (PHY_1)	O	3.3V	Activity LED
J2	21	ETH_B_LED	N.C.	X	X	Not Connected
J2	23	ETH_B_D1_P	N.C.	X	X	Not Connected
J2	25	ETH_B_D1_N	N.C.	X	X	Not Connected
J2	27	ETH_B_D2_P	N.C.	X	X	Not Connected
J2	29	ETH_B_D2_N	N.C.	X	X	Not Connected
J2	31	ETH_B_D3_P	N.C.	X	X	Not Connected
J2	33	ETH_B_D3_N	N.C.	X	X	Not Connected
J2	35	ETH_B_D4_P	N.C.	X	X	Not Connected
J2	37	ETH_B_D4_N	N.C.	X	X	Not Connected
J2	69	GPIO_J2_69	SNVS_TAMPER1	I/O	3.3V	Can be used as GPIO
J2	73	GPIO_J2_73	ENET2_RX_DATA1	I/O	3.3V	Can be used as GPIO
J2	75	GPIO_J2_75	ENET2_RX_DATA0	I/O	3.3V	Can be used as GPIO
J2	77	GPIO_J2_77	ENET2_RX_EN	I/O	3.3V	Can be used as GPIO
J2	79	GPIO_J2_79	ENET2_TX_DATA0	I/O	3.3V	Can be used as GPIO
J2	83	SPI_C_SS0	ENET2_RX_ER	I/O	3.3V	SPI Interface or GPIO
J2	85	SPI_C_MISO	ENET2_TX_CLK	I/O	3.3V	SPI Interface or GPIO
J2	87	SPI_C_MOSI	ENET2_TX_EN	I/O	3.3V	SPI Interface or GPIO
J2	89	SPI_C_SCLK	ENET2_TX_DATA1	I/O	3.3V	SPI Interface or GPIO

Table 9: Ethernet Interface Signals (1x PHY)

4.6.3 Ethernet Interface with 2x PHY

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
Option2: 2x 10/100Mbit Ethernet						
J2	1	ETH_A_D1_P	TXP (PHY_1)	I/O	1.2V	Ethernet A Data 1+
J2	3	ETH_A_D1_N	TXM (PHY_1)	I/O	1.2V	Ethernet A Data 1-
J2	5	ETH_A_D2_P	RXP (PHY_1)	I/O	1.2V	Ethernet A Data 2+
J2	7	ETH_A_D2_N	RXM (PHY_1)	I/O	1.2V	Ethernet A Data 2-
J2	9	ETH_A_D3_P	N.C.	X	X	Not Connected
J2	11	ETH_A_D3_N	N.C.	X	X	Not Connected
J2	13	ETH_A_D4_P	N.C.	X	X	Not Connected
J2	15	ETH_A_D4_N	N.C.	X	X	Not Connected
J2	17	ETH_A_LED	LED0 (PHY_1)	O	3.3V	Activity LED
J2	21	ETH_B_LED	LED0 (PHY_2)	O	3.3V	Activity LED
J2	23	ETH_B_D1_P	TXP (PHY_2)	I/O	1.2V	Ethernet A Data 1+
J2	25	ETH_B_D1_N	TXM (PHY_2)	I/O	1.2V	Ethernet A Data 1-
J2	27	ETH_B_D2_P	RXP (PHY_2)	I/O	1.2V	Ethernet A Data 2+
J2	29	ETH_B_D2_N	RXM (PHY_2)	I/O	1.2V	Ethernet A Data 2-
J2	31	ETH_B_D3_P	N.C.	X	X	Not Connected
J2	33	ETH_B_D3_N	N.C.	X	X	Not Connected
J2	35	ETH_B_D4_P	N.C.	X	X	Not Connected
J2	37	ETH_B_D4_N	N.C.	X	X	Not Connected
J2	69	GPIO_J2_69	N.C.	X	X	Not Connected
J2	73	GPIO_J2_73	N.C.	X	X	Not Connected
J2	75	GPIO_J2_75	N.C.	X	X	Not Connected
J2	77	GPIO_J2_77	N.C.	X	X	Not Connected
J2	79	GPIO_J2_79	N.C.	X	X	Not Connected
J2	83	SPI_C_SS0	N.C.	X	X	Not Connected
J2	85	SPI_C_MISO	N.C.	X	X	Not Connected
J2	87	SPI_C_MOSI	N.C.	X	X	Not Connected
J2	89	SPI_C_SCLK	N.C.	X	X	Not Connected

Table 10: Ethernet Interface Signals (2x PHY)

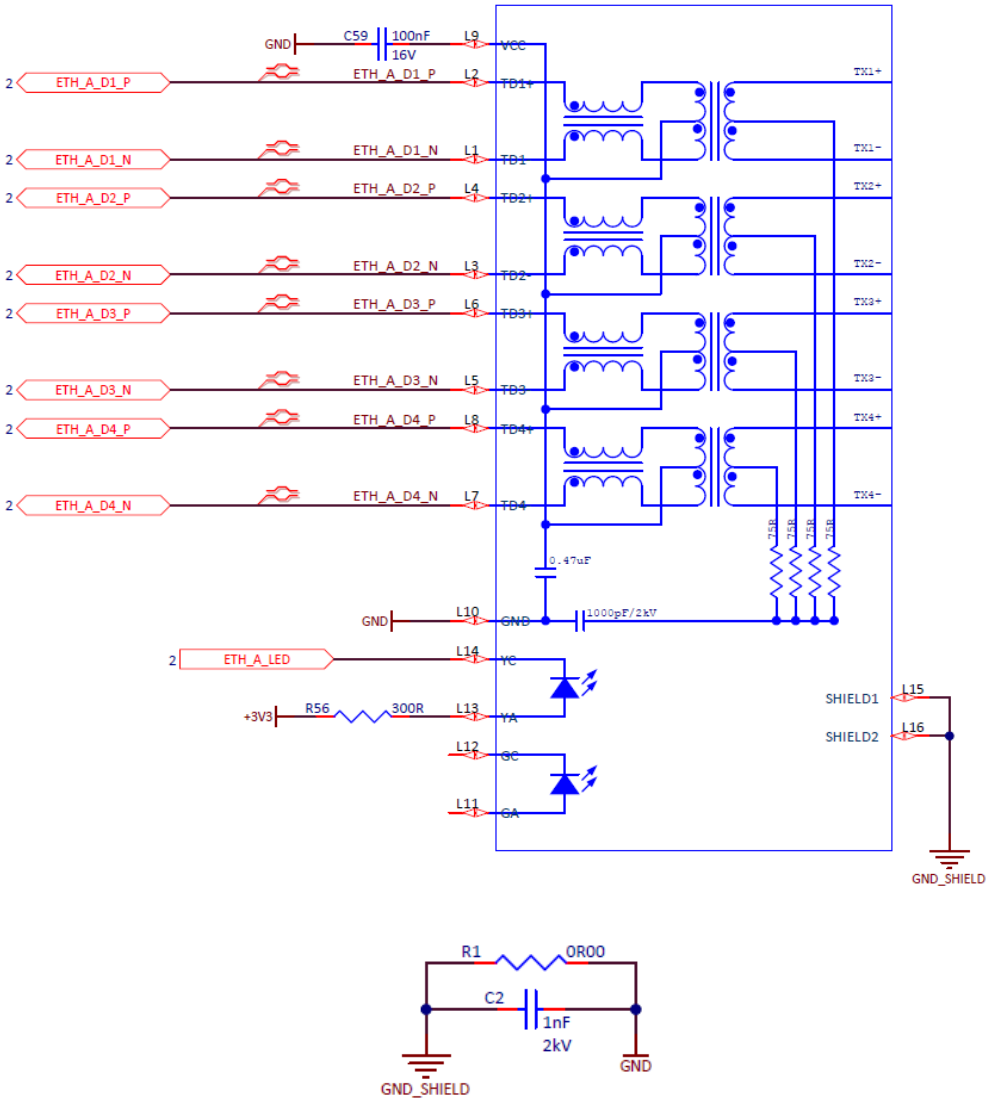


Figure 9: LAN output example

4.7 Audio

The PicoCoreMX6UL100 module can support audio interface either directly via I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied internally on PicoCore module as default. For a better and smoother audio quality, an external low-noise power supply (e.g. LDO) can be used.

AUDIO_A_GND is connected to GND on PicoCore module as default. There is a mounting option to use external GND for the analogue part of the audio codec.

Please contact us to have the right assembly option for the external-supplied AUDIO_A_VCC and/or AUDIO_A_GND.

	Pin	Signal	Function	I/O	Voltage	Remarks
Analog Line In/Out – With Audio Codec						
J2	2	AUDIO_A_VCC	VDDA	PWR	3.3V / 3V	Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to 3.3V
J2	4	AUDIO_A_GND	AGND	PWR		Optional: Noise reduced external power supply for audio codec. Default: Onboard connection to GND
J2	6	AUDIO_A_LOUT_L	LOUT	O	AUDIO_A_VCC	
J2	8	AUDIO_A_LOUT_R	ROUT	O	AUDIO_A_VCC	
J2	10	AUDIO_A_MIC	MICIN	I	AUDIO_A_VCC	
J2	12	AUDIO_A_LIN_L	LLINEIN	I	AUDIO_A_VCC	
J2	14	AUDIO_A_LIN_R	RLINEIN	I	AUDIO_A_VCC	
J2	18	AUDIO_A_HP_L	LHPOUT	O	AUDIO_A_VCC	
J2	20	AUDIO_A_HP_R	RHPOUT	O	AUDIO_A_VCC	
J2	22	AUDIO_A_HP_GND	HP_VGND	O		Do not connect to common GND directly!

Table 11: Audio Interface (with Audio Codec)

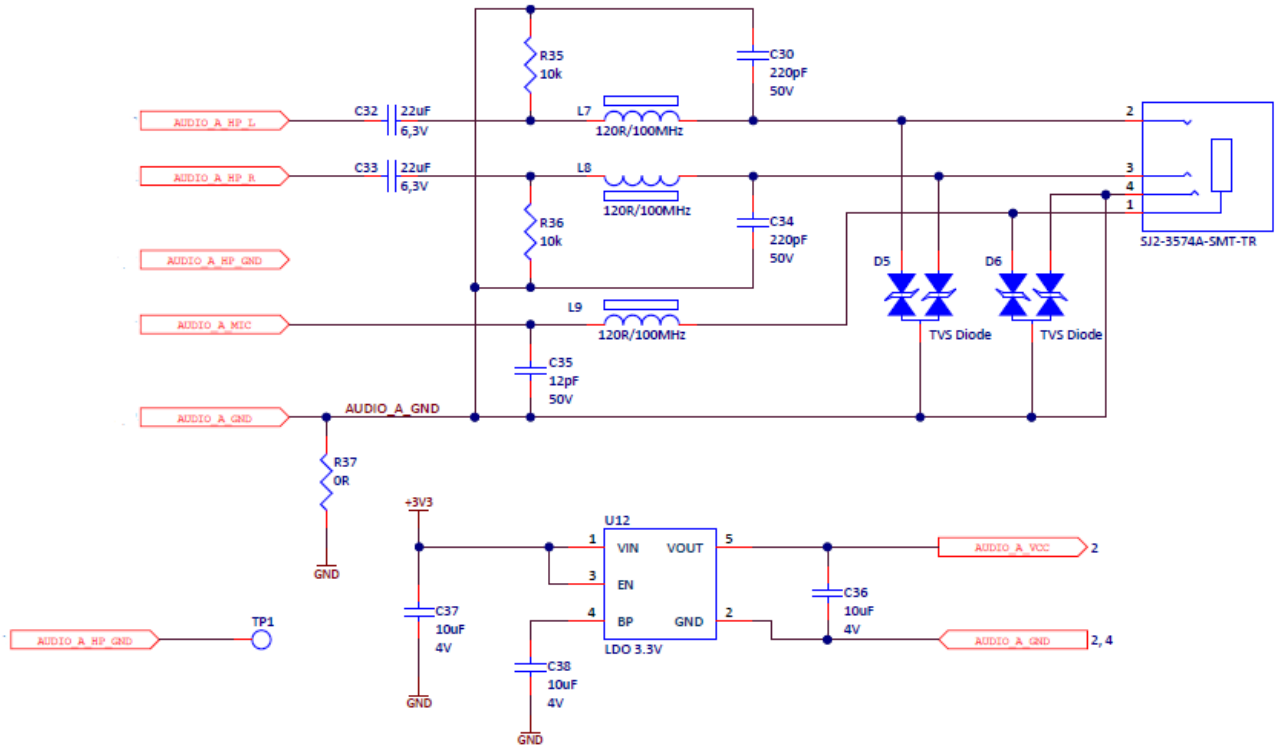


Figure 10: Headphone-Out Mic-In Example Circuit

Pin		Signal	CPU Pad	I/O	Voltage	Remarks
I2S Option – Without Audio Codec						
J2	2	AUDIO_A_VCC	N.C.	X	X	Do not connect
J2	4	AUDIO_A_GND	N.C.	X	X	Do not connect
J2	6	AUDIO_A_LOUT_L	JTAG_TDI	O	3.3V	I2S_SCLK
J2	8	AUDIO_A_LOUT_R	JTAG_TDO	O	3.3V	I2S_LRCLK
J2	10	AUDIO_A_MIC	N.C.	X	X	Do not connect
J2	12	AUDIO_A_LIN_L	JTAG_TMS	O	3.3V	I2S_MCLK
J2	14	AUDIO_A_LIN_R	N.C.	X	X	Do not connect
J2	18	AUDIO_A_HP_L	JTAG_nTRST	O	3.3V	I2S_DOUT
J2	20	AUDIO_A_HP_R	JTAG_TCK	I	3.3V	I2S_DIN
J2	22	AUDIO_A_HP_GND	N.C	X	X	Do not connect

Table 12: Audio Interface (without Audio Codec)

Note:
I2S signals are shared with JTAG pins. If JTAG Pins are in use, the I2S pins are not available (or vice versa).

4.8 Display

PicoCoreMX6UL100 module offers two options for the display interface. The module can support either 18-bit RGB or 4-lane LVDS. Both of the interfaces uses the DSI_A and DSI_B pins, which means they are not available at the same time.

4.8.1 18-bit RGB

	Pin	Signal	CPU Pad	I/O	Voltage	18-bit RGB
J1	17	DSI_A_CLK_P	LCD_DATA5	O	3.3V	RGB – R5 (MSB)
J1	19	DSI_A_CLK_N	LCD_DATA4	O	3.3V	RGB – R4
J1	23	DSI_A_DATA0_P	LCD_ENABLE	O	3.3V	RGB – EN
J1	25	DSI_A_DATA0_N	LCD_CLK	O	3.3V	RGB – CLK
J1	29	DSI_A_DATA1_P	LCD_DATA1	O	3.3V	RGB – R1
J1	31	DSI_A_DATA1_N	LCD_DATA0	O	3.3V	RGB – R0 (LSB)
J1	35	DSI_A_DATA2_P	LCD_DATA3	O	3.3V	RGB – R3
J1	37	DSI_A_DATA2_N	LCD_DATA2	O	3.3V	RGB – R2
J1	41	DSI_A_DATA3_P	LCD_DATA7	O	3.3V	RGB – G1
J1	43	DSI_A_DATA3_N	LCD_DATA6	O	3.3V	RGB – G0 (LSB)
J1	47	DSI_B_CLK_P	LCD_DATA15	O	3.3V	RGB – B3
J1	49	DSI_B_CLK_N	LCD_DATA14	O	3.3V	RGB – B2
J1	53	DSI_B_DATA0_P	LCD_DATA9	O	3.3V	RGB – G3
J1	55	DSI_B_DATA0_N	LCD_DATA8	O	3.3V	RGB – G2
J1	59	DSI_B_DATA1_P	LCD_DATA11	O	3.3V	RGB – G5 (MSB)
J1	61	DSI_B_DATA1_N	LCD_DATA10	O	3.3V	RGB – G4
J1	65	DSI_B_DATA2_P	LCD_DATA13	O	3.3V	RGB – B1
J1	67	DSI_B_DATA2_N	LCD_DATA12	O	3.3V	RGB – B0 (LSB)
J1	71	DSI_B_DATA3_P	LCD_DATA17	O	3.3V	RGB – B5
J1	73	DSI_B_DATA3_N	LCD_DATA16	O	3.3V	RGB – B4
J1	52	GPIO_J1_52*	LCD_HSYNC	O	3.3V	RGB – HSYNC
J1	54	GPIO_J1_54*	LCD_VSYNC	O	3.3V	RGB – VSYNC

Table 13: RGB Interface

4.8.2 LVDS

Also there is a mounting option on the module to get single channel LVDS instead of RGB. In this case the module comes with Lontium LT9211 RGB to LVDS converter chip.

	Pin	Signal	LT9211 Pad	I/O	Voltage	Remarks
J1	17	DSI_A_CLK_P	MLTXA_M1LCP	O	1.8V	LVDS Clock+
J1	19	DSI_A_CLK_N	MLTXA_M1LCN	O	1.8V	LVDS Clock-
J1	23	DSI_A_DATA0_P	MLTXA_M3L0P	O	1.8V	LVDS Data0+
J1	25	DSI_A_DATA0_N	MLTXA_ M3L0N	O	1.8V	LVDS Data0-
J1	29	DSI_A_DATA1_P	MLTXA_M2L1P	O	1.8V	LVDS Data1+
J1	31	DSI_A_DATA1_N	MLTXA_ M2L1N	O	1.8V	LVDS Data1-
J1	35	DSI_A_DATA2_P	MLTXA_MCL2P	O	1.8V	LVDS Data2+
J1	37	DSI_A_DATA2_N	MLTXA_ MCL2N	O	1.8V	LVDS Data2-
J1	41	DSI_A_DATA3_P	MLTXA_M0L3P	O	1.8V	LVDS Data3+
J1	43	DSI_A_DATA3_N	MLTXA_M0L3N	O	1.8V	LVDS Data3-
J1	47	DSI_B_CLK_P	N.C.	X	X	Not connected
J1	49	DSI_B_CLK_N	N.C.	X	X	Not connected
J1	53	DSI_B_DATA0_P	N.C.	X	X	Not connected
J1	55	DSI_B_DATA0_N	N.C.	X	X	Not connected
J1	59	DSI_B_DATA1_P	N.C.	X	X	Not connected
J1	61	DSI_B_DATA1_N	N.C.	X	X	Not connected
J1	65	DSI_B_DATA2_P	N.C.	X	X	Not connected
J1	67	DSI_B_DATA2_N	N.C.	X	X	Not connected
J1	71	DSI_B_DATA3_P	N.C.	X	X	Not connected
J1	73	DSI_B_DATA3_N	N.C.	X	X	Not connected

Table 14: Single Channel LVDS Interface

4.9 CAN Interface

The module can also support up to 2x CAN Interfaces.

The second CAN channel can be reached via GPIO_J1_44 and GPIO_J1_46 Pins. Please refer to the GPIO reference card. These pins can also be used as standard GPIOs.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	10	CAN_RX	UART3_RTS	I	3.3V	CAN_A_RX
J1	12	CAN_TX	UART3_CTS	O	3.3V	CAN_A_TX
J1	44	GPIO_J1_44	UART2_CTS	O	3.3V	CAN_B_TX
J1	46	GPIO_J1_46	UART2_RTS	I	3.3V	CAN_B_RX

Table 15: CAN FD Pin Layout

4.10 WLAN/BT Interface

The PicoCoreMX6UL100 contains a certified high performance WLAN and Bluetooth module.

The module is based on NXP 88W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan (pre) certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: In case WLAN/BT module is mounted, there are no SD card interfaces available.

4.11 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO contacts. Also a higher voltage as the announced IO power is not allowed.

For more information about the alternative usages of the GPIOs please refer to the GPIO Reference Card.

4.12 JTAG

JTAG pins are shared with I2S interface. There is a mounting option to disconnect I2S/Audio Codec from JTAG interface. Ask support for more information

	Pin	Signal	Function	I/O	Voltage	Remarks
J2	93	JTAG_TCK	JTAG_TCK	I	3.3V	
J2	95	JTAG_TMS	JTAG_TMS	I	3.3V	
J2	97	JTAG_TDI	JTAG_TDI	I	3.3V	
J2	99	JTAG_TDO	JTAG_TDO	O	3.3V	

Table 16: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

5 Flash

PicoCoreMX6UL100 can be shipped with SLC NAND Flash or MLC eMMC. By default fuses of i.MX6 processors are configured so that PicoCore boots from the assembled flash memory.

Please contact support for other boot options.

5.1 NAND Flash

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system

5.2 eMMC

If mounted instead NAND an eMMC v4.41 or higher with 4GB or more is mounted from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

5.3 EEPROM

There is also an extra 2kbit 2-wire EEPROM option on the module which is controlled via I2C signals. Standard modules do not come with an EEPROM. Please contact with our engineers for further informations.

Note:
This component is optional and not mounted in all configurations. Please contact sales to get more information.

6 RTC

There is an external RTC (NXP PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

Note:

This component is optional and not mounted in all configurations. Please contact sales to get more information.

8 Power and Power Control Contacts

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main power supply input
J2	30 32 34	GND[*5]	I	Main power supply ground input
J2	36	VDD_VBAT[*1]	I	RTC battery input; tie to 3.0V Please refer chapter 9
J2	40	VDD_3V3[*2]	O	20mA output from on module DCDC powered from VDD_VIN
J2	52	SD_A_VCC	I	SDHC power output; 3.3V or 1.8V
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_H_VBUS	I	USB Phy voltage input; 5V
J2	42	RESETINN[*3]	I	Power on reset input; 10k Pull-Up to 3.3V
J2	44	PMIC_STBY[*4]	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button Active high – 10k pull-down

Table 17: Power and Power Control

[*1] By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

[*2] VDD_3V3 is a 3.3V @20mA output. It's generated from the internal PMIC and powered from VIN. Can be used as "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 as power supply for carrier board.

[*3] RESETIN is the reset input for the module. RESETIN only resets the CPU. In the event of a power failure, VDD_VIN must be switched off and on to avoid latch-up effects.

[*4] PMIC_STBY_REQ is set HIGH when the CPU is in standby mode. This allows to switch off peripheral functions and save more power. Wakeup from standby mode needs support by the driver, you have to check.

[*5] The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts)

9 Electrical characteristic

9.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 18: Absolute Maximum Ratings

9.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VDD_VIN	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_OTG_VBUS	USB supply voltage		4.5	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_SNVS		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

Table 19: DC Electrical Characteristics

10 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top (Ψ_{JT}) – **i.MX6ULL**		0.2		°C /W

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. In this case cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 2: WLAN/BT is -30°C to +85°C only. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN5337 (https://www.nxp.com/docs/en/application-note/AN5337.pdf)

11 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

12 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

13 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

14 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (70°C/85°C).

The maximum power consumption of the board could be **t.b.d**. This values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d to t.b.d** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

15 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

16 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

17 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.

The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

18 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 11: Matrix Code Sticker

19 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

F&S reserves the right to make changes in its products or product specifications or product documentation with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

F&S makes no warranty or guarantee regarding the suitability of its products for any particular purpose, nor does F&S assume any liability arising out of the documentation or use of any product and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

Products are not designed, intended, or authorized for use as components in systems intended for applications intended to support or sustain life, or for any other application in which the failure of the product from F&S could create a situation where personal injury or death may occur. Should the Buyer purchase or use a F&S product for any such unintended or unauthorized application, the Buyer shall indemnify and hold F&S and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that F&S was negligent regarding the design or manufacture of said product.

Specifications are subject to change without notice.

Warranty Terms

Hardware Warranties

F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S's sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Software Warranties

Software is provided "AS IS". F&S makes no warranties, either express or implied, with regard to the software object code or software source code either or with respect to any third party materials or intellectual property obtained from third parties. F&S makes no warranty that the software is useable or fit for any particular purpose. This warranty replaces all other warranties written or unwritten. F&S expressly disclaims any such warranties. In no case shall F&S be liable for any consequential damages.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN PLACE OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL F&S BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL F&S BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE PRODUCT, THE CUSTOMER APPROVES THAT THE F&S PRODUCT, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS

20 Content

Table 1: Mechanical Dimensions 7
Table 2: B2B connector 16
Table 3: USB OTG & Host Interface Connections 17
Table 4: SD Card Interface A 19
Table 5: SPI Interface Signals 21
Table 6: I2C Interface Signals 22
Table 7: UART A/B/C/D Interface Signals 23
Table 8: Ethernet Interface RMII Signals 25
Table 9: Ethernet Interface Signals (1x PHY) 26
Table 10: Ethernet Interface Signals (2x PHY) 27
Table 11: Audio Interface (with Audio Codec) 29
Table 12: Audio Interface (without Audio Codec) 30
Table 13: RGB Interface 31
Table 14: Single Channel LVDS Interface 32
Table 15: CAN FD Pin Layout 33
Table 16: JTAG Interface 34
Table 17: Power and Power Control 37
Table 18: Absolute Maximum Ratings 38
Table 19: DC Electrical Characteristics 38

Figure 1: Block Diagram 5
Figure 2: Mechanical Dimension Top 6
Figure 3: Mechanical Dimension Bottom 7
Figure 4: SMT Steel Spacer 8
Figure 5: USB OTG example connection 18
Figure 6: Recommended Solution for swapped USB Data Signals 18
Figure 7: SD Card Connector example connection 20
Figure 8: SD_A supply voltage switching circuit 20
Figure 9: LAN output example 28
Figure 10: Headphone-Out Mic-In Example Circuit 30
Figure 11: Matrix Code Sticker 42