Hardware Documentation

armStone™MX8MP

Preliminary

Version 004
(2024-03-28)

© F&S Elektronik Systeme GmbH
Untere Waldplätze 23
D-70569 Stuttgart
Phone: +49(0)711-123722-0

About This Document

This document describes how to use the armStone™MX8MP board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
30.05.2022	001	All			Initial release	MD, UK
19.08.2022	002	All	A	5.4	Add Info for UART_B	MW
30.11.2023	003	All	A	5.10	Add Info for VLCD	MW
04.03.2024	004	All	M	2.1	Update mechanical drawing Top	MW

V	Document Version
A, M, R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block Diagram

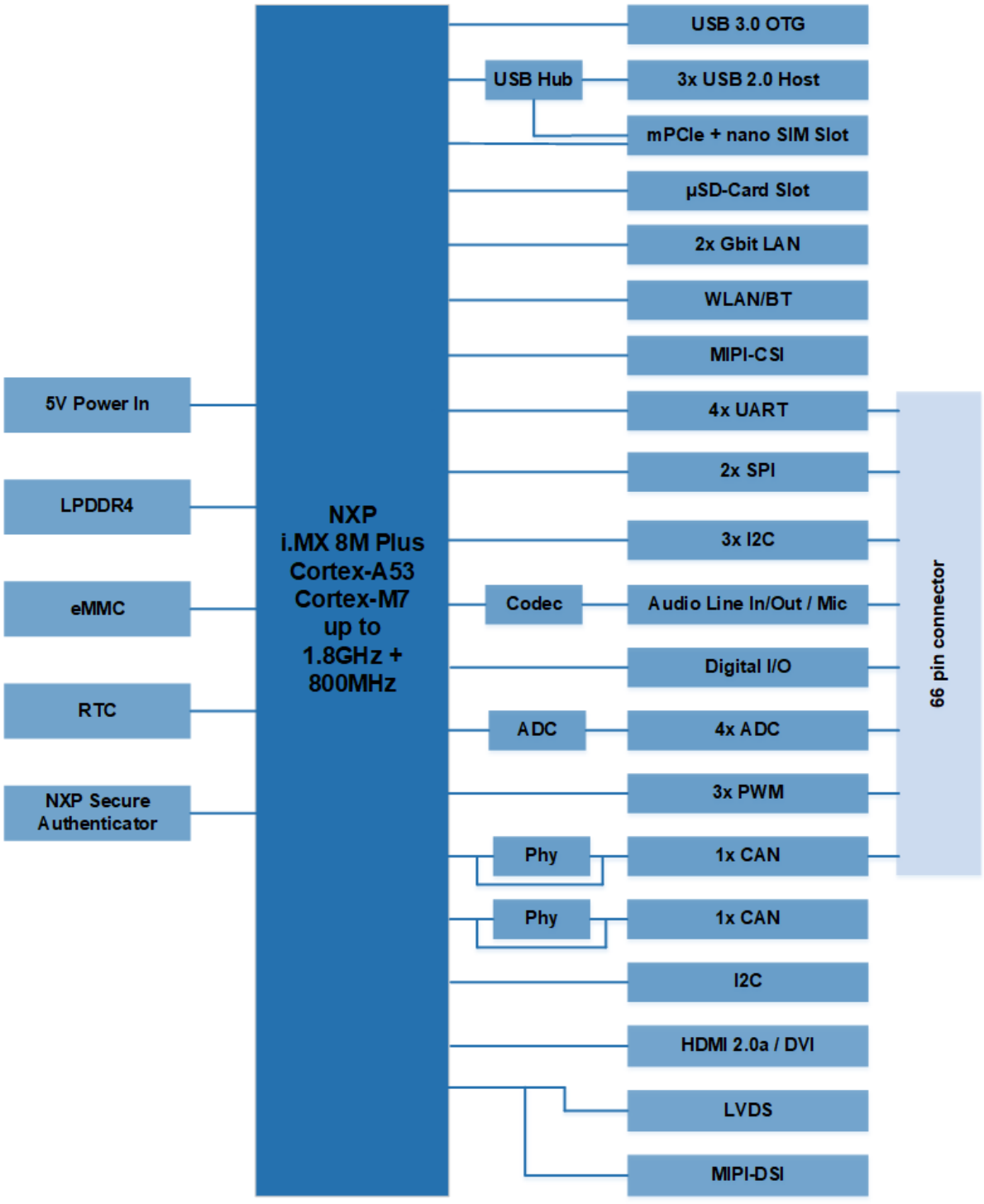


Figure 1: Block Diagram

2 Mechanical Characteristics

2.1 Board

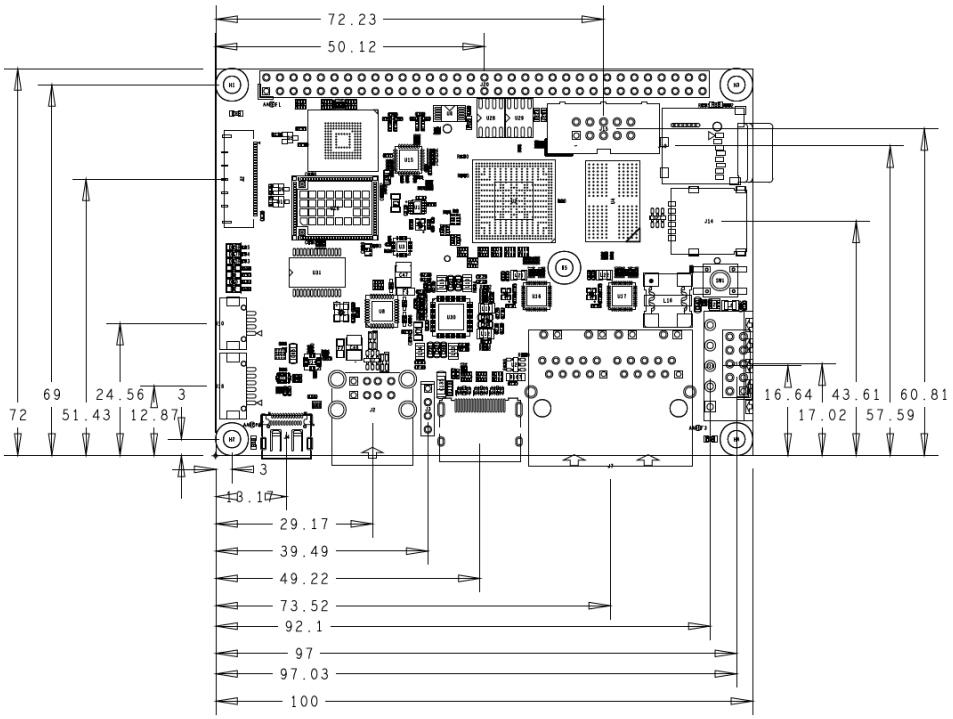


Figure 2: Top View

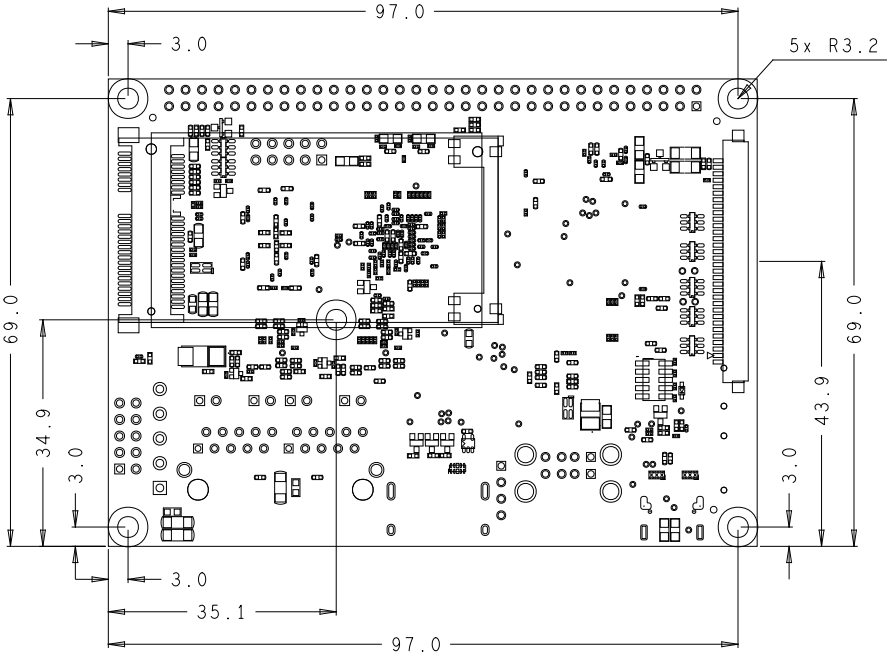


Figure 3: Bottom View

Note: *All Dimensions are in mm.*

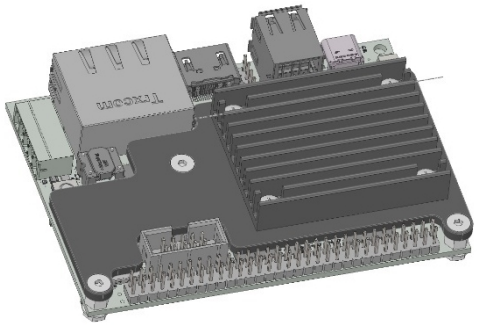
Dimension	Value
Size	100 mm x 72 mm
PCB Thickness	1.6 mm ± 0.16 mm
Height of the parts on the top side (max.)	15.5 mm
Height of the parts on the bottom side (max.)	5.9 mm
Weight	63 g

Table 1: Mechanical Specifications

3D Step model available, please contact support@fs-net.de.

2.2 Heat Spreader

For heat dissipation, F&S offers a heat spreader, which can be ordered at the F&S web shop (p.n.: **MHS.AS8MP.1**). It can be used as a connection point for cooling elements.



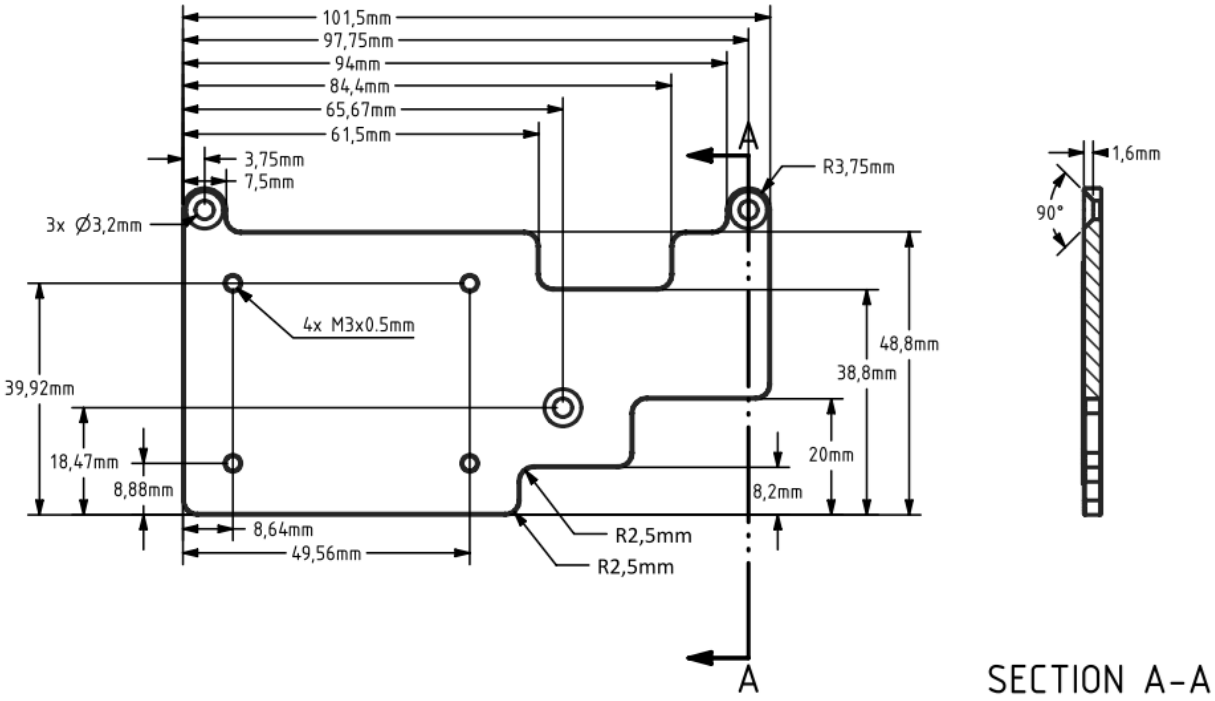


Figure 4: armStone™MX8MP Heat Spreader

3 Connectors

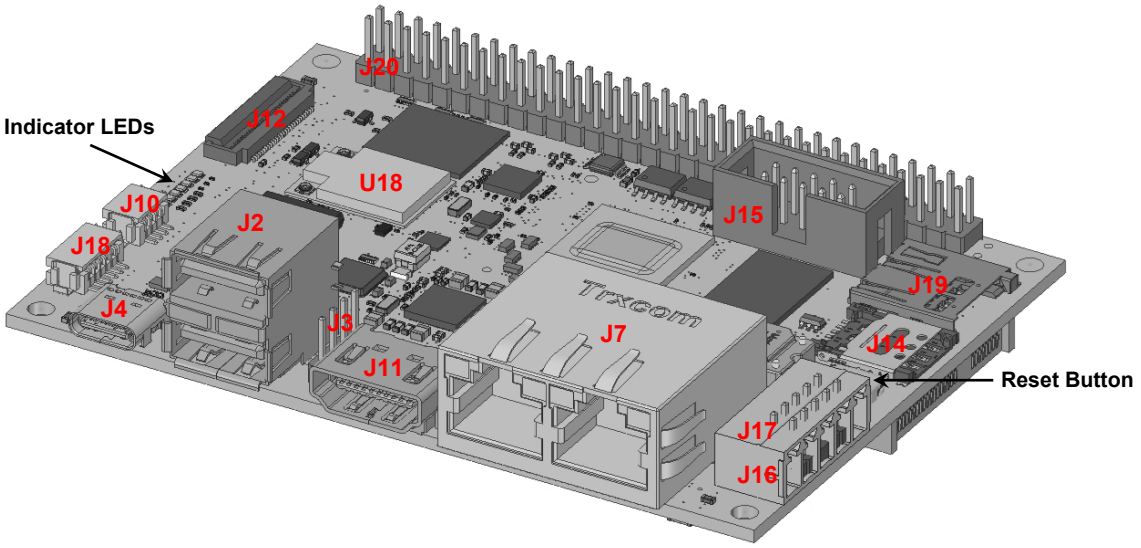


Figure 5: armStone™MX8MP Top View

Ref.	Description	No. of Pins	Connector Type
J2	USB Host (Stacked Type A, USB 2.0)	-	US-2005-3GNB-TR
J3	USB Host (Pin Header, 2.54 mm)	4	-
J4	USB OTG (Type C, USB 3.1)	-	UC-3019-2GNB-RR
J7	ETH (2xRJ45 with integrated magnetics)	-	TRJG27440ADNL
J10	Display (Backlight Supply)	4	DF13-4P-1.25H
J11	HDMI	-	WR-COM HDMI 685119134923
J12	Camera (FFC, Basler)	28	FH41-28S-0.5SH(05)
J14	Nano SIM Slot	-	SM-3003-1XNB-RR
J15	CAN (Pin Header shrouded, 2.54 mm)	10	WR-BHD 61201021621
J16	Power (Header, 3.81 mm)	5	WR-TBL 691322310005
J17	Power (Pin Header, 2.54 mm) [1]	10	-
J18	Display (Touch)	6	DF13-6P-1.25H
J19	µSD Card Slot	-	WR-CRD 693071010811
J20	Feature Connector (Pin Header, 2.54 mm)	66	-
U18	WLAN/BT-module (CM276NF)	-	MHF-4

Table 2: Connector Types Top Side

Note 1: *Optional (instead of J16), please contact support@fs-net.de for further information.*

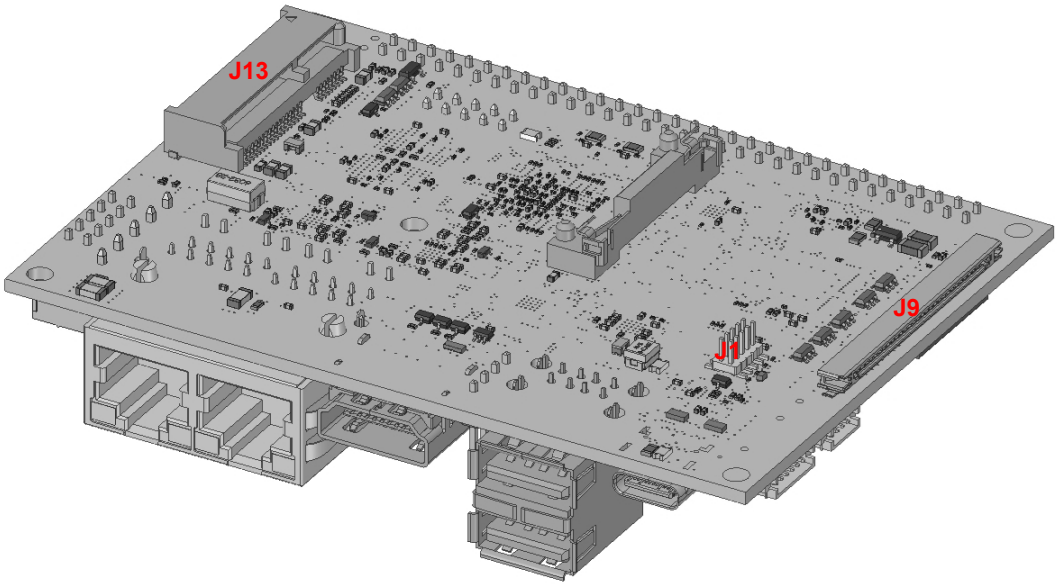


Figure 6: armStone™MX8MP Bottom View

Ref.	Description	No. of Pins	Connector Type
J1	JTAG (Pin Header, 1.27 mm)	10	-
J9	MIPI-DSI and/or LVDS (FPC)	30	Hirose, MDF76GW-30S-1H(55)
J13	Mini PCIe Slot	52	-

Table 3: Connector Types Bottom Side

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Description	Symbol	Condition	Min	Max	Unit
Input Voltage	VCC_IN		2.7	6.0	V
USB Voltage			-0.3	5.6	V
Voltage on 3.3V IO pins		board powered up	-0.3	3.6	V
Voltage on any IO pin		board powered down	-0.3	0.3	V

Table 4: Absolute Maximum Ratings

4.2 Recommended Operating Conditions

Description	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	VCC_IN		4.5	5.0	5.5	V
RTC Battery Voltage	VDD_VBAT		0.9	3.0	5.5	V
RTC Battery Current		T_{AMB} =25°C	0.3	-	10	µA
		T_{AMB} =85°C	0.6	-	10	µA
On Board 3.3 V DCDC	VDD_3V3		3.15	3.3	3.45	V
Output Current IOs		VDD_3V3	-	-	5	mA
High Level Input Voltage	V_{ih}		0.7 x VDD_3V3	-	VDD_3V3	V
Low Level Input Voltage	V_{il}		0	-	0.3 x VDD_3V3	V
High Level Output Voltage	V_{oh}	I_{oh}=0.1mA	VDD_3V3 – 0.15	-	VDD_3V3	V
Low Level Output Voltage	V_{ol}	I_{oh}=0.1mA	-	-	0.15	V

Table 5: Recommended Operating Conditions

5 Interfaces

5.1 Power Supply

5.1.1 Default

J16 [1] is the default connector for an external DC power supply.

Pin	Signal Name	I/O	Voltage	Description
1	N.C.	X		Not Connected
2	VDD_VBAT [2]	PWR	3.0 V	External RTC Supply Voltage (optional)
3	VCC_IN	PWR	5.0 V	Supply Voltage (board)
4	GND			
5	VDD_3V3	O	3.3 V	Feedback (if board is powered up)

Table 6: Power (J16)

Note 1: *The connector is compatible to F&S power supply ADP-NT24V2, please contact support@fs-net.de for further information.*

Note 2: *If using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.*

5.1.2 Optional

J17 is an optional connection for an external DC power supply.

Pin	Signal Name	I/O	Voltage	Description
1	VDD_VBAT	PWR	3.0 V	External RTC Supply Voltage (optional)
2	VDD_VBAT	PWR	3.0 V	External RTC Supply Voltage (optional)
3	VCC_IN	PWR	5.0 V	Supply Voltage (board)
4	VCC_IN	PWR	5.0 V	Supply Voltage (board)
5	VCC_IN	PWR	5.0 V	Supply Voltage (board)
6	VCC_IN	PWR	5.0 V	Supply Voltage (board)
7	GND			
8	GND			
9	GND			
10	GND			

Table 7: Power (J17)

5.2 USB

5.2.1 USB Host

The board provides 4 USB 2.0 Host Ports (Hub [1]: USB2514):

- USB Port1, 2: Stacked USB Connector (J2) [2]
- USB Port3: 2.54mm Pin Header (J3)
- USB Port4: Mini PCIe Slot (J13)

Pin	Signal Name	I/O	Voltage	Description
Port 1 (J2 bottom)				
A1	+5V_USB_Port1	PWR	5.0 V	V_{BUS} (fused: 1.1 A)
A2	USB_HUB_P1_N	I/O		Port 1 Data-
A3	USB_HUB_P1_P	I/O		Port 1 Data+
A4	GND			
Port 2 (J2 top)				
B1	+5V_USB_Port2	PWR	5.0 V	V_{BUS} (fused: 1.1 A)
B2	USB_HUB_P2_N	I/O		Port 2 Data-
B3	USB_HUB_P2_P	I/O		Port 2 Data+
B4	GND			
Port 3 (J3)				
1	+5V_USB_Port3	PWR	5.0 V	V_{BUS} (fused: 1.1 A)
2	USB_HUB_P3_N	I/O		Port 3 Data-
3	USB_HUB_P3_P	I/O		Port 3 Data+
4	GND			

Table 8: USB Host (J2, J3)

Note 1: *Default configuration. Optionally it's possible to get the board without hub. Only USB Port 1 is available and J3 is not mounted in this case. Please contact support@fs-net.de for further information.*

Note 2: *ESD protected*

5.2.2 USB OTG

The board provides an USB OTG Port [1] (J4, USB Type C).

Pin	Signal Name	I/O	Voltage	Description
A1 B1	GND			
A2 B2	SSTX1_P	O		SuperSpeed TX+
A3 B3	SSTX1_N	O		SuperSpeed TX-
A4 B4	USB_OTG_CN_VBUS	PWR [2]	5.0 V	V_{BUS} (fused: 1.1 A)
A5	CC1	I		Configuration Channel
B5	CC2	I		Configuration Channel
A6 B6	USB_OTG_CN_DP	I/O		USB 2.0 Data+
A7 B7	USB_OTG_CN_DN	I/O		USB 2.0 Data-
A8	N.C.	X		Not Connected
B8	N.C.	X		Not Connected
A9 B9	USB_OTG_CN_VBUS	PWR [2]	5.0 V	V_{BUS} (fused: 1.1 A)
A10 B10	SSRX1_P	I		SuperSpeed RX+
A11 B11	SSRX1_N	I		SuperSpeed RX-
A12 B12	GND			

Table 9: USB OTG (J4)

Note 1: *ESD protected*

Note 2: *device mode: input / host mode: output*

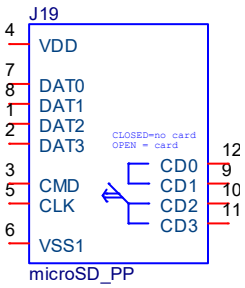
5.3 SD Card

The board provides a push&push connector for Micro SD cards (J19).

Pin	Signal Name	I/O	Voltage	Description
1	SD_A_DATA2	I/O		Serial Data 2
2	SD_A_DATA3	I/O		Serial Data 3
3	SC_A_CMD	O	3.3V	Command
4	VDD_SDCARD	PWR	3.3V	Power
5	SD_A_CLK	O	3.3V	Clock
6	GND			
7	SD_A_DATA0	I/O		Serial Data 0
8	SD_A_DATA1	I/O		Serial Data 1
9	CD1	I		Card Detect 1 [1]
10	CD2	I		Card Detect 2 [1]
11	CD3	I		Card Detect 3 [1]
12	CD0	I		Card Detect 0 [1]

Table 10: SD Card Slot (J19)

Note 1: *CD0, CD1: 49.9R Pull Down*
CD2, CD3: 10k Pull Up to 3.3V



CD0, CD1	CD2, CD3	
CLOSED		no card
OPEN		card

5.4 Feature Connector

The board provides a feature connector (J20) for general purposes (CAN, RS232, I2C, Audio, ADC Input, PWM output, GPIOs).

For HW Revision 1.00 UART_B RXD and TXD are exchanged.

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
1	V33OUT		PWR	3.3 V	3.3 V Output Voltage
2	V5OUT		PWR	5.0 V	5.0 V Output Voltage
3	GPIO0	NAND_CE0_B	I/O	3.3 V	GPIO 0 (4.7k Pull Up)
4	SPI_B_SCLK	ECSPI2_SCLK	O	3.3 V	ECSPI2_SCLK (4.7k Pull Up)
5	GPIO1	NAND_ALE	I/O	3.3 V	GPIO 1 (4.7k Pull Up)
6	SPI_B_SS0	ECSPI2_SS0	O	3.3 V	ECSPI2_SS0 (4.7k Pull Up)
7	GPIO2	NAND_DQS	I/O	3.3 V	GPIO 2 (4.7k Pull Up)
8	SPI_B_MOSI [1] I2C_A_SCL [1]	ECSPI2_MOSI I2C4_SCL	O O	3.3 V 3.3 V	ECSPI2_MOSI (4.7k Pull Up) I2C4_SCL (2.49k Pull Up)
9	GPIO3	NAND_CE3_B	I/O	3.3 V	GPIO 3 (4.7k Pull Up)
10	SPI_B_MISO [1] I2C_A_SDA [1]	ECSPI2_MISO I2C4_SDA	I I/O	3.3 V 3.3 V	ECSPI2_MISO (4.7k Pull Up) I2C4_SDA (2.49k Pull Up)
11	GND				
12	SPI_A_SCLK	UART1_RXD	O	3.3 V	ECSPI1_SCLK (4.7k Pull Up)
13	UART_B_TXD	ECSPI1_SCLK	O	3.3 V	UART3_TXD **Pin is wrong (UART3_RXD)**
14	SPI_A_SS0	UART2_TXD	O	3.3 V	ECSPI1_SS0 (4.7k Pull Up)
15	UART_B_RXD	ECSPI1_MOSI	I	3.3 V	UART3_RXD (100k Pull Up) **Pin is wrong (UART3_TXD)**
16	SPI_A_MOSI	UART1_TXD	O	3.3 V	ECSPI1_MOSI (4.7k Pull Up)
17	SPI_A_MISO	UART2_RXD	I	3.3 V	ECSPI1_MISO (4.7k Pull Up)
18	UART_D_TXD	NAND_DATA01	O	3.3 V	UART4_TXD
19	I2C_C_SCL	ECSPI1_MISO	O	3.3 V	I2C2_SCL | UART3_RTS[2] (2.49k Pull Up)
20	UART_D_RXD	NAND_DATA00	I	3.3 V	UART4_RXD (100k Pull Up)
21	I2C_C_SDA	ECSPI1_SS0	I/O	3.3 V	I2C2_SDA | UART3_CTS [2] (2.49k Pull Up)
22	UART_D_RTS	NAND_DATA02	O	3.3 V	UART4_CTS
23	UART_C_TXD	SAI2_RXFS	O	3.3 V	UART1_TXD
24	UART_D_CTS	NAND_DATA03	I	3.3 V	UART4_RTS
25	UART_C_RXD	SAI2_RXC	I	3.3 V	UART1_RXD (100k Pull Up)
26	GPIO_A	SA3_TXD	I/O	3.3 V	Free GPIO
27	GND				
28	PWM_A	GPIO1_IO13	O	3.3 V	PWM Output
29	AIN_A [3] I2C_D_SDA [3, 4]	- I2C1_SDA	I I/O	3.3 V	Analog In A (opt. AD Converter) I2C1_SDA (2.49k Pull Up)
30	PWM_B	SPDIF_EXT_CLK	O	3.3 V	PWM Output

31	AIN_B [3] I2C_D_SCL [3, 4]	- I2C1_SCL	I O	3.3 V	Analog In B (opt. AD Converter) I2C1_SCL (2.49k Pull Up)
32	PWM_C	SAI3_MCLK	O	3.3 V	PWM Output
33	AIN_C [3] I2C_D_IRQ [3]	- UART4_RXD	I I	3.3 V	Analog In C (opt. AD Converter) I2C_D Interrupt Request
34	BL_ON	SAI3_RXFS	O	3.3 V	Backlight Enable
35	AIN_D [3] I2C_D_RSTn [3]	- UART4_TXD	I O	3.3 V	Analog In D (opt. AD Converter) I2C_D Reset Output
36	RS_RXDBCD	-	I	3.3 V	RS232_RXD [UART_B | UART_C | UART_D] [5]
37	GND				
38	RS_TXDBCD	-	O	3.3 V	RS232_TXD [UART_B | UART_C | UART_D] [5]
39	V33OUT		PWR	3.3 V	3.3 V Output Voltage
40	V5OUT		PWR	5.0 V	5.0 V Output Voltage
41	AUDIO_MICIN		I	3.3 V	Audio Codec MIC Input
42	GND				
43	AUDIO_ MONOUT		O	3.3 V	Audio Codec Mono Out
44	AUDIO_LIN_R		I	3.3 V	Audio Codec Line In – Right
45	AUDIO_LOUT_R		O	3.3 V	Audio Codec Line Out – Right
46	GND				
47	GND				
48	AUDIO_LIN_L		I	3.3 V	Audio Codec Line In – Left
49	AUDIO_LOUT_L		O	3.3 V	Audio Codec Line Out – Left
50	GND				
51	RESETINn_1V8		I	1.8 V	System Reset (100k Pull Up)
52	V33OUT		PWR	3.3 V	
53	SPKR_LOUT_N		O	5.0 V	1W Speaker Out – Left-
54	SPKR_LOUT_P		O	5.0 V	1W Speaker Out – Left+
55	RS_RXDA		I	3.3 V	RS232_RXD [UART_A]
56	RS_RTSA		O	3.3 V	RS232_CTS [UART_A]
57	RS_TXDA		O	3.3 V	RS232_TXD [UART_A]
58	RS_CTSA		I	3.3 V	RS232_RTS [UART_A]
59	SPKR_ROUT_N		O	5.0 V	1W Speaker Out – Right-
60	SPKR_ROUT_P		O	5.0 V	1W Speaker Out – Right+
61	GND				
62	V5OUT		PWR	5.0 V	
63	CAN1L [6] CAN1RX [6]	- SPDIF_RX	I/O I	5.0 V 3.3 V	CAN1L, Optional CAN-FD Transceiver CAN_A_RX, FlexCAN [CPU]

64	CAN1H [6] CAN1TX [6]	- SPDIF_TX	I/O O	5.0 V 3.3 V	CAN1L, Optional CAN-FD Transceiver CAN_A_TX, Flex-CAN [CPU]
65	BOOTSELn_1V8	BOOT_MODE0	I	1.8 V	Boot Select (10k Pull Up) HI -> USB Serial Download (default) LO -> Internal Fuses
66	GND				

Table 11: Feature Connector (J20)

Note 1: *Either I2C or ECSPI. Please contact support@fs-net.de for further information.*

Note 2: *Secondary function. Device tree must be modified to use the secondary functions.*

Note 3: *Either I2C or AD converter.*

Note 4: *I2C_D is shared with internal components. It is recommended to use I2C_D in Master Mode.*

Note 5: *UART_B, UART_C, UART_D can be chosen for RS232 RXD and TXD signals.*

Note 6: *Either FlexCAN from CPU or High Speed CAN (Transceiver). Please contact support@fs-net.de for further information.*

5.5 Ethernet

Depending on the mounting option, the board provides (PHY: RTL8211):

- 2x 10/100/1000Mbit LAN (J7),
- 1x 10/100/1000Mbit LAN (J7, left port only [1]).

Pin	Signal Name	I/O	Voltage	Description
ETH A (J7 left)				
L1	ETH_A_D1N	I/O		ETH A Data1-
L2	ETH_A_D1P	I/O		ETH A Data1+
L3	ETH_A_D2N	I/O		ETH A Data2-
L4	ETH_A_D2P	I/O		ETH A Data2+
L5	ETH_A_D3N	I/O		ETH A Data3-
L6	ETH_A_D3P	I/O		ETH A Data3+
L7	ETH_A_D4N	I/O		ETH A Data4-
L8	ETH_A_D4P	I/O		ETH A Data4+
L9	GND			ETH A CTREF (via 100 nF)
L10	GND			
L11	3.3 V (via 300R)	PWR	3.3 V	ETH A Link LED – Anode
L12	ETH_A_LINK	O		ETH A Link LED – Cathode
L13	ETH_A_ACTIVITY	O		ETH A Activity LED – Anode
L14	GND (via 300R)	PWR		ETH A Activity LED – Cathode
ETH B (J7 right)				
R1	ETH_B_D1N			ETH B Data1-
R2	ETH_B_D1P			ETH B Data1+
R3	ETH_B_D2N			ETH B Data2-
R4	ETH_B_D2P			ETH B Data2+
R5	ETH_B_D3N			ETH B Data3-
R6	ETH_B_D3P			ETH B Data3+
R7	ETH_B_D4N			ETH B Data4-
R8	ETH_B_D4P			ETH B Data4+
R9	GND			ETH B CTREF (via 100 nF)
R10	GND			
R11	3.3 V (via 300R)	PWR	3.3 V	ETH B Link LED – Anode
R12	ETH_B_LINK	O		ETH B Link LED – Cathode
R13	ETH_B_ACTIVITY	O		ETH B Activity LED – Anode
R14	GND (via 300R)	PWR		ETH B Activity LED – Cathode

Table 12: Ethernet (J7)

Note 1: *The right port is not connected in this case.*

5.6 Mini PCI Express

The board provides a Mini PCIe Slot (J13).

Pin	Signal Name	I/O	Voltage	Description
1	mPCIE_WAKE	O		Mini PCIe Wake Signal
2	VDD_3V3	PWR	3.3 V	Supply Voltage for PCIe Card
3	N.C.	X		Not Connected
4	GND			
5	N.C.	X	X	Not Connected
6	VDD_MPCIE_1V5	PWR	1.5 V	Supply Voltage for PCIe Card
7	N.C.	X		Not Connected
8	UIM_PWR	PWR	5.0 V	UIM Power [1]
9	GND			
10	UIM_DATA	I/O		UIM Data (connected to J14)
11	mPCIE_CLK_N	I/O		
12	UIM_CLK	O		UIM Clock (connected to J14)
13	mPCIE_CLK_P	I/O		
14	UIM_RESET	O		UIM Reset (connected to J14)
15	GND			
16	UIM_VPP	PWR		UIM VPP, Connected to J14
17	N.C.	X		Not Connected
18	GND			
19	N.C.	X		Not Connected
20	mPCIE_DISABLE	O		Mini PCIe Disable Signal
21	GND			
22	mPCIE_PERST	O		Mini PCIe Power Enable/Reset Signal
23	mPCIE_CRX_N	I		Mini PCIe Data Receive-
24	VDD_3V3	PWR	3.3 V	
25	mPCIE_CRX_P	I		Mini PCIe Data Receive+
26	GND			
27	GND			
28	VDD_MPCIE_1V5	PWR	1.5 V	Supply Voltage for PCIe Card
29	GND			
30	I2C_SCL	O		Connected to I2C_D_SCL
31	mPCIE_CTX_N	O		Mini PCIe Data Transmit-
32	I2C_SDA	I/O		Connected to I2C_D_SDA
33	mPCIE_CTX_P	O		Mini PCIe Data Transmit+
34	GND			
35	GND			
36	PCIE_USB_DN	I/O		USB Data- (USB Hub Port4)

37	GND			
38	PCIE_USB_DP	I/O		USB Data+ (USB Hub Port4)
39	VDD_3V3	PWR	3.3 V	Supply Voltage for PCIe Card
40	GND			
41	VDD_3V3	PWR	3.3 V	Supply Voltage for PCIe Card
42	LED_WWANn	I	3.3 V	(active HIGH)
43	GND			
44	LED_WLANn	I	3.3V	(active HIGH)
45	N.C.	X		Not Connected
46	LED_WPANn	I	3.3 V	(active HIGH)
47	N.C.	X		Not Connected
48	VDD_MPCIE_1V5	PWR	1.5 V	Supply Voltage for PCIe Card
49	N.C.	X	X	Not Connected
50	GND			
51	N.C.	X		Not Connected
52	VDD_3V3	PWR	3.3 V	Supply Voltage for PCIe Card

Table 13: Mini PCIe (J13)

Note 1: *connected to J14*

5.7 UIM Interface (SIM Card)

The board provides a Nano SIM Card Slot (J14) that can be used with the Mini PCIe Interface.

Pin	Signal Name	I/O	Voltage	Description
1	UIM_PWR	PWR		UIM Supply Voltage (from PCIe Card)
2	UIM_RESET	O		UIM Reset Signal
3	UIM_CLK	O		UIM Clock Signal
4	Reserved	X		
5	GND			
6	UIM_VPP	O		UIM VPP
7	UIM_DATA	I/O		UIM Data In/Out
8	Reserved	X		

Table 14: Nano SIM (J14)

5.8 CAN

The board provides provides up to 2 CAN-FD interfaces. Possible configurations are:

- 2 x High Speed CAN (transceivers: TJA1051),
- FlexCAN (RX/TX) [1].

CAN1 Signals are available on the Feature Connector (J20). CAN2 Signals are available on the CAN Connector (J15).

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
1	VDD		PWR	5.0 V 3.3 V	5.0 V for High Speed CAN 3.3 V for FlexCAN
2	GND				
3	CAN2L CAN2RX	- UART3_TXD	I/O I	5.0 V 3.3 V	LOW Signal (Transceiver) CAN_B_RX Signal (FlexCAN)
4	CAN2H CAN2TX	- UART3_RXD	I/O O	5.0 V 3.3 V	HIGH Signal (Transceiver) CAN_B_TX Signal (FlexCAN)
5	GND				
6	N.C.		X		Not Connected
7	N.C.		X		Not Connected
8	VDD		PWR	5.0 V 3.3 V	5.0 V for High Speed CAN 3.3 V for FlexCAN
9	N.C.		X		Not Connected
10	N.C.		X		Not Connected

Table 15: CAN (J15)

Note 1: *Either High Speed CAN or FlexCAN (transceivers are not mounted in FlexCAN configuration). Please contact support@fs-net.de for further information.*

5.9 HDMI/DVI

The board provides an HDMI / DVI interface [1] with up to 4K resolution (J11).

Pin	Signal Name	I/O	Voltage	Description
1	HDMI_CN_TXD2_P	O		Data Lane2+
2	D2_SHIELD			Shield Data Lane2
3	HDMI_CN_TXD2_N	O		Data Lane2-
4	HDMI_CN_TXD1_P	O		Data Lane1+
5	D1_SHIELD			Shield Data Lane1
6	HDMI_CN_TXD1_N	O		Data Lane1-
7	HDMI_CN_TXD0_P	O		Data Lane0+
8	D0_SHIELD			Shield Data Lane0
9	HDMI_CN_TXD0_N	O		Data Lane0-
10	HDMI_CN_CLK_P	O		Clock Lane+

11	CLK_SHIELD			Shield Clock Lane
12	HDMI_CN_CLK_N	O		HDMI Clock Lane-
13	HDMI_CN_CEC			
14	HDMI_CN_UTIL	O		Utility Output
15	HDMI_CN_DDC_SCL	O		DDC I2C Clock
16	HDMI_CN_DDC_SDA	I/O		DDC I2C Data
17	GND			
18	+5VS_HDMI	PWR	5.0 V	Supply Voltage
19	HDMI_CN_HPD	I		Hot Plug Detect

Table 16: HDMI/DVI (J11)

Note 1: *ESD protected*

5.10 MIPI-DSI & LVDS

Depending on the mounting option, the board provides MIPI-DSI and/or LVDS (J9):

- Option1 [1]: 1x 4-lane MIPI-DSI (Channel A) & 1x 4-lane LVDS (Channel B),
- Option2: 1x 8-lane LVDS (Channel A & B) – for larger displays.

Pin	Signal Name	I/O	Voltage	Description
1	MIPI_DSI1_D0_N LVDS0_D0_N	O		Channel A Data Lane0-
2	MIPI_DSI1_D0_P LVDS0_D0_P	O		Channel A Data Lane0+
3	MIPI_DSI1_D1_N LVDS0_D1_N	O		Channel A Data Lane1-
4	MIPI_DSI1_D1_P LVDS0_D1_P	O		Channel A Data Lane1+
5	MIPI_DSI1_D2_N LVDS0_D2_N	O		Channel A Data Lane2-
6	MIPI_DSI1_D2_P LVDS0_D2_P	O		Channel A Data Lane2+
7	GND			
8	MIPI_DSI1_CLK_N LVDS0_CLK_N	O		Channel A Clock Lane-
9	MIPI_DSI1_CLK_P LVDS0_CLK_P	O		Channel A Clock Lane+
10	MIPI_DSI1_D3_N LVDS0_D3_N	O		Channel A Data Lane3-
11	MIPI_DSI1_D3_P LVDS0_D3_P	O		Channel A Data Lane3+
12	LVDS1_D0_N	O		Channel B Data Lane0-
13	LVDS1_D0_P	O		Channel B Data Lane0+
14	GND			

15	LVDS1_D1_N	O		Channel B Data Lane1-
16	LVDS1_D1_P	O		Channel B Data Lane1+
17	GND			
18	LVDS1_D2_N	O		Channel B Data Lane2-
19	LVDS1_D2_P	O		Channel B Data Lane2+
20	LVDS1_CLK_N	O		Channel B Clock Lane-
21	LVDS1_CLK_P	O		Channel B Clock Lane+
22	LVDS1_D3_N	O		Channel B Data Lane3-
23	LVDS1_D3_P	O		Channel B Data Lane3+
24	GND			
25	I2C_B_SDA	I/O	3.3 V	I2C Serial Data (I2C3_SDA, Touch Controller)
26	I2C_B_IRQ	I	3.3 V	I2C Interrupt Request (GPIO1_IO07, Touch Controller)
27	I2C_B_SCL	O	3.3 V	I2C Serial Clock (I2C3_SCL, Touch Controller)
28	LVDS_RSTn	O	3.3 V	Reset Out (GPIO1_IO15, Touch Controller)
29	VLCD	PWR O	3.3 V 5.0 V	LCD Supply Voltage [2,3]
30	VLCD	PWR O	3.3 V 5.0 V	LCD Supply Voltage [2,3]

Table 17: MIPI-DSI/LVDS (J9)

Note 1: *Default option. For ordering option 2, please contact our sales team.*
Note 2: *LCD Voltage depends on the mounting option.*
Note 3 *VLCD can't be switched in HW Revision 1.00*

5.11 Touch Interface

In addition to J9, the board provides a dedicated connection for a touch controller (J18), communicating via I2C.

Pin	Signal Name	I/O	Voltage	Description
1	VDD_3V3	PWR	3.3 V	Supply Voltage
2	I2C_B_SDA	I/O	3.3 V	I2C Serial Data (I2C3_SDA)
3	I2C_B_SCL	O	3.3 V	I2C Serial Clock (I2C3_SCL)
4	TOUCH_RSTn	O	3.3 V	Reset Out (GPIO1_IO15)
5	I2C_B_IRQ	I	3.3 V	I2C Interrupt Request (GPIO1_IO07)
6	GND			

Table 18: Touch (J18)

5.12 Backlight Interface

The board provides a 4-pin connector for the control of LCD voltage and backlight (J10).

Pin	Signal Name	I/O	Voltage	Description
1	VLCD_ON	O	3.3 V	VLCD Enable
2	BL_ON	O	3.3 V	Backlight Enable
3	BL_PWM	O	3.3 V	Backlight PWM
4	GND			

Table 19: Backlight (J18)

5.13 MIPI-CSI

The board provides a 1x4-lane MIPI CSI interface (J12).

Pin	Signal Name	I/O	Voltage	Description
1	GND			
2	CSI_A_DATA3_P	I		Data Lane3+
3	CSI_A_DATA3_N	I		Data Lane3-
4	GND			
5	CSI_A_DATA2_P	I		Data Lane2+
6	CSI_A_DATA2_N	I		Data Lane2-
7	GND			
8	CSI_A_CLK_P	I		Clock Lane+
9	CSI_A_CLK_N	I		Clock Lane-
10	GND			
11	CSI_A_DATA1_P	I		Data Lane1+
12	CSI_A_DATA1_N	I		Data Lane1-
13	GND			
14	CSI_A_DATA0_P	I		Data Lane0+
15	CSI_A_DATA0_N	I		Data Lane0-
16	GND			
17	N.C.	X		Not Connected
18	N.C.	X		Not Connected
19	GND			
20	I2C_D_SCL	O	1.8V	I2C Serial Clock (I2C1_SCL, voltage level shifted to 1.8 V)
21	I2C_D_SDA	I/O	1.8V	I2C Serial Data (I2C1_SDA, voltage level shifted to 1.8 V)
22	GND			
23	N.C.	X		Not Connected
24	N.C.	X		Not Connected

25	+5VS	PWR	5.0 V	Camera Supply Voltage
26	+5VS	PWR	5.0 V	Camera Supply Voltage
27	+5VS	PWR	5.0 V	Camera Supply Voltage
28	GND			

Table 20: MIPI-CSI (J12)

5.14 WLAN and Bluetooth Interface

The board contains a high performance WLAN and BT module [1, 2, 3] (based on NXP W8997), supporting:

- IEEE802.11 ac/a/b/g/n,
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy).

Note 1: *CE, FCC, IC, NCC, AU/NZ, India, Japan certificates available.*

Note 2: *Please contact support@fs-net.de for additional information about process of certification.*

Note 3: *Refer to the following BT QDID info for 88W8997 (AW-CM276NF).*

QDID: D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

5.15 JTAG

The board provides a JTAG connection (J1) for debug purposes [1, 2].

Pin	Signal Name	I/O	Voltage	Description
1	JTAG_VTREF	PWR	1.8V	Reference for JTAG Debug Adapter
2	JTAG_TMS	I	1.8V	JTAG Test Mode Select (10k Pull Up)
3	GND			
4	JTAG_TCK	I	1.8V	JTAG Test Clock (10k Pull Up)
5	GND			
6	JTAG_TDO	O	1.8V	JTAG Test Data Out (10k Pull Up)
7	N.C.	X		Not Connected
8	JTAG_TDI	I	1.8V	JTAG Test Data In (10k Pull Up)
9	GND			
10	RESETINn_1V8	I	1.8V	System Reset (Connected to Reset Button)

Table 21: JTAG (J1)

Note 1: *Leave unconnected if you don't use JTAG.*

Note 2: *Don't use a JTAG chain, because different power sequence and power level could kill the CPU.*

5.16 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up.

On a non-powered board, it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

5.17 System Reset

A system reset can be initiated by either pushing the reset button (beside the Nano SIM Card Slot) or applying 0V to pin 51 on the Feature Connector (J20).

5.18 Indicator LEDs

The board provides seven LEDs which indicate the status of the functions listed below.

LED	Description
1	WPAN active on PCIe Card
2	WLAN active on PCIe Card
3	WWAN active on PCIe Card
4	3.3V
5	WLAN active on WLAN/BT Module
6	BT active on WLAN/BT Module
7	5V

Figure 7: Indicator LEDs (Description)

6 eMMC

The armStone™MX8MP support eMMC flash memory. The eMMC technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of eMMC [1], independent if the device is powered or not.

Note 1: *Please contact support@fs-net.de if your device is constantly in an environment where temperature is higher than 50°C.*

7 Real Time Clock (RTC)

A NXP PCF85263ATL or a compatible RTC [1] is implemented on the board.

Note 1: *The accuracy of the RTC is limited by the crystal (e.g. frequency drift due to warming) and could drift some seconds per day.*

8 Secure Authenticator IC

The secure tamper-resistant authentication IC (NXP EdgeLock™ SE050 [1]) offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and/or customer safety [2].

Note 1: *This component is optional and not mounted in all configurations. Please contact sales to get more information.*

Note 2: *For more information visit NXPs website.*

9 Thermal Specification

The following table shows the nominal thermal specifications [1, 2] for the armStone™MX8MP.

Description	Min	Typ	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature [3]	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		**t.b.d.**	°C
Industrial Range CPU Junction Temperature [3] (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		**t.b.d.**	°C
Extended Industrial Range CPU Junction Temperature [3] (XI)	-40		+105	°C
Junction to Package Top **(Ψ_{JT})**		0.98		°C/W

Table 22: armStone™MX8MP (Thermal Specs)

Note 1: *Cooling is necessary and highly recommended near the limits. Please contact support@fs-net.de for recommended cooling solutions.*

Note 2: *WLAN/BT is -30°C to +85°C only.*

Note 3: *Life expectancy of the CPU is shortened by high temperatures.*
Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf).

10 Power consumption and cooling

The power consumption differs, depending on the product version and usage. The maximum power consumption could be up to **t.b.d.** W [1], but, depending on your specific application, will be much lower in most cases [2].

This Embedded Module is a high-performance computing system. With respect to the system performance and lifetime, an appropriate cooling solution must be established. A general statement for such a solution is not possible, because it depends on many factors (e. g. housing, power consumption (including other components like power supply and LCD inside the system), ambient temperature, airflow, …).

At least the following topics should be considered:

- The heat production highly depends on the usage of CPU [3, 4] and GPU and therefore on customers software application (use peak performance only for short times).
- Just cooling the CPU (70-90% power consumption of the entire board) is the best way to cool the board.
- The ambient temperature has a big effect to the temperature of the system.
- The housing has a big influence on the heat dissipation. Analyze:
  - Is there an option of dissipating heat to the housing?
  - Is there a possibility that the air can circulate / flow inside the housing?
  - Is an active cooling possible?

For calculating your cooling solution, we recommend this helpful literature:

- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction! For an optimal cooling performance we recommend to use F&S heat spreader, designed for armStone™MX8MP (MHS.AS8MP.1).

Note 1:	*This value considers all cores and GPU at full load. Generally, this scenario needs an extensive cooling.*
Note 2:	*We recommend to measure the max. power consumption in your specific application.*
Note 3:	*The CPU offers a "Dynamic Voltage and Frequency Scaling" (DVFS):* *CPU clock and core voltage are lowered, according to the performance, needed from the application.*
Note 4:	*The CPU offers a "Thermal Throttling":* *An integrated sensor measures the die-temperature and lowers CPU clock / shut down CPU if the die-temperature rises above defined values.*

11 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

12 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags. The boards are shipped in cartons. One carton can hold 30 boards.

13 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 8: Matrix Code Sticker

14 ADP-NT24V2

F&S provides the ADP-NT24V2 power adapter to power the armStone™MX8MP with 7.5-36V input voltage:

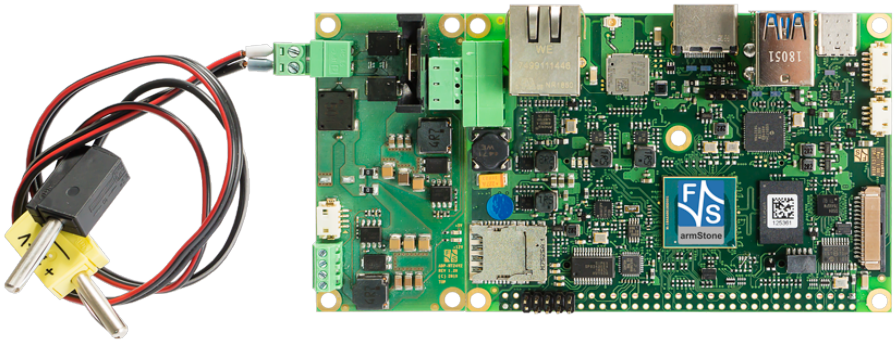


Figure 9: ADP-NT24V2 connected to the armStone™ Module

For more information check the F&S website:

https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/

15 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

16 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

17 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

18 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

F&S reserves the right to make changes in its products or product specifications or product documentation with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

F&S makes no warranty or guarantee regarding the suitability of its products for any particular purpose, nor does F&S assume any liability arising out of the documentation or use of any product and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

Products are not designed, intended, or authorized for use as components in systems intended for applications intended to support or sustain life, or for any other application in which the failure of the product from F&S could create a situation where personal injury or death may occur. Should the Buyer purchase or use a F&S product for any such unintended or unauthorized application, the Buyer shall indemnify and hold F&S and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that F&S was negligent regarding the design or manufacture of said product.

Specifications are subject to change without notice.

Warranty Terms

Hardware Warranties

F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S's sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Software Warranties

Software is provided "AS IS". F&S makes no warranties, either express or implied, with regard to the software object code or software source code either or with respect to any third party materials or intellectual property obtained from third parties. F&S makes no warranty that the software is useable or fit for any particular purpose. This warranty replaces all other warranties written or unwritten. F&S expressly disclaims any such warranties. In no case shall F&S be liable for any consequential damages.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN PLACE OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL F&S BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL F&S BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE PRODUCT, THE CUSTOMER APPROVES THAT THE F&S PRODUCT, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS

19 Content