Hardware Documentation

SolderCore8ULP
for HW Revision 1.00

preliminary

Version 001
(2023-03-27)

Elektronik Systeme

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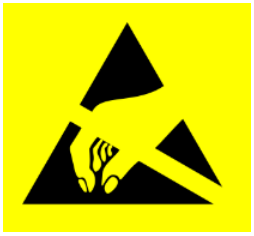
About This Document

This document describes how to use the SolderCore8ULP SOM with mechanical and electrical information. The latest version of this document can be found at: http://www.fs-net.de.

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
23.03.23	001		-	All	Initial Version	DB

V	Version
A, M, R	Added, Modified, Removed
Au	Author

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1 Overview

The SolderCore8ULP is solder down SOM with the NXP i.MX8ULP Processor. It is designed for maximum flexibility and lowest power consumption. It has a LGA to connect to the base board. It contains only the minimum necessary components (processor, RAM, eMMC, PMIC). All I/O pins of the processor (except pins used by onboard eMMC and PMIC) can be used for the application without restrictions. It is designed to be used with a 4-layer base board.

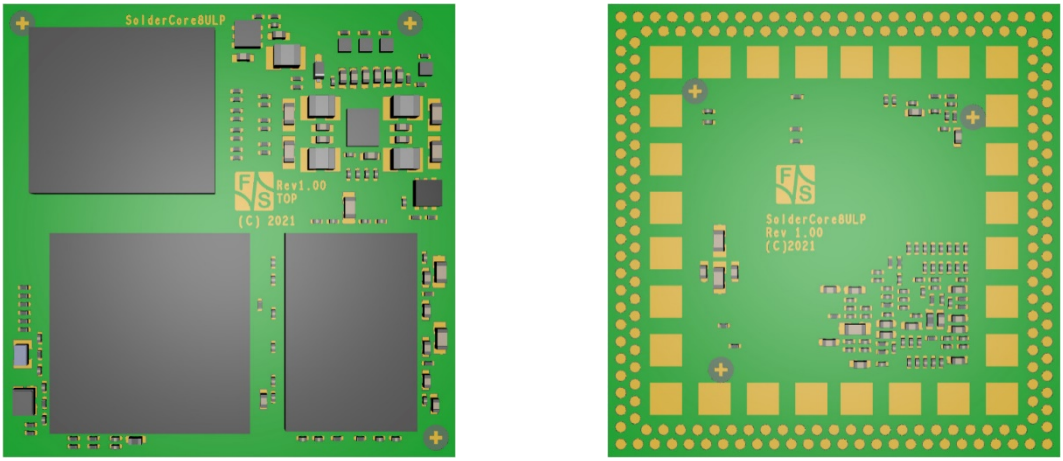

Figure 1: SolderCore8ULP

2 Mechanical

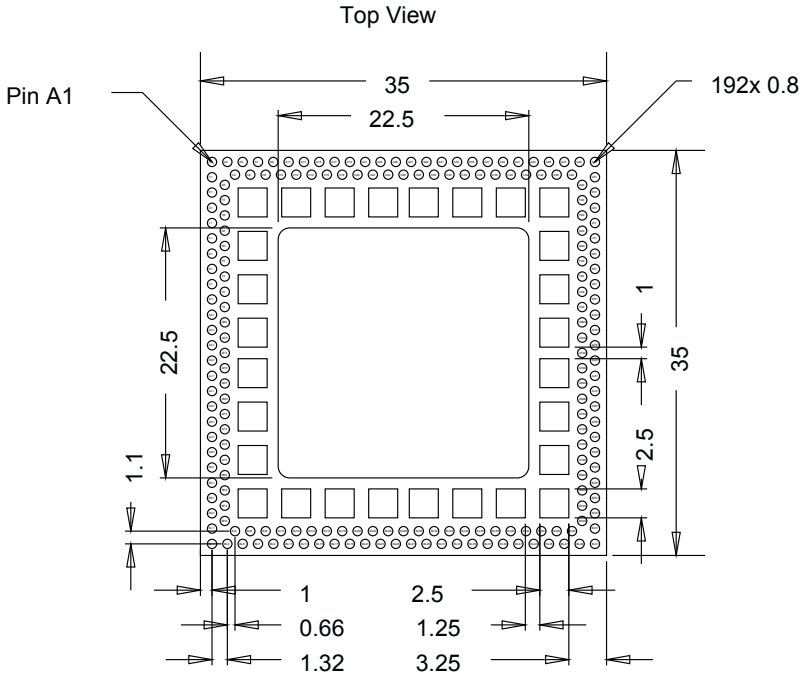

Figure 2: Pad layout

The SolderCore8ULP has components on the back side and needs a 22.5mm x 22.5mm cutout in the carrier board.

3 Additonal Documentation

The SolderCore8ULP is a very versatile SOM. It is recommended to read the documentation for the processor and PMIC:

i.MX 8ULP Applications Processor Family

PCA9460 PMIC for Ultra Low Power Application

4 Module Pin Out

Pin	Signal Name	Type	Voltage	Description
A1	PTD23	GPIO	1.8V/3.3V	
A3	PTD22	GPIO	1.8V/3.3V	
C4	PTD21	GPIO	1.8V/3.3V	
A5	PTD20	GPIO	1.8V/3.3V	
C6	PTD19	GPIO	1.8V/3.3V	
A7	PTD18	GPIO	1.8V/3.3V	
C8	PTD17	GPIO	1.8V/3.3V	
A9	PTD16	GPIO	1.8V/3.3V	
C10	PTD15	GPIO	1.8V/3.3V	
A11	PTD14	GPIO	1.8V/3.3V	
C12	PTD13	GPIO	1.8V/3.3V	
A13	PTD12	GPIO	1.8V/3.3V	
C14	CSI_DATA1_N	MIPI		
A15	CSI_DATA1_P	MIPI		
C16	CSI_CLK_N	MIPI		
A17	CSI_CLK_P	MIPI		
C18	CSI_DATA0_N	MIPI		
A19	CSI_DATA0_P	MIPI		
C20	DSI_DATA3_N	MIPI		
A21	DSI_DATA3_P	MIPI		
C22	DSI_DATA1_N	MIPI		
A23	DSI_DATA1_P	MIPI		
C24	DSI_CLK_N	MIPI		
A25	DSI_CLK_P	MIPI		
C26	DSI_DATA0_N	MIPI		
A27	DSI_DATA0_P	MIPI		
C28	DSI_DATA2_N	MIPI		
A29	DSI_DATA2_P	MIPI		
C30	VDD_PTA_1V8	PWR Out	1.8V	PTA Power Supply
A31	VDD_PTA_IN	PWR In	1.8V/3.3V	PTA Power Supply
C32	VDD_PTA_3V3	PWR Out	3.3V	PTA Power Supply
A33	NC			Not connected
C34	VDD_PTB	PWR Out	1.8V	PTB Power Supply
C35	NC			Not connected
C36	VDD_PTC_1V8	PWR Out	1.8V	PTC Power Supply
A37	VDD_PTC_IN	PWR In	1.8V/3.3V	PTC Power Supply

Pin	Signal Name	Type	Voltage	Description
C38	VDD_PTC_3V3	PWR Out	3.3V	PTC Power Supply
A39	VDD_PTD_1V8	PWR Out	1.8V	PTD Power Supply
C40	VDD_PTD_IN	PWR In	1.8V/3.3V	PTD Power Supply [4]
A41	VDD_PTD_3V3	PWR Out	3.3V	PTD Power Supply
C42	VDD_PTE_1V8	PWR Out	1.8V	PTE Power Supply
A43	VDD_PTE_IN	PWR In	1.8V/3.3V	PTE Power Supply
C44	VDD_PTE_3V3	PWR Out	3.3V	PTE Power Supply
A45	VDD_PTF_1V8	PWR Out	1.8V	PTF Power Supply
C46	VDD_PTF_IN	PWR In	1.8V/3.3V	PTF Power Supply
A47	VDD_PTF_3V3	PWR Out	3.3V	PTF Power Supply
C48	VSYS_IN	PWR In	5V	System Power Supply
A49	VSYS_IN	PWR In	5V	System Power Supply
A51	VSYS_IN	PWR In	5V	System Power Supply
C51	VSYS_IN	PWR In	5V	System Power Supply
D49	LICELL	PWR In/Out	3V	Supply for Battery Backed Secure Module
E51	SYS_RST_B	Input	[1]	PMIC Reset In
F49	PMIC_WDOG_B	Input	[2]	PMIC Watchdog In
G51	PMIC_ACOK_B	Input	[1]	PMIC ACOK In
H49	PMIC_IRQ_B	Output	[3]	PMIC Interrupt Request
J51	NC			Not connected
K49	PTE23	GPIO	1.8V/3.3V	
L51	PTE22	GPIO	1.8V/3.3V	
M49	PTE21	GPIO	1.8V/3.3V	
N51	PTE20	GPIO	1.8V/3.3V	
P49	PTE19	GPIO	1.8V/3.3V	
R51	PTE18	GPIO	1.8V/3.3V	
T49	PTE17	GPIO	1.8V/3.3V	
U51	PTE16	GPIO	1.8V/3.3V	
V49	PTE15	GPIO	1.8V/3.3V	
W51	PTE14	GPIO	1.8V/3.3V	
Y49	PTE13	GPIO	1.8V/3.3V	
AA51	PTE12	GPIO	1.8V/3.3V	
AB49	PTE11	GPIO	1.8V/3.3V	
AC51	PTE10	GPIO	1.8V/3.3V	
AD49	PTE9	GPIO	1.8V/3.3V	
AE51	PTE8	GPIO	1.8V/3.3V	
AF49	PTE7	GPIO	1.8V/3.3V	
AG51	PTE6	GPIO	1.8V/3.3V	

Pin	Signal Name	Type	Voltage	Description
AH49	PTE5	GPIO	1.8V/3.3V	
AJ51	PTE4	GPIO	1.8V/3.3V	
AK49	PTE3	GPIO	1.8V/3.3V	
AL51	PTE2	GPIO	1.8V/3.3V	
AM49	PTE1	GPIO	1.8V/3.3V	
AN51	PTE0	GPIO	1.8V/3.3V	
AP49	PTC23	GPIO	1.8V/3.3V	
AR51	PTC22	GPIO	1.8V/3.3V	
AT49	PTC21	GPIO	1.8V/3.3V	
AU51	PTC20	GPIO	1.8V/3.3V	
AV49	PTC19	GPIO	1.8V/3.3V	
AW51	PTC18	GPIO	1.8V/3.3V	
AY49	PTC17	GPIO	1.8V/3.3V	
BA51	PTC16	GPIO	1.8V/3.3V	
BB49	PTC15	GPIO	1.8V/3.3V	
BC51	PTC14	GPIO	1.8V/3.3V	
BD49	PTC13	GPIO	1.8V/3.3V	
BE51	PTC12	GPIO	1.8V/3.3V	
BF49	PTC11	GPIO	1.8V/3.3V	
BG51	PTC10	GPIO	1.8V/3.3V	
BH49	PTC9	GPIO	1.8V/3.3V	
BJ51	PTC8	GPIO	1.8V/3.3V	
BL51	PTC7	GPIO	1.8V/3.3V	
BL49	PTC6	GPIO	1.8V/3.3V	
BJ48	PTC5	GPIO	1.8V/3.3V	
BL47	PTC4	GPIO	1.8V/3.3V	
BJ46	PTC3	GPIO	1.8V/3.3V	
BL45	PTC2	GPIO	1.8V/3.3V	
BJ44	PTC1	GPIO	1.8V/3.3V	
BL43	PTC0	GPIO	1.8V/3.3V	
BJ42	PTB15	GPIO	1.8V	
BL41	PTB14	GPIO	1.8V	
BJ40	PTB13	GPIO	1.8V	
BL39	PTB12	GPIO	1.8V	
BJ38	PTB11	GPIO	1.8V	
BL37	PTB10	GPIO	1.8V	
BJ36	PTB9	GPIO	1.8V	
BL35	PTB8	GPIO	1.8V	

Pin	Signal Name	Type	Voltage	Description
BJ34	PTB7	GPIO	1.8V	
BL33	PTB6	GPIO	1.8V	
BJ32	PTB5	GPIO	1.8V	
BL31	PTB4	GPIO	1.8V	
BJ30	PTB3	GPIO	1.8V	
BL29	PTB2	GPIO	1.8V	
BJ28	PTB1	GPIO	1.8V	
BL27	PTB0	GPIO	1.8V	
BJ26	PTA24	GPIO	1.8V/3.3V	
BL25	PTA23	GPIO	1.8V/3.3V	
BJ24	PTA22	GPIO	1.8V/3.3V	
BL23	PTA21	GPIO	1.8V/3.3V	
BJ22	PTA20	GPIO	1.8V/3.3V	
BL21	PTA19	GPIO	1.8V/3.3V	
BJ20	PTA18	GPIO	1.8V/3.3V	
BL19	PTA17	GPIO	1.8V/3.3V	
BJ18	PTA16	GPIO	1.8V/3.3V	
BL17	PTA15	GPIO	1.8V/3.3V	
BJ16	PTA14	GPIO	1.8V/3.3V	
BL15	PTA13	GPIO	1.8V/3.3V	
BJ14	PTA12	GPIO	1.8V/3.3V	
BL13	PTA11	GPIO	1.8V/3.3V	
BJ12	PTA10	GPIO	1.8V/3.3V	
BL11	PTA9	GPIO	1.8V/3.3V	
BJ10	PTA8	GPIO	1.8V/3.3V	
BL9	PTA7	GPIO	1.8V/3.3V	
BJ8	PTA6	GPIO	1.8V/3.3V	
BL7	PTA5	GPIO	1.8V/3.3V	
BJ6	PTA4	GPIO	1.8V/3.3V	
BL5	PTA3	GPIO	1.8V/3.3V	
BJ4	PTA2	GPIO	1.8V/3.3V	
BL3	PTA1	GPIO	1.8V/3.3V	
BL1	PTA0	GPIO	1.8V/3.3V	
BJ1	DAC1_OUT	Analog	1.8V	
BH3	DAC0_OUT	Analog	1.8V	
BG1	BOOT_MODE1	Input	1.8V/3.3V	VDD_PTA
BF3	BOOT_MODE0	Input	1.8V/3.3V	VDD_PTA
BE1	RESET0_B	I/O	1.8V	

Pin	Signal Name	Type	Voltage	Description
BD3	RESET1_B	I/O	1.8V	
BC1	ONOFF	Input	1.8V	
BB3	TAMPER1	Input	1.8V	
BA1	TAMPER0	Input	1.8V	
AY3	USB1_DM	USB		
AW1	USB1_DP	USB		
AV3	USB1_VBUS_DETECT	Analog	5V	
AU1	USB0_VBUS_DETECT	Analog	5V	
AT3	USB0_DM	USB		
AR1	USB0_DP	USB		
AP3	PTF31	GPIO	1.8V/3.3V	
AN1	PTF30	GPIO	1.8V/3.3V	
AM3	PTF29	GPIO	1.8V/3.3V	
AL1	PTF28	GPIO	1.8V/3.3V	
AK3	PTF27	GPIO	1.8V/3.3V	
AJ1	PTF26	GPIO	1.8V/3.3V	
AH3	PTF25	GPIO	1.8V/3.3V	
AG1	PTF24	GPIO	1.8V/3.3V	
AF3	PTF23	GPIO	1.8V/3.3V	
AE1	PTF22	GPIO	1.8V/3.3V	
AD3	PTF21	GPIO	1.8V/3.3V	
AC1	PTF20	GPIO	1.8V/3.3V	
AB3	PTF19	GPIO	1.8V/3.3V	
AA1	PTF18	GPIO	1.8V/3.3V	
Y3	PTF17	GPIO	1.8V/3.3V	
W1	PTF16	GPIO	1.8V/3.3V	
V3	PTF15	GPIO	1.8V/3.3V	
U1	PTF14	GPIO	1.8V/3.3V	
T3	PTF13	GPIO	1.8V/3.3V	
R1	PTF12	GPIO	1.8V/3.3V	
P3	PTF11	GPIO	1.8V/3.3V	
N1	PTF10	GPIO	1.8V/3.3V	
M3	PTF9	GPIO	1.8V/3.3V	
L1	PTF8	GPIO	1.8V/3.3V	
K3	PTF7	GPIO	1.8V/3.3V	
J1	PTF6	GPIO	1.8V/3.3V	
H3	PTF5	GPIO	1.8V/3.3V	
G1	PTF4	GPIO	1.8V/3.3V	

Pin	Signal Name	Type	Voltage	Description
F3	PTF3	GPIO	1.8V/3.3V	
E1	PTF2	GPIO	1.8V/3.3V	
D3	PTF1	GPIO	1.8V/3.3V	
C1	PTF0	GPIO	1.8V/3.3V	

[1] 100k Pull-Up to VSYS
[2] Input High Level > 1.4V, max. voltage: VSYS
[3] Open-Drain, max. voltage: VSYS
[4] HS mode for eMMC is not supported if 3.3V is used

Table 1: Module Pin Out

5 Pin Description

5.1 Power

The SolderCore8ULP has a main power supply input (VSYS_IN) and an Always On supply input (LICELL).

LICELL can be connected to a Lithium Coin Cell to supply the BBSM voltage. Use a diode to prevent current flow into the battery if using a non-rechargeable type.

The voltages for the I/O Power Domains can be configured for 1.8V or 3.3V (PTB is 1.8V only).

When all Power Domains are 1.8V the VSYS input voltage can be as low as 2.7V (special configuration required, available on request).

Each I/O Power Domain VDD_PTx_IN must be connected to either VDD_PTx_1V8 or VDD_PTx_3V3. Do not connect to other voltages. VDD_PTB is always 1.8V.

VDD_PTx_IN and VDD_PTB can be used to supply pull-ups on the corresponding I/O pins on the carrier board. If other voltages are used, leakage currents can occur and the processor can be damaged.

VDD_PTA_1V8	Connect either VDD_PTA_1V8 or VDD_PTA_3V3 to VDD_PTA_IN. VDD_PTA_IN can be used to supply pull-ups on the PTA dower domain pins.
VDD_PTA_IN	
VDD_PTA_3V3	
VDD_PTB	1.8V only
VDD_PTC_1V8	Connect either VDD_PTC_1V8 or VDD_PTC_3V3 to VDD_PTC_IN. VDD_PTC_IN can be used to supply pull-ups on the PTC dower domain pins.
VDD_PTC_IN	
VDD_PTC_3V3	
VDD_PTD_1V8	Connect either VDD_PTD_1V8 or VDD_PTD_3V3 to VDD_PTD_IN. VDD_PTD_IN can be used to supply pull-ups on the PTD dower domain pins. PTD is used for internal eMMC. Use 1.8V for maximum performance. HS Mode is not supported for 3.3V
VDD_PTD_IN	
VDD_PTD_3V3	
VDD_PTE_1V8	Connect either VDD_PTE_1V8 or VDD_PTE_3V3 to VDD_PTE_IN. VDD_PTE_IN can be used to supply pull-ups on the PTE dower domain pins.
VDD_PTE_IN	
VDD_PTE_3V3	
VDD_PTF_1V8	Connect either VDD_PTF_1V8 or VDD_PTF_3V3 to VDD_PTF_IN. VDD_PTF_IN can be used to supply pull-ups on the PTF dower domain pins.
VDD_PTF_IN	
VDD_PTF_3V3	
VSYS_IN	System Power Supply
LICELL	Supply for Battery Backed Secure Module

5.2 Control

There are two versions of the SolderCore8ULP available with different connections to the PMIC. Either PTB or PTA can be used for PMIC control (PTA version available on request).

Signal.	Description	Comment
SYS_RST_B	PMIC reset input pin.	Connect to reset generator
PMIC_WDOG_B	PMIC Watchdog reset input from application processor.	Route externally to GPIO if needed
PMIC_ACOK_B	PMIC ON signal	See PCA9460A Manual
PMIC_IRQ_B	PMIC interrupt pin.	Open drain output requiring external pull up resistor Route externally to GPIO if needed
BOOT_MODE0 BOOT_MODE1	Boot Mode selection pins.	Pulled low internally. Boot Mode “00” (boot from fuses) is the preferred mode. For recovery Boot Mode “01” or “11” (serial downloader) is needed.
ONOFF	Power Button	See Reference Manual
RESET0_B	M33 reset signal	Connected to PMIC POR_B
RESET1_B	A35 reset signal	
TAMPER0 TAMPER1	Tamper detection pins	See Reference Manual

5.3 GPIO

GPIO pins are connected directly to the processor.

Please see i.MX 8ULP Processor Reference Manual and Data Sheet for detailed pin descriptions.

5.4 USB

Pin.	Description	Comment
AT3	USB0_DM	Leave open if not used
AR1	USB0_DP	Leave open if not used
AU1	USB0_VBUS_DETECT	Leave open if not used
AY3	USB1_DM	Leave open if not used
AW1	USB1_DP	Leave open if not used
AV3	USB1_VBUS_DETECT	Leave open if not used

Table 2: Pins used for USB

5.5 MIPI-CSI

Pin.	Description	Comment
C18	CSI_DATA0_N	Leave open if not used
A19	CSI_DATA0_P	Leave open if not used
C14	CSI_DATA1_N	Leave open if not used
A15	CSI_DATA1_P	Leave open if not used
C16	CSI_CLK_N	Leave open if not used
A17	CSI_CLK_P	Leave open if not used

Table 3: Pins used for MIPI-CSI

5.6 MIPI-DSI

Pin.	Description	Comment
C26	DSI_DATA0_N	Leave open if not used
A27	DSI_DATA0_P	Leave open if not used
C22	DSI_DATA1_N	Leave open if not used
A23	DSI_DATA1_P	Leave open if not used
C28	DSI_DATA2_N	Leave open if not used
A29	DSI_DATA2_P	Leave open if not used
C20	DSI_DATA3_N	Leave open if not used
A21	DSI_DATA3_P	Leave open if not used
C24	DSI_CLK_N	Leave open if not used
A25	DSI_CLK_P	Leave open if not used

Table 4: Pins used for MIPI-DSI

5.7 Internally used pins

The following pins are used internally and cannot be used externally.

Used for internal eMMC:

Pin.	Description	Comment
PTD0	SDHC0_RESET	Not routed to pads

PTD1	SDHC0_CMD	Not routed to pads
PTD2	SDHC0_CLK	Not routed to pads
PTD3	SDHC_D7	Not routed to pads
PTD4	SDHC_D6	Not routed to pads
PTD5	SDHC_D5	Not routed to pads
PTD6	SDHC_D4	Not routed to pads
PTD7	SDHC_D3	Not routed to pads
PTD8	SDHC_D2	Not routed to pads
PTD9	SDHC_D1	Not routed to pads
PTD10	SDHC_D0	Not routed to pads
PTD11	SDHC_DQS	Not routed to pads

Table 5: Pins used for eMMC

There are two options for the PMIC connection using the pins on PTA or PTB. This is a hardware option, PTB is standard version, PTA version is available on request. The used pins must not be used as GPIO.

Pin.	Description	Comment
PTB7	PMIC_MODE2	Do not use as GPIO pin
PTB8	PMIC_MODE1	Do not use as GPIO pin
PTB9	PMIC_MODE0	Do not use as GPIO pin
PTB10	PMIC_I2C_SDA	Do not use as GPIO pin
PTB11	PMIC_I2C_SCL	Do not use as GPIO pin

Table 6: Pins used for PMIC, PTB version, default

Pin.	Description	Comment
PTA3	PMIC_MODE2	Do not use as GPIO pin
PTA4	PMIC_MODE1	Do not use as GPIO pin
PTA8	PMIC_MODE0	Do not use as GPIO pin
PTA12	PMIC_I2C_SDA	Do not use as GPIO pin
PTA13	PMIC_I2C_SCL	Do not use as GPIO pin

Table 7: Pins used for PMIC, PTA version

5.8 Required connections for operation

The following connections must be established to use the module:

- VSYS must be present.
- VDD_PTD_IN must be connected to VDD_PTD_1V8 or VDD_PTD_3V3 (to boot from eMMC)
- When using PTA option for PMIC VDD_PTA_IN must be connected to VDD_PTA_1V8 or VDD_PTA_3V3

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter.	Description	Min	Max	Unit
VSYS	Main Power Supply	-0.5	6.0	V
LICELL	Backup Battery	-0.3	4.5	V
USBx_VBUS_DETCET	USB Voltage detection	-0.3	5.6	V
SYS_RST_B PMIC_WDOG_B PMIC_ACOK_B PMIC_IRQ_B		-0.5	VSYS+0.5	V

Table 8: Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Parameter.	Description	Min	Typ.	Max	Unit
VSYS	Main Power Supply	2.7[1)]	5.0	5.5	V
LICELL	Backup Battery	2.4	3.0	4.5	V

[1)] PMIC has to be configured for this voltage, 1.8V operation only.

Table 9: Recommended Operation Conditions

7 Customer Specific Mounting Options

Customer specific mounting options are available on request. Please contact sales@fs-net.de for more information.

8 ESD and EMI Implementation

The connectors do not have any ESD protection. We highly recommend using the adapter board with wires as short as possible.

A helpful guide is available from TI; just search for slva680 at ti.com.

9 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

10 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

11 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

12 Packaging

All F&S ESD-sensitive products will be shipped either in trays or in bags.

13 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

14 Appendix

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