Hardware Documentation

PicoCore™MX93
for HW Revision 1.00

Preliminary

Version 004
(2023-10-24)

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About This Document

This document describes how to use the PicoCore™MX93 board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Note:
Please use our schematic review service!

PicoCoreMX93 uses pre series NXP CPU and the module itself is under development.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
07.07.2023	001	1.00	A	-	Initial Version	HF
27.07.2023	002	1.00	M	3.1; 4.13; 4.8.2	Correct J2 Pin65; Correct RGMII Pins (ETH_x_LED)	MW
01.09.2023	002	1.00	A	4.10.3; 4.10.4	Pin mapping for RGB display interface added	HF
05.09.2023	003	1.00	M	0; 4.5; 4.6; 4.8.2; 4.9; 4.10.3; 4.10.4	Correct CPU Pin for: SPI_B; I2C_IRQ; UART; RGMII; Audio (I2S) Add Comment to UART_B about Wifi / BT Correct connector mapping for RGB display	MW
24.10.2023	004	1.00	M	3.1	Add mPCIE J1-77,79,83,85,89,91,95,97, not connected	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block diagram

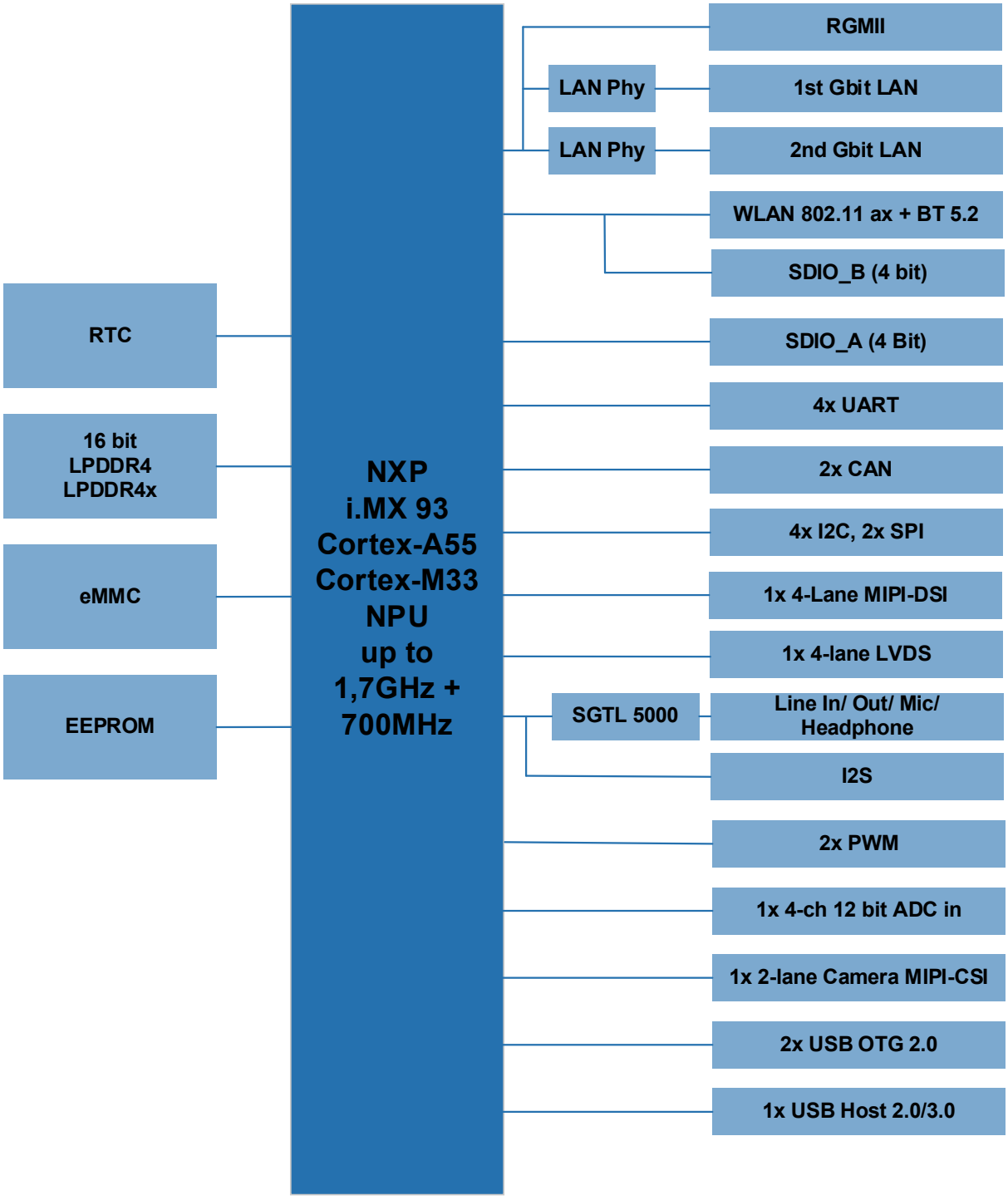

Figure 1: Block Diagram

2 Mechanical Dimension

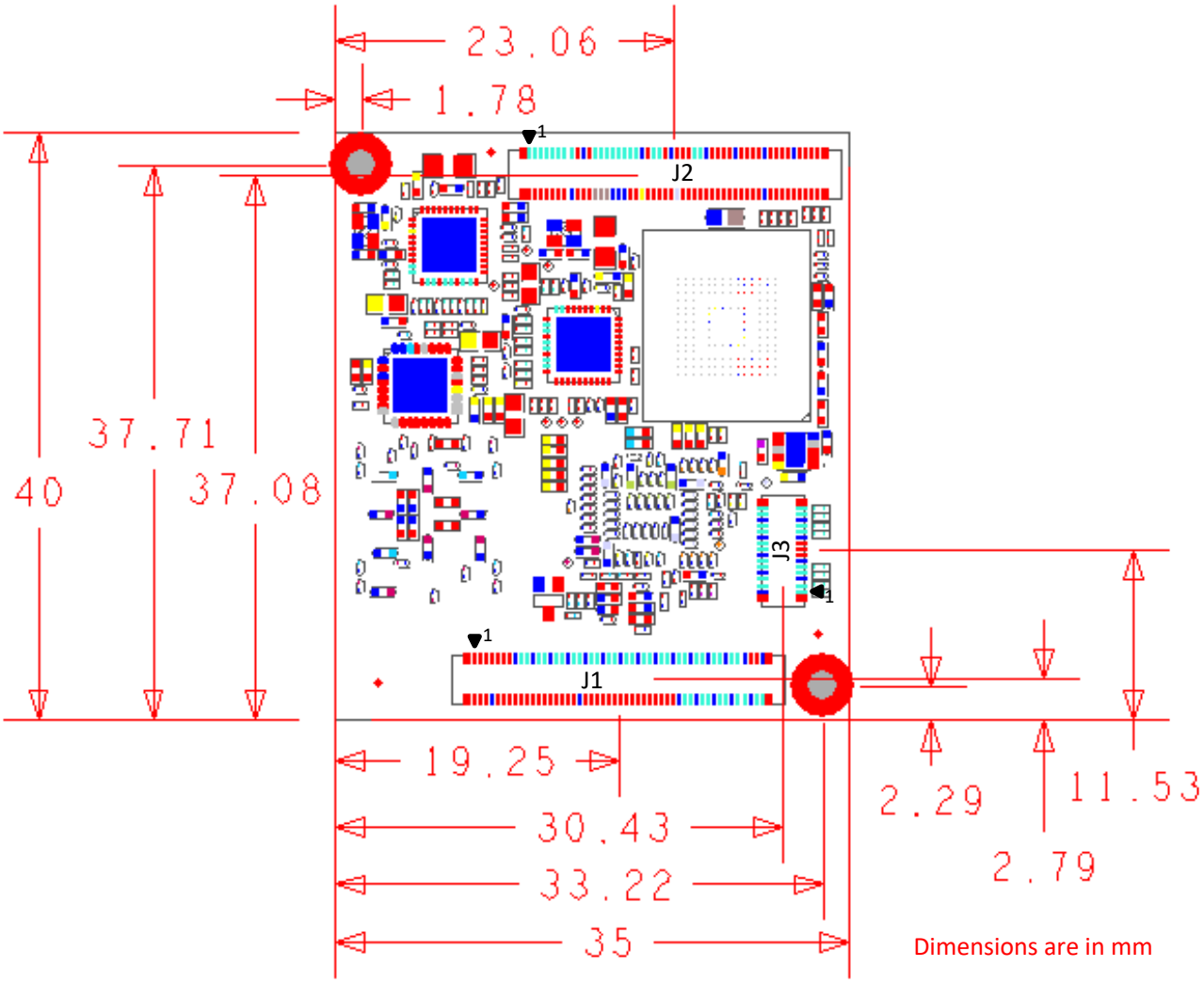

Figure 2: Mechanical Dimension from bottom side (dimensions in imm)

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.22.** This part is in F&S stock and can be ordered via F&S web shop.

The stack height of the space is 1.5mm. If a different stack height is needed, another spacer should be chosen.

Data sheet and 3D model (STP) is available on our website.

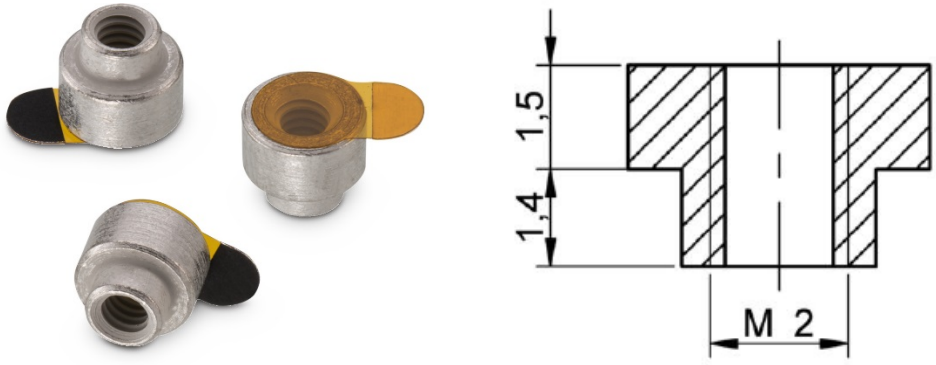

Figure 3: SMT Steel Spacer

2.2 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of heat spreader is **MHS.PC100.1** and can be ordered via F&S web shop.

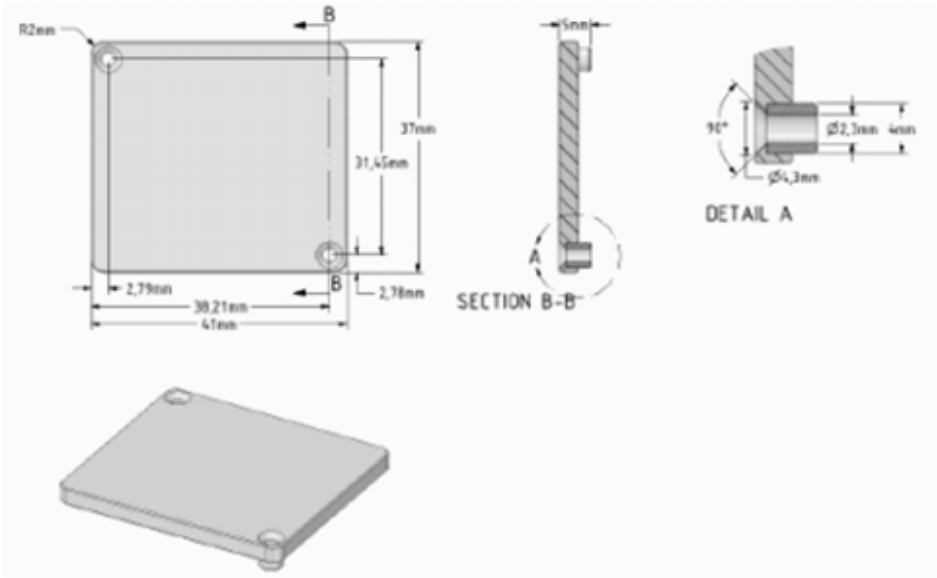

Figure 4: Heat Spreader (Images are not to scale)

3 Interface and signal description

3.1 B2B connectors

PicoCoreMX93 is using two 100 pin connectors (J1/J2) from manufacturer Hirose.

Part number J1/J2: DF40C-100DP-0.4V.

Part number for the counterpart *J1/J2*: DF40C-100DS-0.4V

With this combination you get minimal stacking height of 1,5mm. Other possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered in web shop.

Connector J1/J2 is compatible to J1/J2 of PicoCoreMX8MP (NXP i.MX8M Plus) and PicoCoreMX8MM (NXP i.MX8M Mini) and PicoCoreMX8MN (NXP i.MX8M Nano) and PicoCoreMX6UL100 (NXP i.MX6UL).

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1						
J1	1	I2C_B_IRQ	GPIO_IO18	I	3.3V	
J1	3	I2C_B_SCL	GPIO_IO13	I/O	3.3V	2k49 PU
J1	5	I2C_B_SDA	GPIO_IO12	I/O	3.3V	2k49 PU
J1	7	GPIO_J1_7	GPIO_IO24		3.3V	
J1	9	BL_ON	PCA9634PW: LED1	O	3.3V	Display Backlight Enable Via IO expander PCA9634PW
J1	11	BL_PWM	PCA9634PW: LED0	O		Display Backlight PWM Via IO expander PCA9634PW
J1	13	VLCD_ON	PCA9634PW: LED2	O	3.3V	Via IO expander PCA9634PW
J1	15	GND		PWR	GND	
J1	17	DISP_A_CLK_P	MIPI_DSI1_CLK_P	O	1.8V	4 Lane MIPI-DSI
J1	19	DISP_A_CLK_N	MIPI_DSI1_CLK_N	O	1.8V	4 Lane MIPI-DSI
J1	21	GND		PWR	GND	
J1	23	DISP_A_DATA0_P	MIPI_DSI1_D0_P	O	1.8V	4 Lane MIPI-DSI
J1	25	DISP_A_DATA0_N	MIPI_DSI1_D0_N	O	1.8V	
J1	27	GND		PWR	GND	4 Lane MIPI-DSI
J1	29	DISP_A_DATA1_P	MIPI_DSI1_D1_P	O	1.8V	
J1	31	DISP_A_DATA1_N	MIPI_DSI1_D1_N	O	1.8V	4 Lane MIPI-DSI
J1	33	GND		PWR	GND	
J1	35	DISP_A_DATA2_P	MIPI_DSI1_D2_P	I	1.8V	4 Lane MIPI-DSI
J1	37	DISP_A_DATA2_N	MIPI_DSI1_D2_N	I	1.8V	4 Lane MIPI-DSI
J1	39	GND		PWR	GND	
J1	41	DISP_A_DATA3_P	MIPI_DSI1_D3_P	I	1.8V	4 Lane MIPI-DSI
J1	43	DISP_A_DATA3_N	MIPI_DSI1_D3_N	I	1.8V	4 Lane MIPI-DSI
J1	45	GND		PWR	GND	

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J1	47	DISP_B_CLK_P	LVDS_CLK_P	O	1.8V	4 Lane LVDS
J1	49	DISP_B_CLK_N	LVDS_CLK_N	O	1.8V	4 Lane LVDS
J1	51	GND		PWR	GND	
J1	53	DISP_B_DATA0_P	LVDS_D0_P	O	1.8V	4 Lane LVDS
J1	55	DISP_B_DATA0_N	LVDS_D0_N	O	1.8V	4 Lane LVDS
J1	57	GND		PWR	GND	
J1	59	DISP_B_DATA1_P	LVDS_D1_P	O	1.8V	4 Lane LVDS
J1	61	DISP_B_DATA1_N	LVDS_D1_N	O	1.8V	4 Lane LVDS
J1	63	GND		PWR	GND	
J1	65	DISP_B_DATA2_P	LVDS_D2_P	O	1.8V	4 Lane LVDS
J1	67	DISP_B_DATA2_N	LVDS_D2_N	O	1.8V	4 Lane LVDS
J1	69	GND		PWR	GND	
J1	71	DISP_B_DATA3_P	LVDS_D3_P	O	1.8V	4 Lane LVDS
J1	73	DISP_B_DATA3_N	LVDS_D3_N	O	1.8V	4 Lane LVDS
J1	75	GND		PWR	GND	
J1	77	mPCIE_TX_P	N.C.			
J1	79	mPCIE_TX_N	N.C.			
J1	81	GND		PWR	GND	
J1	83	mPCIE_RX_P	N.C.			
J1	85	mPCIE_RX_N	N.C.			
J1	87	GND		PWR	GND	
J1	89	mPCIE_CLK_P	N.C.			
J1	91	mPCIE_CLK_N	N.C.			
J1	93	GND		PWR	GND	
J1	95	mPCIE_PERST#	N.C.			
J1	97	mPCIE_WAKE#	N.C.			
J1	99	GND		PWR	GND	
J1	2	GPIO_J1_2	GPIO_IO19	I/O	3.3V	
J1	4	I2C_A_SCL	I2C1_SCL	I/O	3.3V	I2C serial clock Always On power domain
J1	6	I2C_A_SDA	I2C1_SDA	I/O	3.3V	I2C serial data Always On power domain
J1	8	GND		PWR	GND	
J1	10	CAN_A_RX	PDM_BIT_STREAM0	I	3.3V	CAN data receive Always On power domain
J1	12	CAN_A_TX	PDM_CLK	O	3.3V	CAN data transmit Always On power domain
J1	14	UART_A_RTS	SAI1_TXD0	O	3.3V	Don't connect PU or PD resistor! Always On power domain
J1	16	UART_A_CTS	SAI1_TXC	I	3.3V	Don't connect PU or PD resistor! Always On power domain
J1	18	UART_A_RXD	UART2_RXD	I	3.3V	Don't connect PU or PD resistor!

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
						Always On power domain
J1	20	UART_A_TXD	UART2_TXD	O	3.3V	Don't connect PU or PD resistor! Always On power domain
J1	22	UART_B_RTS	GPIO_IO07	O	3.3V	ⓘ 4.6 Serial Interface (UART) Not available if WLAN/BT mounted
J1	24	UART_B_CTS	GPIO_IO06	I	3.3V	ⓘ 4.6 Serial Interface (UART) Not available if WLAN/BT mounted
J1	26	UART_B_RXD	GPIO_IO05	I	3.3V	100k PU ⓘ 4.6 Serial Interface (UART) Not available if WLAN/BT mounted
J1	28	UART_B_TXD	GPIO_IO04	O	3.3V	ⓘ 4.6 Serial Interface (UART) Not available if WLAN/BT mounted
J1	30	UART_C_RXD	UART1_RXD	I	3.3V	10k PU Always On power domain
J1	32	UART_C_TXD	UART1_TXD	O	3.3V	Don't connect PU or PD resistor! Always On power domain
J1	34	UART_D_RXD	GPIO_IO15	I	3.3V	100k PU
J1	36	UART_D_TXD	GPIO_IO14	O	3.3V	
J1	38	GND		PWR	GND	
J1	40	I2C_C_SCL	GPIO_IO23	I/O	3.3V	2k49 PU
J1	42	I2C_C_SDA	GPIO_IO22	I/O	3.3V	2k49 PU
J1	44	GPIO_J1_44	GPIO_IO25		3.3V	2nd Fctn: CAN_B_TX 3rd Fctn: WLAN_WAKE ⓘ 4.7 CAN Interface
J1	46	GPIO_J1_46	GPIO_IO27		3.3V	2nd Fctn: CAN_B_RX 3rd Fctn: BT_WAKE ⓘ 4.7 CAN Interface
J1	48	I2C_D_SCL	I2C2_SCL	I/O	3.3V	No 2nd Fctn! ⓘ 4.5 I2C Interface 2k49 PU Always On power domain
J1	50	I2C_D_SDA	I2C2_SDA	I/O	3.3V	No 2nd Fctn! ⓘ 4.5 I2C Interface 2k49 PU Always On power domain
J1	56	SPI_B_SS0	GPIO_IO08		3.3V	SPI slave select
J1	58	SPI_B_MISO	GPIO_IO10		3.3V	SPI master in slave out
J1	60	SPI_B_MOSI	GPIO_IO09		3.3V	SPI master out slave in

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J1	62	SPI_B_SCLK	GPIO_IO11		3.3V	SPI serial clock
J1	64	SPI_A_SS0	GPIO_IO00		3.3V	SPI slave select
J1	66	SPI_A_MISO	GPIO_IO02		3.3V	SPI master in slave out
J1	68	SPI_A_MOSI	GPIO_IO01		3.3V	SPI master out slave in
J1	70	SPI_A_SCLK	GPIO_IO03		3.3V	SPI serial clock
J1	72	GND		PWR	GND	
J1	74	CSI_CLK_P	MIPI_CSI1_CLK_P		1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	76	CSI_CLK_N	MIPI_CSI1_CLK_N		1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	78	GND		PWR	GND	
J1	80	CSI_DATA0_P	MIPI_CSI1_D0_P	I	1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	82	CSI_DATA0_N	MIPI_CSI1_D0_N	I	1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	84	GND		PWR	GND	
J1	86	CSI_DATA1_P	MIPI_CSI1_D1_P	I	1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	88	CSI_DATA1_N	MIPI_CSI1_D1_N	I	1.8V	ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	90	GND		PWR	GND	
J1	92	CSI_DATA2_P	N.C.			ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	94	CSI_DATA2_N	N.C.			ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	96	GND		PWR	GND	
J1	98	CSI_DATA3_P	N.C.			ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J1	100	CSI_DATA3_N	N.C.			ⓘ 4.11 Camera Serial Interface (MIPI-CSI)
J2						
J2	1	ETH_A_D1_P	RTL8211FDI: MDIP0	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	3	ETH_A_D1_N	RTL8211FDI: MDIN0	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	5	ETH_A_D2_P	RTL8211FDI: MDIP1	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	7	ETH_A_D2_N	RTL8211FDI: MDIN1	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J2	9	ETH_A_D3_P	RTL8211FDI: MDIP2	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	11	ETH_A_D3_N	RTL8211FDI: MDIN2	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	13	ETH_A_D4_P	RTL8211FDI: MDIP3	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	15	ETH_A_D4_N	RTL8211FDI: MDIN3	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	17	ETH_A_LED	RTL8211FDI: LED2			ⓘ 4.8 Ethernet Default: Gbit link LED 2nd Fctn: RGMII
J2	19	GND		PWR	GND	
J2	21	ETH_B_LED	RTL8211FDI: LED2			ⓘ 4.8 Ethernet Default: Gbit link LED 2nd Fctn: RGMII
J2	23	ETH_B_D1_P	RTL8211FDI: MDIP0	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	25	ETH_B_D1_N	RTL8211FDI: MDIN0	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	27	ETH_B_D2_P	RTL8211FDI: MDIP1	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	29	ETH_B_D2_N	RTL8211FDI: MDIN1	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	31	ETH_B_D3_P	RTL8211FDI: MDIP2	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	33	ETH_B_D3_N	RTL8211FDI: MDIN2	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	35	ETH_B_D4_P	RTL8211FDI: MDIP3	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	37	ETH_B_D4_N	RTL8211FDI: MDIN3	Analog		ⓘ 4.8 Ethernet 2nd Fctn: RGMII
J2	39	GND		PWR	GND	
J2	41	USB_HOST_VBUS	USB2_VBUS	I	3.3V	ⓘ 4.2 USB 2.0 Interface
J2	43	USB_HOST_D_P	USB2_D_P	I/O		ⓘ 4.2 USB 2.0 Interface
J2	45	USB_HOST_D_N	USB2_D_N	I/O		ⓘ 4.2 USB 2.0 Interface
J2	47	USB_HOST_PWR	GPIO_IO28	O	3.3V	ⓘ 4.2 USB 2.0 Interface USB Host Power Enable
J2	49	GND		PWR	GND	
J2	51	USB_OTG_VBUS	USB1_VBUS	I	3.3V	ⓘ 4.2 USB 2.0 Interface
J2	53	USB_OTG_PWR	GPIO_IO29	O	3.3V	ⓘ 4.2 USB 2.0 Interface USB Power Enable
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	ⓘ 4.2 USB 2.0 Interface
J2	57	USB_OTG_D_P	USB1_D_P	I/O		ⓘ 4.2 USB 2.0 Interface
J2	59	USB_OTG_D_N	USB1_D_N	I/O		ⓘ 4.2 USB 2.0 Interface
J2	61	GND		PWR	GND	
J2	63	PWM	PCA9634PW: LED3			Via IO expander PCA9634PW

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J2	65	GPIO_J2_65	N.C.			
J2	67	GPIO_J2_67	CLKIN1	I	1.8V	No GPIO! If not used, a 10k PD is recommended ⓘ 4.1 ADC Interface
J2	69	GPIO_J2_69	CLKIN2	I	1.8V	No GPIO! If not used, a 10k PD is recommended ⓘ 4.1 ADC Interface
J2	71	GND		PWR	GND	
J2	73	GPIO_J2_73	ADC_IN0	I	1.8V	No GPIO, only ADC! ⓘ 4.1 ADC Interface
J2	75	GPIO_J2_75	ADC_IN1	I	1.8V	No GPIO, only ADC! ⓘ 4.1 ADC Interface
J2	77	GPIO_J2_77	ADC_IN2	I	1.8V	No GPIO, only ADC! ⓘ 4.1 ADC Interface
J2	79	GPIO_J2_79	ADC_IN3	I	1.8V	No GPIO, only ADC! ⓘ 4.1 ADC Interface
J2	81	GND		PWR	GND	
J2	83	GPIO_J2_83	PCA9634PW: LED6			Via IO expander PCA9634PW
J2	85	GPIO_J2_85	PCA9634PW: LED7			Via IO expander PCA9634PW
J2	87	GPIO_J2_87	TAMPER0	I/O	1.8V	
J2	89	GPIO_J2_89	TAMPER1	I/O	1.8V	
J2	91	GND		PWR	GND	
J2	93	JTAG_TCK	DAP_TCLK_SWCLK			
J2	95	JTAG_TMS	DAP_TMS_SWDIO			
J2	97	JTAG_TDI	DAP_TDI			
J2	99	JTAG_TDO	DAP_TDO_TRACESW			
J2	2	AUDIO_A_VCC				ⓘ 4.9 Audio
J2	4	AUDIO_A_GND		PWR		ⓘ 4.9 Audio
J2	6	AU-DIO_A_LOUT_L	SGTL5000: LOUT	O		ⓘ 4.9 Audio 2nd Fctn: I2S_SCLK
J2	8	AU-DIO_A_LOUT_R	SGTL5000: ROUT	O		ⓘ 4.9 Audio 2nd Fctn: I2S_LRCLK
J2	10	AUDIO_A_MIC	SGTL5000: MICIN	I		ⓘ 4.9 Audio
J2	12	AUDIO_A_LIN_L	SGTL5000: LLINEIN	I		ⓘ 4.9 Audio 2nd Fctn: I2S_MCLK
J2	14	AUDIO_A_LIN_R	SGTL5000: RLINEIN	I		ⓘ 4.9 Audio
J2	16	GND		PWR	GND	
J2	18	AUDIO_A_HP_L	SGTL5000: LHPOUT	O		ⓘ 4.9 Audio 2nd Fctn: I2S_DOUT
J2	20	AUDIO_A_HP_R	SGTL5000: RHPOUT	O		ⓘ 4.9 Audio 2nd Fctn: I2S_DIN
J2	22	AU-DIO_A_HP_GND	SGTL5000: HP_VGND	PWR		ⓘ 4.9 Audio

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J2	24	VDD_VIN	VSYS		5.0V	ⓘ 4.15 Power and Power Control Pins
J2	26	VDD_VIN	VSYS		5.0V	ⓘ 4.15 Power and Power Control Pins
J2	28	VDD_VIN	VSYS		5.0V	ⓘ 4.15 Power and Power Control Pins
J2	30	GND		PWR	GND	
J2	32	GND		PWR	GND	
J2	34	GND		PWR	GND	
J2	36	VDD_BAT_IN		PWR	0.9V .. 5.5V	ⓘ 4.15 Power and Power Control Pins RTC battery backup sup-ply voltage
J2	38	RESERVED	N.C.			
J2	40	VDD_3V3	VIO	O	3.3V	20mA output from on module DCDC powered from VDD_VIN
J2	42	RESET_IN	PMIC_RST_B	I	1.8V	ⓘ 4.15 Power and Power Control Pins
J2	44	PMIC_STBY	PMIC_STBY_REQ			ⓘ 4.15 Power and Power Control Pins
J2	46	PMIC_ON_REQ	PMIC_ON_REQ			ⓘ 4.15 Power and Power Control Pins
J2	48	ON_OFF	ONOFF	I		ⓘ 4.15 Power and Power Control Pins Toggle state from ON to OFF 100k PU to 1.8V
J2	50	BOOTSEL		I		ⓘ 5 Boot Mode Service jumper, normally left open
J2	52	SD_A_VCC	PMIC: LDO5	O	1.8V/3 .3V	ⓘ 4.3 SD Card Interface SD_A Supply Voltage, 150mA max Output
J2	54	RESERVED				
J2	56	SD_A_RST	SD2_RESET_B	O	SD_A_ VCC	ⓘ 4.3 SD Card Interface
J2	58	SD_A_WP	N.C.			ⓘ 4.3 SD Card Interface No write protect pin available.
J2	60	SD_A_CD	SD2_CD_B	I	SD_A_ VCC	ⓘ 4.3 SD Card Interface SD card detect
J2	62	SD_A_CMD	SD2_CMD	O	SD_A_ VCC	ⓘ 4.3 SD Card Interface
J2	64	SD_A_CLK	SD2_CLK	O	SD_A_ VCC	ⓘ 4.3 SD Card Interface
J2	66	SD_A_DATA0	SD2_DATA0	I/O	SD_A_ VCC	ⓘ 4.3 SD Card Interface

	Pin	Default Function	Internal Pad	I/O	Vol-tage	Remarks
J2	68	SD_A_DATA1	SD2_DATA1	I/O	SD_A_VCC	ⓘ 4.3 SD Card Interface
J2	70	SD_A_DATA2	SD2_DATA2	I/O	SD_A_VCC	ⓘ 4.3 SD Card Interface
J2	72	SD_A_DATA3	SD2_DATA3	I/O	SD_A_VCC	ⓘ 4.3 SD Card Interface
J2	74	SD_A_DATA4	N.C.			Not available, only four data bits
J2	76	SD_A_DATA5	N.C.			Not available, only four data bits
J2	78	SD_A_DATA6	N.C.			Not available, only four data bits
J2	80	SD_A_DATA7	N.C.			Not available, only four data bits
J2	82	GND	GND	PWR	GND	
J2	84	SD_B_RST	N.C.			Not available
J2	86	SD_B_WP	N.C.			Not available
J2	88	SD_B_CD	N.C.			Not available
J2	90	SD_B_CMD	SD3_CMD	O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted
J2	92	SD_B_CLK	SD3_CLK	O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted
J2	94	SD_B_DATA0	SD3_DATA0	I/O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted
J2	96	SD_B_DATA1	SD3_DATA1	I/O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted
J2	98	SD_B_DATA2	SD3_DATA2	I/O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted
J2	100	SD_B_DATA3	SD3_DATA3	I/O	1.8V	ⓘ 4.3 SD Card Interface N.C. if WLAN/BT mounted

Table 2: B2B connector

4 Interfaces

4.1 ADC Interface

PicoCoreMX93 module has internal four channel 12 bit single-ended ADC controller.

	Pin	Function	I/O	Min	Max	Notes
J2	73	ADC_IN0	I	GND	1.8V	
J2	75	ADC_IN1	I	GND	1.8V	
J2	77	ADC_IN2	I	GND	1.8V	
J2	79	ADC_IN3	I	GND	1.8V	

These pins are not compatible with other PicoCores.

4.2 USB 2.0 Interface

PicoCoreMX93 module can support 2x USB 2.0 OTG. The USB OTG can also support USB-Type C connection.

The 90 Ohm differential pairs of USB signals need no termination.

For external ports ESD and EMV protection is required nearby the USB connectors.

If the USB OTG will be used in Host Mode, the **USB_OTG_ID** pin should be pulled down to GND with a resistor. Otherwise it must be directly connected to the USB connector.

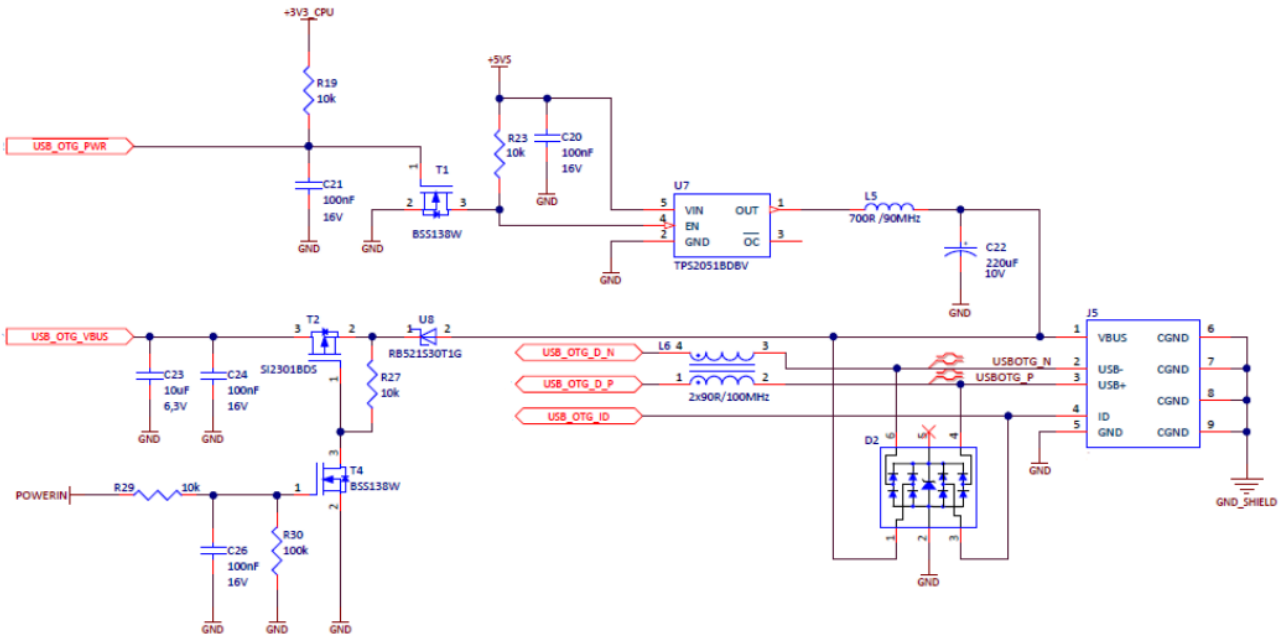

Figure 5: USB OTG example connection

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
USB Host 2.0						
J2	41	USB_HOST_VBUS	USB2_VBUS	I	5.0V	USB Host voltage detection. There is a resistance divider to scale 5V to 3.3V CPU input. N.C. for USB host function.
J2	43	USB_HOST_D_P	USB2_D_P	I/O	3.3V	90Ohm differential pair
J2	45	USB_HOST_D_N	USB2_D_N	I/O	3.3V	90Ohm differential pair
J2	47	USB_HOST_PWR	GPIO1_IO28	O	3.3V	**No pull-up/down on module**
USB OTG 2.0						
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	USB OTG Voltage detection. There is a resistance divider to scale 5V to 3.3V CPU input. N.C. for USB host function.
J2	53	USB_OTG_PWR	GPIO1_IO29	O	3.3V	**No pull-up/down on module**
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	Should be pulled down to GND for Host Mode, otherwise connect directly to the connector
J2	57	USB_OTG_D_P	USB1_D_P	I/O	3.3V	90Ohm differential pair
J2	59	USB_OTG_D_N	USB1_D_N	I/O	3.3V	90Ohm differential pair

Table 3: USB Host & OTG Interface

4.3 SD Card Interface

The PicoCoreMX93 module can support two SD Card Interfaces (SD_A and SD_B). For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The SD_A interface support 4 bit with card detect and reset. There is no dedicated write protect pin. SD_A_VCC is an adjustable voltage supply for SD_A Interface. It can be selected between 3.3V and 1.8V via software adjustment. The current output is limited to 150mA.

The SD_B interface is shared with the WLAN/BT module. This interface is only available, if WLAN/BT isn't mounted on module. SD_B has no dedicated pin for write protect, no reset and no card detect signal. SD_B_VCC is fixed to 1.8V.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
SDIO_A						
J2	52	SD_A_VCC		O	1.8V / 3.3V	Selectable; max 150mA output
J2	54	NC	NC	NC	SD_A_VCC	
J2	56	SD_A_RST	SD2_RESET_B	O	SD_A_VCC	active low; 100k pull-up on module
J2	58	SD_A_WP	NC	NC		No dedicated I/O available.
J2	60	SD_A_CD	SD2_CD_B	I	3.3V	
J2	62	SD_A_CMD	SD2_CMD	O	SD_A_VCC	100k pull-up on module
J2	64	SD_A_CLK	SD2_CLK	O	SD_A_VCC	
J2	66	SD_A_DATA0	SD2_DATA0	I/O	SD_A_VCC	100k pull-up on module
J2	68	SD_A_DATA1	SD2_DATA1	I/O	SD_A_VCC	
J2	70	SD_A_DATA2	SD2_DATA2	I/O	SD_A_VCC	
J2	72	SD_A_DATA3	SD2_DATA3	I/O	SD_A_VCC	
J2	74	SD_A_DATA4	NC	NC		
J2	76	SD_A_DATA5	NC	NC		
J2	78	SD_A_DATA6	NC	NC		
J2	80	SD_A_DATA7	NC	NC		
SDIO_B [optional without WLAN/BT]						
J2	84	SD_B_RST	NC	NC		
J2	86	SD_B_WP	NC	NC		
J2	88	SD_B_CD	NC	NC		
J2	90	SD_B_CMD	SD3_CMD	O	SD_B_VCC	100k pull-up on module
J2	92	SD_B_CLK	SD3_CLK	O	SD_B_VCC	
J2	94	SD_B_DATA0	SD3_DATA0	I/O	SD_B_VCC	100k pull-up on module
J2	96	SD_B_DATA1	SD3_DATA1	I/O	SD_B_VCC	
J2	98	SD_B_DATA2	SD3_DATA2	I/O	SD_B_VCC	
J2	100	SD_B_DATA3	SD3_DATA3	I/O	SD_B_VCC	

Table 4: SD Card Interface Pinout

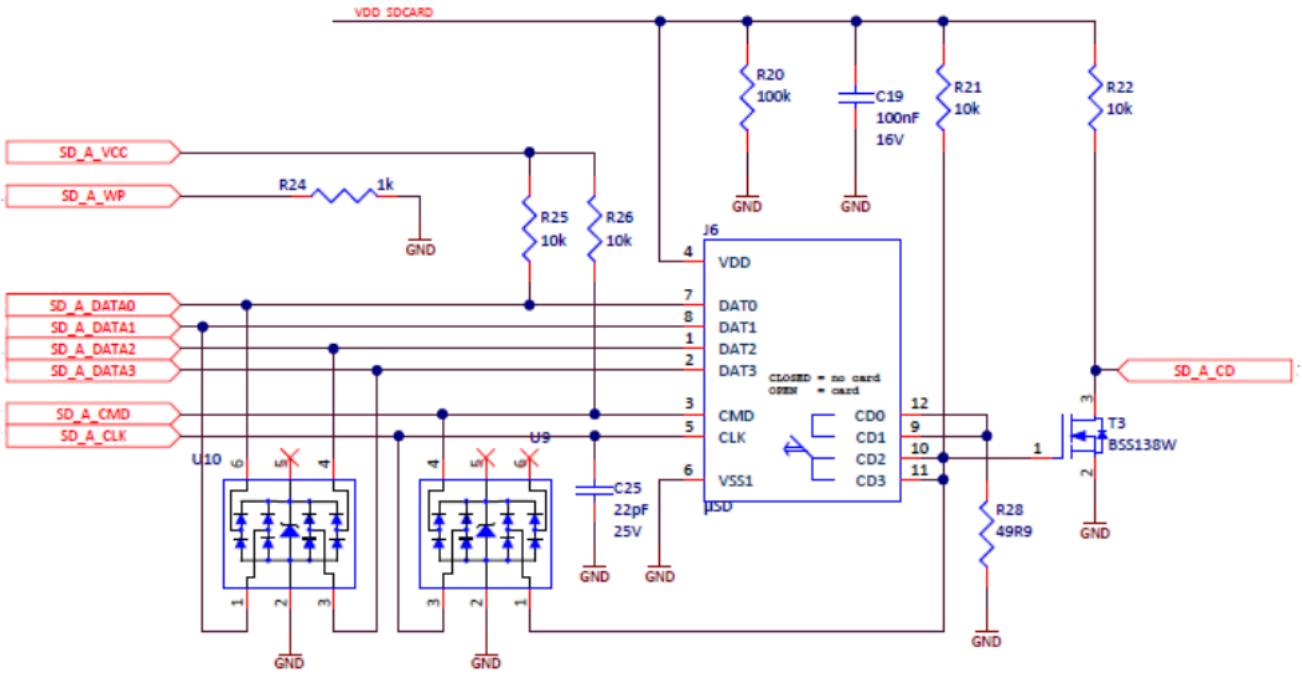

Figure 6: SD Card connector example connection

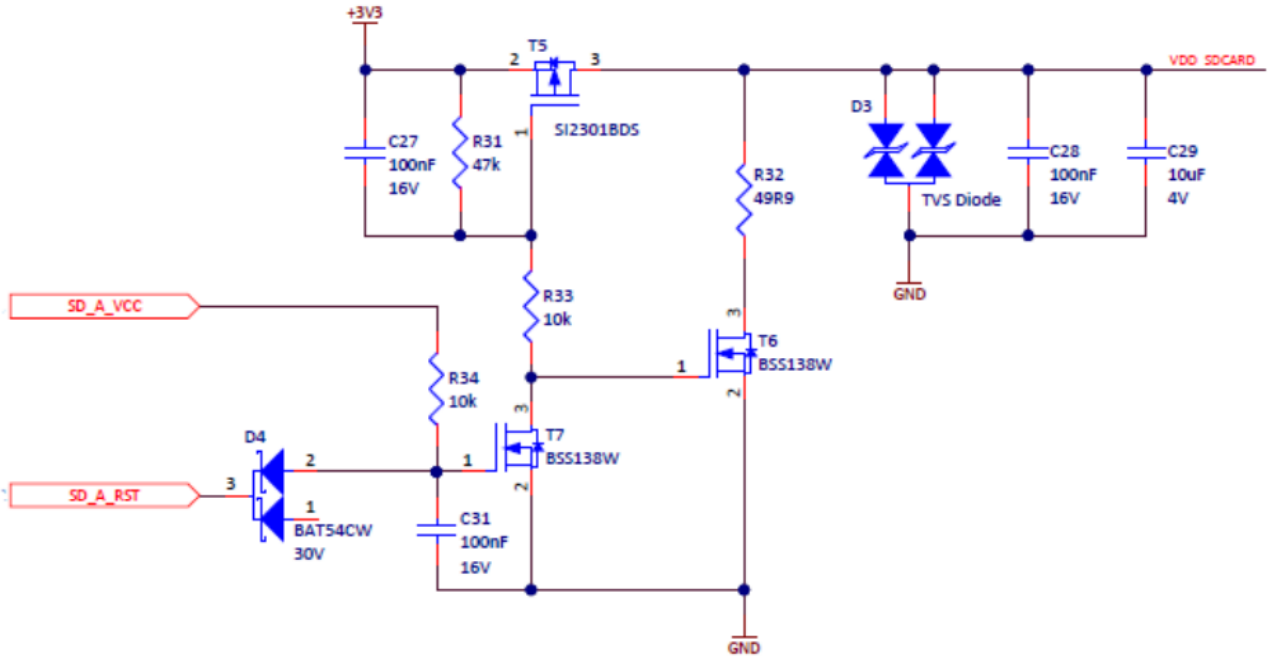

Figure 7: SD_A supply voltage switching circuit

4.4 Serial Peripheral Interface (SPI)

The module support two Hi-Speed SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage levels need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*	MM*	Voltage	Remarks
SPI_A							
J1	64	SPI_A_SS0	GPIO0_IO00	I	O	3.3V	
J1	66	SPI_A_MISO	GPIO0_IO02	O	I	3.3V	
J1	68	SPI_A_MOSI	GPIO0_IO01	I	O	3.3V	
J1	70	SPI_A_SCLK	GPIO0_IO03	I	O	3.3V	
SPI_B							
J1	56	SPI_B_SS0	GPIO0_IO08	I	O	3.3V	
J1	58	SPI_B_MISO	GPIO0_IO10	O	I	3.3V	
J1	60	SPI_B_MOSI	GPIO0_IO09	I	O	3.3V	
J1	62	SPI_B_SCLK	GPIO0_IO11	I	O	3.3V	

**SM: PicoCoreMX93 used in Slave Mode, MM: PicoCoreMX93 used in Master Mode*

Table 5: Serial Peripheral Interface (SPI) Pinout

4.5 I2C Interface

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter.

For more chip selects, interrupts and other signals GPIOs can be used and the driver can be modified.

Note:
I2C_D is used to control several peripherals on module (i.e. RTC, EEPROM, Audio Codec, PMIC, GPIO expander…). Therefore it's not possible to use this contacts as GPIO or any other function. For I2C_D, PicoCore™ is always the bus master. Please use I2C_A/B/C before using I2C_D.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
I2C_A						
J1	4	I2C_A_SCL	I2C1_SCL	O	3.3V	2.49k pull-up on module
J1	6	I2C_A_SDA	I2C1_SDA	I/O	3.3V	2.49k pull-up on module
I2C_B						
J1	1	I2C_B_IRQ	GPIO0_IO18	I	3.3V	
J1	3	I2C_B_SCL	GPIO0_IO13	O	3.3V	2.49k pull-up on module
J1	5	I2C_B_SDA	GPIO0_IO12	I/O	3.3V	2.49k pull-up on module
I2C_C						
J1	40	I2C_C_SCL	GPIO0_IO23	O	3.3V	2.49k pull-up on module
J1	42	I2C_C_SDA	GPIO0_IO22	I/O	3.3V	2.49k pull-up on module
I2C_D						
J1	48	I2C_D_SCL	I2C2_SCL	O	3.3V	2.49k pull-up on module
J1	50	I2C_D_SDA	I2C2_SDA	I/O	3.3V	2.49k pull-up on module

Table 6: I2C Interface Pinout

I2C	Address	Device	Function
I2C_A	0x50	N24S64B	EEPROM
I2C_D	0x51	PCF85263ATL	Low Power RTC
I2C_D	0x60	PCA9634PW	GPIO expander
I2C_D	0x0A	SGTL5000	Audio Codec
I2C_D	0x25	PCA9451A	PMIC

Table 7: On Module I2C Devices

4.6 Serial Interface (UART)

	Pin	Default Function	CPU Pad	I/O	Voltage	Remarks
UART_A						
J1	14	UART_A_RTS	SAI1_TXD0	NC		
J1	16	UART_A_CTS	SAI1_TXC	NC		
J1	18	UART_A_RXD	UART2_RXD	I	3.3V	100k pull-up on module
J1	20	UART_A_TXD	UART2_TXD	O	3.3V	
UART_B [optional without BT]						
J1	22	UART_B_RTS	GPIO_IO07	O	3.3V	
J1	24	UART_B_CTS	GPIO_IO06	I	3.3V	
J1	26	UART_B_RXD	GPIO_IO05	I	3.3V	100k pull-up on module
J1	28	UART_B_TXD	GPIO_IO04	O	3.3V	
UART_C						
J1	30	UART_C_RXD	UART1_RXD	I	3.3V	100k pull-up on module
J1	32	UART_C_TXD	UART1_TXD	O	3.3V	
UART_D						
J1	34	UART_D_RXD	GPIO_IO15	I	3.3V	100k pull-up on module
J1	36	UART_D_TXD	GPIO_IO14	O	3.3V	

Table 8: UART Interface Pin Out

We recommend to use UART_A for debugging and service only.

UART_B is shared with Wifi/BT Module. If BT is used UART_B is not connected.

F&S standard software uses DCE mode for UART.

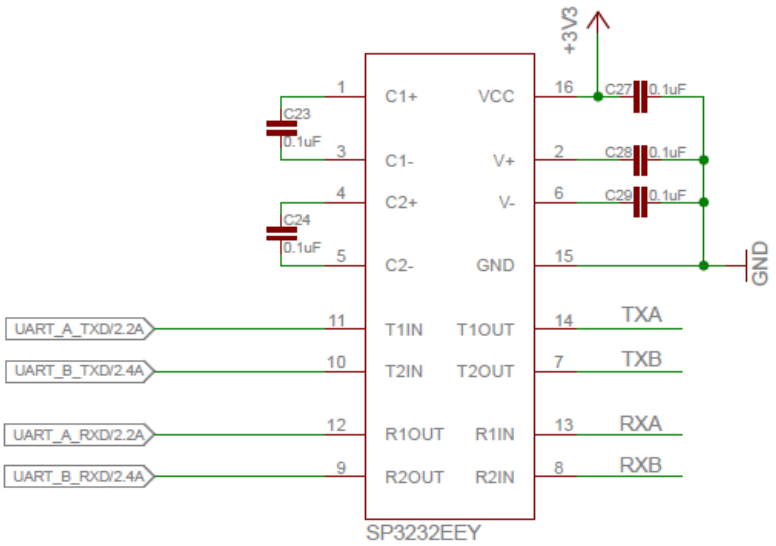

Figure 8: UART transceiver example

4.7 CAN Interface

PicoCoreMX93 module can support up to 2 CAN buses, which are shared with other interfaces or signals. With the CAN bus usage, the other interfaces cannot be used.

There are no on-module pull-up or pull-downs for the CAN signals.

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
CAN_A						
J1	10	CAN_A_RX	PDM_BIT_STREAM0	I	3.3V	
J1	12	CAN_A_TX	PDM_CLK	O	3.3V	
CAN_B						
J1	44	CAN_B_TX	GPIO_IO25	O	3.3V	Not compatible with other Pico-Cores!
J1	46	CAN_B_RX	GPIO_IO27	I	3.3V	Not compatible with other Pico-Cores!

Table 9: CAN Interface Pinout

4.8 Ethernet

4.8.1 Ethernet Interface with Gbit PHY

The module supports up to two 10/100/1000 Mbit LAN interfaces via RealTek RT8211 Ethernet PHYs. There is a mounting option to route one RGMII to the pins of ETH_A and ETH_B.

	Pin	Pin Name	RT8211 Pad	I/O	Voltage	Remarks
Ethernet A (PHY_1: RT8211)						
J2	1	ETH_A_D1_P	MDIP0	I/O	1.2V	
J2	3	ETH_A_D1_N	MDIN0	I/O	1.2V	
J2	5	ETH_A_D2_P	MDIP1	I/O	1.2V	
J2	7	ETH_A_D2_N	MDIN1	I/O	1.2V	
J2	9	ETH_A_D3_P	MDIP2	I/O	1.2V	
J2	11	ETH_A_D3_N	MDIN2	I/O	1.2V	
J2	13	ETH_A_D4_P	MDIP3	I/O	1.2V	
J2	15	ETH_A_D4_N	MDIN3	I/O	1.2V	
J2	17	ETH_A_LED	LED1	O	2.5V	Activity LED (RX/TX) Option:LED2
Ethernet B (PHY_2: RT8211) [optional]						
J2	21	ETH_B_LED	LED1	O	2.5V	Activity LED (RX/TX) Option: LED2
J2	23	ETH_B_D1_P	MDIP0	I/O	1.2V	
J2	25	ETH_B_D1_N	MDIN0	I/O	1.2V	
J2	27	ETH_B_D2_P	MDIP1	I/O	1.2V	
J2	29	ETH_B_D2_N	MDIN1	I/O	1.2V	
J2	31	ETH_B_D3_P	MDIP2	I/O	1.2V	
J2	33	ETH_B_D3_N	MDIN2	I/O	1.2V	
J2	35	ETH_B_D4_P	MDIP3	I/O	1.2V	
J2	37	ETH_B_D4_N	MDIN3	I/O	1.2V	

Table 10: Ethernet A & B Signals

4.8.2 Ethernet RGMII Interface

Without Ethernet PHYs: The module supports one 10/100/1000Mbit LAN interface via RGMII signals. The RGMII signals can be reached from the B2B Connector.

An external Ethernet-PHY or an external Ethernet switch is required on baseboard/carrier board.

Over the ETH_A_LED, ETH_B_LED, ETH_B_D4P and ETH_B_D4N there are 4 GPIOs that can be either used for the external switch or PHY (i.e. Reset, Interrupt, Enable etc.). ETH_A_LED and ETH_B_D4_P are connected to IO expander.

	Pin	Pin Name	Internal Pad	I/O	Voltage	Remarks
RGMII Interface [optional]						
J2	1	ETH_A_D1_P	ENET1 _MDC	O	1.8V	
J2	3	ETH_A_D1_N	ENET1_MDIO	I/O	1.8V	
J2	5	ETH_A_D2_P	ENET1_TX_CTL	O	1.8V	
J2	7	ETH_A_D2_N	ENET1_TXC	O	1.8V	
J2	9	ETH_A_D3_P	ENET1_TD0	O	1.8V	
J2	11	ETH_A_D3_N	ENET1_TD1	O	1.8V	
J2	13	ETH_A_D4_P	ENET1_ TD2	O	1.8V	
J2	15	ETH_A_D4_N	ENET1_ TD3	O	1.8V	
J2	17	ETH_A_LED	SAI1_TXFS	O	3.3V	Standard GPIO
J2	21	ETH_B_LED	PCA9634PW: LED5	I/O	3.3V	
J2	23	ETH_B_D1_P	ENET1_RX_CTL	I	1.8V	
J2	25	ETH_B_D1_N	ENET1_RXC	I	1.8V	
J2	27	ETH_B_D2_P	ENET1_RD0	I	1.8V	
J2	29	ETH_B_D2_N	ENET1_RD1	I	1.8V	
J2	31	ETH_B_D3_P	ENET1_ RD2	I	1.8V	
J2	33	ETH_B_D3_N	ENET1_ RD3	I	1.8V	
J2	35	ETH_B_D4_P	PCA9634PW: LED4	O	3.3V	
J2	37	ETH_B_D4_N	PDM_BIT_STREAM1	O	3.3V	Standard GPIO

Table 11: RGMII Interface Signals

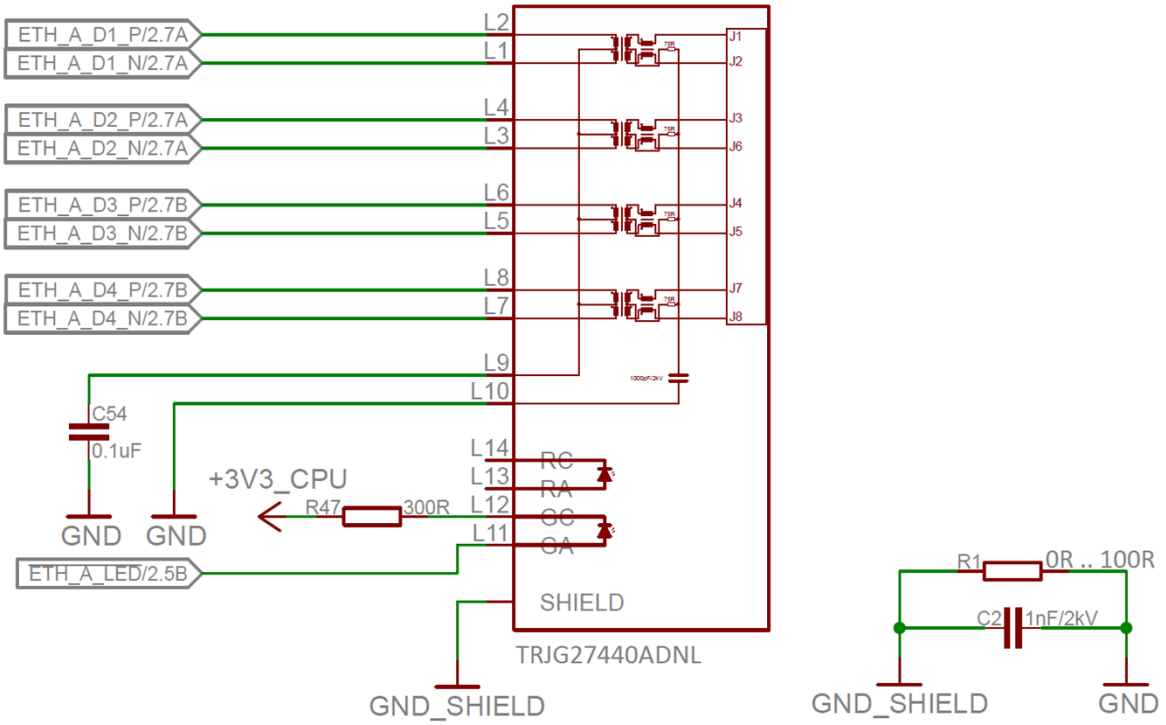

Figure 9: LAN output example

4.9 Audio

The PicoCoreMX93 module can support audio interface either directly via I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied from the PMIC on PicoCore Module as default. For a better and smoother audio quality an external low-noise power supply (e.g. LDO) is highly recommended (3V~3.3V – 5mA). In this case, the intern voltage source must be separated from the audio circuitry. Please contact us to have the correct jumper configuration for the external-supplied AUDIO_A_VCC.

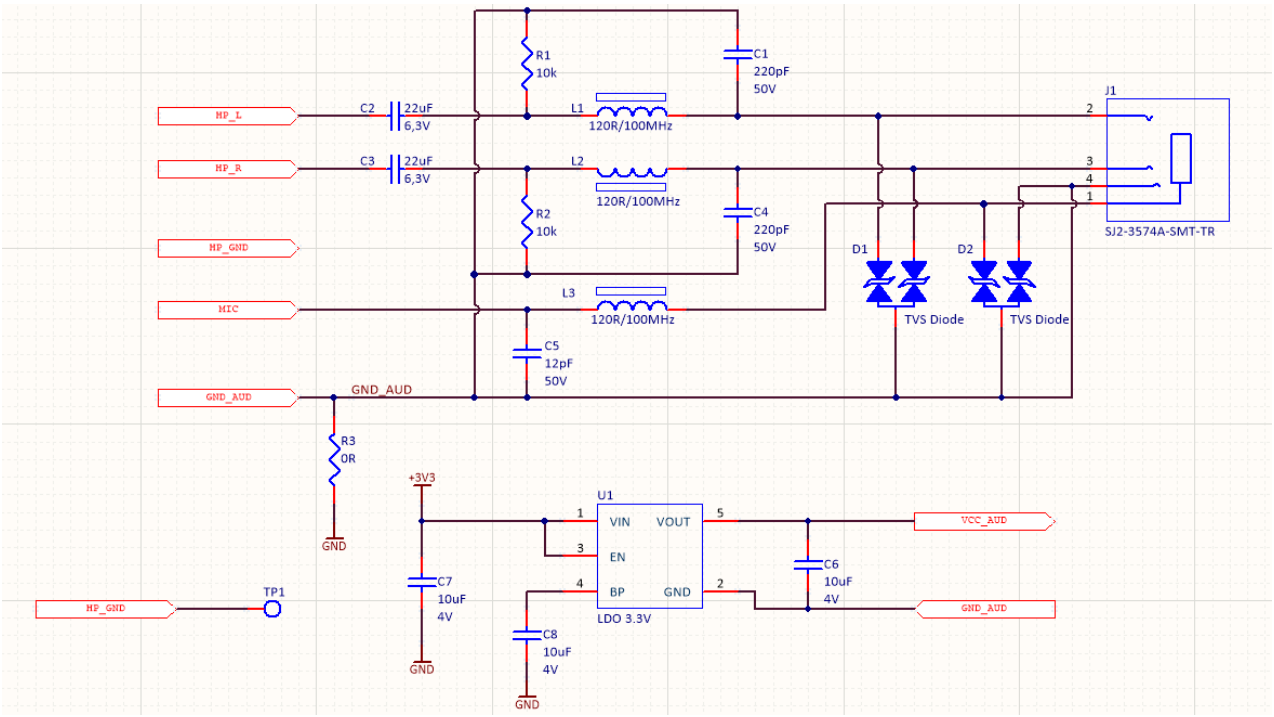

Figure 10: Headphone-Out Mic-In Example Circuit

	Pin	Signal	CPU Pad	I/O	Voltage*	Remarks
Audio A – with Audio Codec (SGTL5000) [optional]						
J2	2	AUDIO_A_VCC	VDDA	PWR	3V/3.3V	max 16.50mW power consumption
J2	4	AUDIO_A_GND	AGND	PWR	GND	
J2	6	AUDIO_A_LOUT_L	LOUT	O	3V/3.3V	
J2	8	AUDIO_A_LOUT_R	ROUT	O	3V/3.3V	
J2	10	AUDIO_A_MIC	MICIN	I	3V/3.3V	
J2	12	AUDIO_A_LIN_L	LLINEIN	I	3V/3.3V	
J2	14	AUDIO_A_LIN_R	RLINEIN	I	3V/3.3V	
J2	18	AUDIO_A_HP_L	LHPOUT	O	3V/3.3V	
J2	20	AUDIO_A_HP_R	RHPOUT	O	3V/3.3V	
J2	22	AUDIO_A_HP_GND	HP_VGND	O	GND	
Audio A – I2S Option (without Audio Codec) [standard]						
J2	2	AUDIO_A_VCC	N.C.	-	-	Do Not Connect! Leave open
J2	4	AUDIO_A_GND	N.C.	-	-	Do Not Connect! Leave open
J2	6	AUDIO_A_LOUT_L	GPIO_16	I/O	3.3V	I2S_A_SCLK
J2	8	AUDIO_A_LOUT_R	GPIO_26	I/O	3.3V	I2S_A_LRCLK
J2	10	AUDIO_A_MIC	N.C.	-	-	Do Not Connect! Leave open
J2	12	AUDIO_A_LIN_L	GPIO_17	O	3.3V	I2S_A_MCLK
J2	14	AUDIO_A_LIN_R	N.C.	-	-	Do Not Connect! Leave open
J2	18	AUDIO_A_HP_L	GPIO_21	I	3.3V	I2S_A_DOUT
J2	20	AUDIO_A_HP_R	GPIO_20	O	3.3V	I2S_A_DIN
J2	22	AUDIO_A_HP_GND	N.C.	-	-	Do Not Connect! Leave open

**Depends on the AUDIO_A_VCC source*

Table 12: Audio A Interface

4.10 Display Interface

The PicoCoreMX93 module support MIPI DSI interface or LVDS interface or RGB interface. Following maximum resolution:

MIPI-DSI: up top 1920x1200p60

LVDS: up to 1366x768p60 or 1280x800p60

On the module there are 2 display channels:

Configuration	Channel A	Channel B
DSI + LVDS	4-lane MIPI-DSI	4-lane LVDS

Table 13: Display Combinations

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1	9	BL_ON	PCA9634PW: LED1	O	3.3V	Display Backlight Enable Via IO expander PCA9634PW
J1	11	BL_PWM	PCA9634PW: LED0	O		Display Backlight PWM Via IO expander PCA9634PW
J1	13	VLCD_ON	PCA9634PW: LED2	O	3.3V	Via IO expander PCA9634PW

Table 14: Display Control Signals

It is also possible to connect RGB TTL display to the PicoCoreMX93. Pease see chapter 4.10.3 and 4.10.4 for connection.

4.10.1 Display Channel A (MIPI-DSI)

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
Channel A – MIPI-DSI Configuration						
J1	17	DISP_A_CLK_P	MIPI_DSI1_CLK_P	O	1.8V	
J1	19	DISP_A_CLK_N	MIPI_DSI1_CLK_N	O	1.8V	
J1	23	DISP_A_DATA0_P	MIPI_DSI1_D0_P	O	1.8V	
J1	25	DISP_A_DATA0_N	MIPI_DSI1_D0_N	O	1.8V	
J1	29	DISP_A_DATA1_P	MIPI_DSI1_D1_P	O	1.8V	
J1	31	DISP_A_DATA1_N	MIPI_DSI1_D1_ N	O	1.8V	
J1	35	DISP_A_DATA2_P	MIPI_DSI1_D2_ P	O	1.8V	
J1	37	DISP_A_DATA2_N	MIPI_DSI1_D2_ N	O	1.8V	
J1	41	DISP_A_DATA3_P	MIPI_DSI1_D3_ P	O	1.8V	
J1	43	DISP_A_DATA3_N	MIPI_DSI1_D3_ N	O	1.8V	

Table 15: MIPI DSI Interface

4.10.2 Display Channel B (LVDS)

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
Channel B – LVDS Configuration						
J1	47	DISP_B_CLK_P	LVDS_CLK_P	O	1.8V	
J1	49	DISP_B_CLK_N	LVDS_CLK_N	O	1.8V	
J1	53	DISP_B_DATA0_P	LVDS_D0_P	O	1.8V	
J1	55	DISP_B_DATA0_N	LVDS_D0_N	O	1.8V	
J1	59	DISP_B_DATA1_P	LVDS_D1_P	O	1.8V	
J1	61	DISP_B_DATA1_N	LVDS_D1_N	O	1.8V	
J1	65	DISP_B_DATA2_P	LVDS_D2_P	O	1.8V	
J1	67	DISP_B_DATA2_N	LVDS_D2_N	O	1.8V	
J1	71	DISP_B_DATA3_P	LVDS_D3_P	O	1.8V	
J1	73	DISP_B_DATA3_N	LVDS_D3_N	O	1.8V	

Table 16: LVDS Interface

4.10.3 18 bit RGB Display Interface

	Pin	RGB Function	CPU Pad	I/O	Voltage	Remarks
J1	64	lcdif.PCLK	GPIO_IO00	O		
J1	68	lcdif.DE	GPIO_IO01	O		
J1	66	lcdif.VSYNC	GPIO_IO02	O		
J1	70	lcdif.HSYNC	GPIO_IO03	O		
J1	28	lcdif.D[0]	GPIO_IO04	O		On Board Wifi must be removed
J1	26	lcdif.D[1]	GPIO_IO05	O		On Board Wifi must be removed
J1	24	lcdif.D[2]	GPIO_IO06	O		On Board Wifi must be removed
J1	22	lcdif.D[3]	GPIO_IO07	O		On Board Wifi must be removed
J1	56	lcdif.D[4]	GPIO_IO08	O		
J1	60	lcdif.D[5]	GPIO_IO09	O		
J1	58	lcdif.D[6]	GPIO_IO10	O		
J1	62	lcdif.D[7]	GPIO_IO11	O		
J1	5	lcdif.D[8]	GPIO_IO12	O		Pull-Up on Board must be removed
J1	3	lcdif.D[9]	GPIO_IO13	O		Pull-Up on Board must be removed
J1	36	lcdif.D[10]	GPIO_IO14	O		
J1	34	lcdif.D[11]	GPIO_IO15	O		Pull-Up on Board must be removed
J2	6	lcdif.D[12]	GPIO_IO16	O		On Board Audio must be removed
J2	12	lcdif.D[13]	GPIO_IO17	O		On Board Audio must be removed
J1	1	lcdif.D[14]	GPIO_IO18	O		
J1	2	lcdif.D[15]	GPIO_IO19	O		
J2	20	lcdif.D[16]	GPIO_IO20	O		On Board Audio must be removed
J2	18	lcdif.D[17]	GPIO_IO21	O		On Board Audio must be removed

Table 17: 18 bit RGB Interface

4.10.4 24 bit RGB Display Interface

	Pin	RGB Function	CPU Pad	I/O	Voltage	Remarks
J1	64	lcdif.PCLK	GPIO_IO00	O		
J1	68	lcdif.DE	GPIO_IO01	O		
J1	66	lcdif.VSYNC	GPIO_IO02	O		
J1	70	lcdif.HSYNC	GPIO_IO03	O		
J1	28	lcdif.D[0]	GPIO_IO04	O		On Board Wifi must be removed
J1	26	lcdif.D[1]	GPIO_IO05	O		On Board Wifi must be removed
J1	24	lcdif.D[2]	GPIO_IO06	O		On Board Wifi must be removed
J1	22	lcdif.D[3]	GPIO_IO07	O		On Board Wifi must be removed
J1	56	lcdif.D[4]	GPIO_IO08	O		
J1	60	lcdif.D[5]	GPIO_IO09	O		
J1	58	lcdif.D[6]	GPIO_IO10	O		
J1	62	lcdif.D[7]	GPIO_IO11	O		
J1	5	lcdif.D[8]	GPIO_IO12	O		Pull-Up on Board must be removed
J1	3	lcdif.D[9]	GPIO_IO13	O		Pull-Up on Board must be removed
J1	36	lcdif.D[10]	GPIO_IO14	O		
J1	34	lcdif.D[11]	GPIO_IO15	O		Pull-Up on Board must be removed
J2	6	lcdif.D[12]	GPIO_IO16	O		On Board Audio must be removed
J2	12	lcdif.D[13]	GPIO_IO17	O		On Board Audio must be removed
J1	1	lcdif.D[14]	GPIO_IO18	O		
J1	2	lcdif.D[15]	GPIO_IO19	O		
J2	20	lcdif.D[16]	GPIO_IO20	O		On Board Audio must be removed
J2	18	lcdif.D[17]	GPIO_IO21	O		On Board Audio must be removed
J1	42	lcdif.D[18]	GPIO_IO22	O		Pull-Up on Board must be removed
J1	40	lcdif.D[19]	GPIO_IO23	O		Pull-Up on Board must be removed
J1	7	lcdif.D[20]	GPIO_IO24	O		
J1	44	lcdif.D[21]	GPIO_IO25	O		On Board Wifi must be removed
J2	8	lcdif.D[22]	GPIO_IO26	O		On Board Audio must be removed
J1	46	lcdif.D[23]	GPIO_IO27	O		On Board Wifi must be removed

Table 18: 24 bit RGB Interface

4.11 Camera Serial Interface (MIPI-CSI)

The module supports up to one dual-lane MIPI-CSI interface.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
MIPI-CSI Channel A						
J1	74	CSI_CLK_P	MIPI_CSI1_CLK_P	I	1.8V	
J1	76	CSI_CLK_N	MIPI_CSI1_CLK_N	I	1.8V	
J1	80	CSI_DATA0_P	MIPI_CSI1_D0_P	I	1.8V	
J1	82	CSI_DATA0_N	MIPI_CSI1_D0_N	I	1.8V	
J1	86	CSI_DATA1_ P	MIPI_CSI1_D1_P	I	1.8V	
J1	88	CSI_DATA1_ N	MIPI_CSI1_D1_N	I	1.8V	
J1	80	CSI_DATA2_P				Only two lanes. Not connected.
J1	82	CSI_DATA2_N				Only two lanes. Not connected.
J1	86	CSI_DATA3_ P				Only two lanes. Not connected.
J1	88	CSI_DATA3_ N				Only two lanes. Not connected.

Table 19: MIPI CSI Interface

4.12 WLAN and Bluetooth Interface

The PicoCore™MX93 contains a certified high performance WI-FI 6 and Bluetooth 5.2 module.

The module is based on NXP IW611 chip, having Europe (RED), US (FCC), Canada (ISED), Japan (Giteki) certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ax/ac/a/b/g/n
- Bluetooth 5.2 BR/EDR and LE long range (supports low Energy)

Note: In case WLAN/BT module is mounted only one external SD card interface (SD_A) is available and SD_B is not available.

4.13 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-up's or pull-down's are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

	Pin	Standard	CPU Pad	Voltage	Remarks
J1	2	GPIO_J1_2	GPIO_IO19	3.3V	
J1	7	GPIO_J1_7	GPIO_IO24	3.3V	
J1	44	GPIO_J1_44	GPIO_IO25	3.3V	2nd Fctn: CAN_B_TX
J1	46	GPIO_J1_46	GPIO_IO27	3.3V	2nd Fctn: CAN_B_RX
J1	52	GPIO_J1_52	N.C.		
J1	54	GPIO_J1_54	N.C.		
J2	63	PWM	PCA9634PW: LED3	3.3V	PWM Output (PWM3), LED3 of PCA9634PW
J2	65	GPIO_J2_65	N.C.		
J2	83	GPIO_J2_83	PCA9634PW: LED6	3.3V	GPIO or PWM Output, LED6 of PCA9634PW
J2	85	GPIO_J2_85	PCA9634PW: LED7	3.3V	GPIO or PWM Output, LED7 of PCA9634PW

Table 20: GPIO Interface

For the alternative usages of all Pins please refer to GPIO Reference Card.

4.14 JTAG

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	93	JTAG_TCK	JTAG_TCK*1	I	1.8V	Test Clock
J2	95	JTAG_TMS	JTAG_TMS*1	I	1.8V	Test Mode Select
J2	97	JTAG_TDI	JTAG_TDI*1	I	1.8V	Test Data In
J2	99	JTAG_TDO	JTAG_TDO*1	O	1.8V	Test Data Out

Table 21: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.15 Power and Power Control Pins

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main Power supply input please refer chapter 8 Electrical characteristic
J2	30 32 34	GND[*5]	I	Main Power supply Ground input
J2	36	VDD_VBAT[*1]	I	RTC battery input; tie to 3.0V please refer chapter 8 Electrical characteristic
J2	40	VDD_3V3[*2]	O	20mA output from on module DCDC powered from VDD_VIN
J2	52	SD_A_VCC	I	SDHC power output; 3.3V or 1.8V; max 150mA
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_HOST_VBUS	I	USB Phy voltage input; 5V
J2	42	RESETIN[*3]	I	Power on reset input; 100k Pull-Up to 1.8V
J2	44	PMIC_STBY[*4]	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button. A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
J2	2	AUDIO_A_VCC	I	External supply for audio codec; 3~3.3V – 5mA

Table 22: Power and Power Control

[*1] By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

[*2] VDD_3V3 is the 3.3V @20mA power supply of the module generated from PMIC and powered from VDD_VIN. Can be used as an "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 pin as a power supply for carrier board.

[*3] RESETINN is a Reset Input for the module. Will just reset the CPU. Button or an Open Collector/Open Drain output will restart the CPU. On power fail VDD_VIN has to be switched off and on to avoid latch up effects.

[*4] PMIC_STBY is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

[*5] The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

5 Boot Mode

The CPU of PicoCore has fuses to configure the default boot device. By default it is eMMC.

With pin 50 of J2 “BOOTSEL” it is possible to switch between “boot from internal fuses” and “boot from USB serial download”.

So you have the following two boot options:

Boot Device Select	BOOTSEL pin of PicoCore
Boot from internal fuses	Leave open
USB Serial Download	Connect to GND

Table 23: Boot Modes of PicoCore

6 Flash

6.1 eMMC Flash

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

The PicoCoreMX93 module can support up to 32GB eMMC flash memory.

7 Real Time Clock (RTC)

There is a NXP PCF85263ATL or a compatible RTC component implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD+0.3	V
Input Voltage range 1.8V IO pins	-0.3	2.15	V
Voltage on any IO with VIN off		0.3	V
USB_*_VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 24: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
+5VS	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_*_VBUS	USB supply voltage		4.5	5.5	
OVDD	On module 3.3V DCDC		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

Table 25: DC Electrical Characteristics

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Description	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top **(Ψ_{JT})**		0.98		°C/W

Table 26: Thermal Specs

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. Cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

10 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMC Implementing

Like all other COM modules on the market there is no ESD protection on any signal out from the COM module. ESD protection has to be placed as near as possible to the ESD source - this is the connector with external access on the COM baseboard.

A helpful guide is available from TI: ESD Protection Layout Guide

The module supports spread spectrum in order to reduce the electromagnetic interference (EMI). This will normally reduce the EMI between 9 and 12 dB and so this can decrease your shielding requirements. We highly recommend to have controlled impedances and wires as short as possible in your layout designs.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power Consumption and Cooling

Depending on your product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d.** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d.** and **t.b.d.** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

For the optimal cooling performance we recommend to use F&S heat spreader set MHS.PC100.1. For more information please contact with us.

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

15 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags. The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 11: Matrix Code Sticker

18 Appendix

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