Hardware Documentation

efus™MX8MP
HW Revision 1.00

Preliminary

Version 002
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About This Document

This document describes how to use the efus™MX8MP board with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
24.04.2022	001	All		-	Initial Version (Preliminary)	HF
28.07.2023	002	All		-	Removed 2nd WLAN chapter, change style of table B2B Connector	HF

V	Version
A, M, R	Added, Modified, Removed
Au	Author

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1 Block Diagram

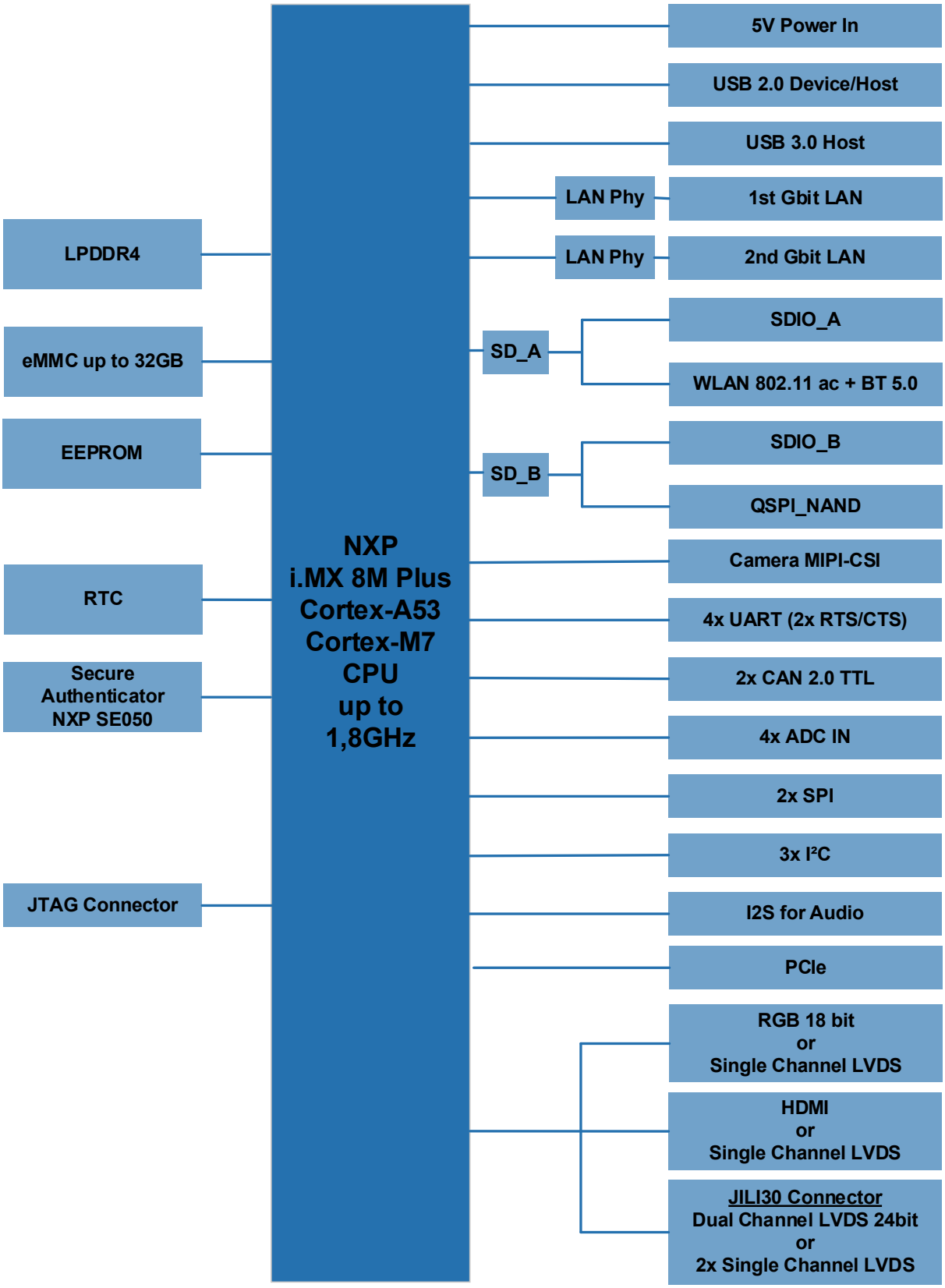

Figure 1: efusMX8MP Block Diagram

2 Mechanical Dimensions

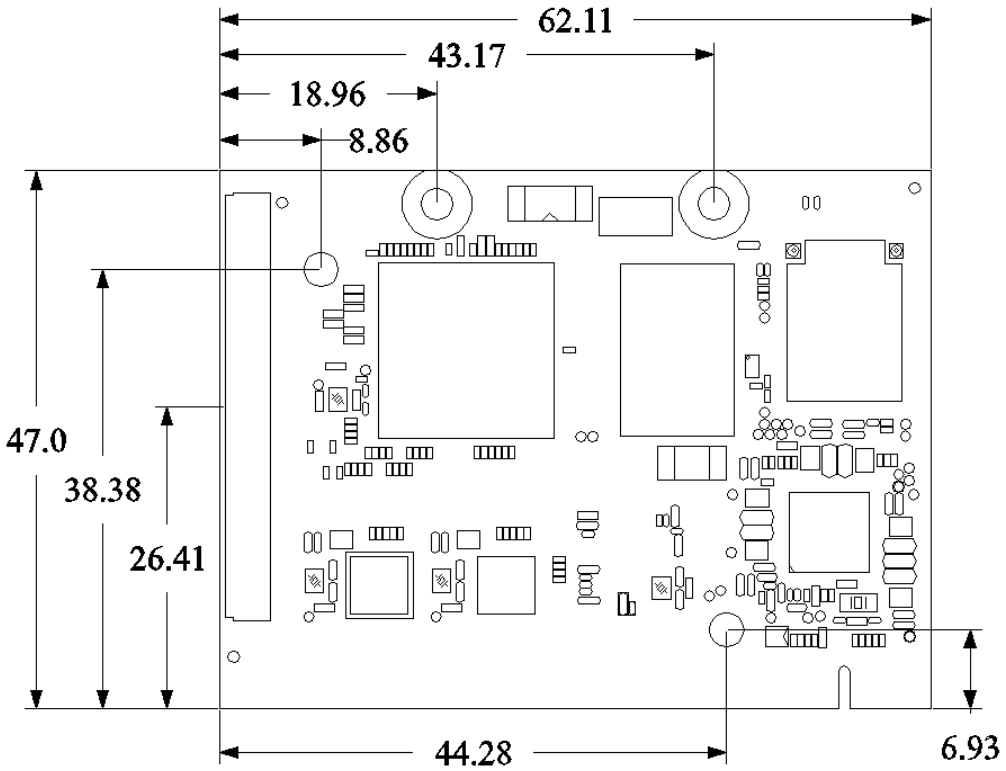

Figure 2: Mechanical Dimensions [mm]

Dimensions	Description
Size	62.1mm x 47mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	4.65mm
Height of the parts on the bottom side	0.9mm
Weight	16gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 B2B Connector (J3)

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
1	VDD_VIN		PWR I	5V	Power Supply Input
3	VDD_VIN		PWR I	5V	Power Supply Input
5	VDD_VIN		PWR I	5V	Power Supply Input
7	GND		PWR	GND	
9	VDD_VBAT		PWR I	3.0V	2.2 < VBAT < 3.45V
11	COK	NC	X	X	
13	-	-	-	-	
15	UART_C_RXD	SAI3_TXFS	I	3.3V	UART_C Data Receive
17	UART_C_TXD	SAI3_TXC	O	3.3V	UART_C Data Transmit
19	UART_C_RTS	UART4_RXD	O	3.3V	UART_C Ready To Send
21	UART_C_CTS	UART4_TXD	I	3.3V	UART_C Clear To Send
23	PWM_B	SPDIF_EXT_CLK	O	3.3V	
25	PWM_A	SAI3_MCLK	O	3.3V	
27	GND		PWR		
29	CAN_A_TX	SPDIF_TX	O	3.3V	
31	CAN_A_RX	SPDIF_RX	I	3.3V	
33	GND		PWR		
35	CAN_B_TX	UART3_RXD	O	3.3V	
37	CAN_B_RX	UART3_TXD	I	3.3V	
39	GND		PWR		
41	MPCIE_CTX_P	PCIE_TXN_P	O		
43	MPCIE_CTX_N	PCIE_TXN_N	O		
45	GND		PWR		
47	MPCIE_CRX_P	PCIE_RXN_P	I		
49	MPCIE_CRX_N	PCIE_RXN_N	I		
51	GND		PWR		
53	MPCIE_CLK_P	PCIE_REF_PAD_CL	O		
55	MPCIE_CLK_N	PCIE_REF_PAD_CL	O		
57	GND		PWR		
59	MPCIE_PERST	SAI3_RXD	O		
61	MPCIE_WAKE	SAI3_TXD	I		
63	GND		PWR		
65	SD_B_DATA2	NAND_DATA06	I/O	SD_B_VCC	
67	SD_B_DATA3	NAND_DATA07	I/O	SD_B_VCC	
69	SD_B_CMD	NAND_WP_B	O	SD_B_VCC	
71	SD_B_VCC		PWR	1.8V / 3.3V	Mounting Option; Default: 3.3V
73	SD_B_CLK	NAND_WE_B	O	SD_B_VCC	
75	GND		PWR		
77	SD_B_DATA0	NAND_DATA04	I/O	SD_B_VCC	
79	SD_B_DATA1	NAND_DATA05	I/O	SD_B_VCC	
81	SD_B_WP	NAND_DATA03	I	SD_B_VCC	
83	SD_B_CD	NAND_DATA02	I	SD_B_VCC	
85	GND		PWR		

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
87	BL_PWM	GPIO1_IO10	O	3.3V	
89	BL_ON	GPIO1_IO01	O	3.3V	
91	GND		PWR		
93	LCD_CLK		O		LT9211 MIPI to RGB IC
95	GND		PWR		
97	LCD_HSYNC		O		LT9211 MIPI to RGB IC
99	LCD_VSYNC		O		LT9211 MIPI to RGB IC
101	GND		PWR		
103	LCD_DATA0		O		LT9211 MIPI to RGB IC
105	LCD_DATA1		O		LT9211 MIPI to RGB IC
107	LCD_DATA2		O		LT9211 MIPI to RGB IC
109	LCD_DATA3		O		LT9211 MIPI to RGB IC
111	LCD_DATA4		O		LT9211 MIPI to RGB IC
113	LCD_DATA5		O		LT9211 MIPI to RGB IC
115	GND		PWR		
117	LCD_DATA6		O		LT9211 MIPI to RGB IC
119	LCD_DATA7		O		LT9211 MIPI to RGB IC
121	LCD_DATA8		O		LT9211 MIPI to RGB IC
123	LCD_DATA9		O		LT9211 MIPI to RGB IC
125	LCD_DATA10		O		LT9211 MIPI to RGB IC
127	LCD_DATA11		O		LT9211 MIPI to RGB IC
129	GND		PWR		
131	LCD_DATA12		O		LT9211 MIPI to RGB IC
133	LCD_DATA13		O		LT9211 MIPI to RGB IC
135	LCD_DATA14		O		LT9211 MIPI to RGB IC
137	LCD_DATA15		O		LT9211 MIPI to RGB IC
139	LCD_DATA16		O		LT9211 MIPI to RGB IC
141	LCD_DATA17		O		LT9211 MIPI to RGB IC
143	GND		PWR		
145	LCD_DE		O		LT9211 MIPI to RGB IC
147	GND		PWR		
149	VLCD_ON	GPIO1_IO05	O	3.3V	
151	I2C_A_SDA	I2C3_SDA	I/O	3.3V	I2C A Data lane
153	I2C_A_IRQ	GPIO1_IO09	I	3.3V	I2C A active low interrupt
155	I2C_A_SCL	I2C3_SCL	I/O	3.3V	I2C A Clock lane
157	I2C_A_RST	GPIO1_IO08	O	3.3V	I2C A reset out
159	GND		PWR		
161	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I		MIPI_CSI Camera Interface
163	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I		MIPI_CSI Camera Interface
165	CSI_A_DATA1_N	MIPI_CSI1_D1_N	I		MIPI_CSI Camera Interface
167	CSI_A_DATA1_P	MIPI_CSI1_D1_P	I		MIPI_CSI Camera Interface
169	CSI_A_DATA2_N	MIPI_CSI1_D2_N	I		MIPI_CSI Camera Interface
171	CSI_A_DATA2_P	MIPI_CSI1_D2_P	I		MIPI_CSI Camera Interface
173	CSI_A_DATA3_N	MIPI_CSI1_D3_N	I		MIPI_CSI Camera Interface
175	CSI_A_DATA3_P	MIPI_CSI1_D3_P	I		MIPI_CSI Camera Interface
177	CSI_A_CLK_N	MIPI_CSI1_CLK_N	O		MIPI_CSI Camera Interface
179	CSI_A_CLK_P	MIPI_CSI1_CLK_P	O		MIPI_CSI Camera Interface
181	GND		PWR		
183	CAMINT_MCLK	NC			Not Connected

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
185	GND		PWR		
187	CAMINT_YDATA9	NC			Not Connected
189	CAMINT_VCAM	NC			Not Connected
191	CAMINT_HREF	NC			Not Connected
193	CAMINT_PWDN	NC			Not Connected
195	CAMINT_VSYNC	NC			Not Connected
197	I2C_C_CAMRST	NC			Not Connected
199	GND		PWR		
201	NC	-			Not Connected
203	NC	-			Not Connected
205	NC	-			Not Connected
207	NC	-			Not Connected
209	GND		PWR		
211	CAM_A_IN	NC			Not Connected
213	CAM_A_GND	NC			Not Connected
215	GND		PWR		
217	USB_OTG_VBUS		I		
219	USB_OTG_PWRN	GPIO1_IO14	O		
221	USB_OTG_OC	GPIO1_IO15	I		
223	USB_OTG_ID	USB2_ID	I		
225	USB_OTG_DN	USB2_D_N	I/O		
227	USB_OTG_DP	USB2_D_P	I/O		
229	GND		PWR		
231	GND		PWR		
2	VDD_VIN		PWR I	5V	Power Supply Input
4	VDD_VIN		PWR I	5V	Power Supply Input
6	VDD_VIN		PWR I	5V	Power Supply Input
8	GND		PWR	GND	
10	VDD_3V3		O	3.3V	Max. 20mA output
12	RESET_IN		I	3.3V	
14	!RESET_OUT	GPIO1_IO13	O	3.3V	
16	SD_A_WP	SD2_WP	I	SD_A_VCC	Shared with WIFI
18	SD_A_CD	SD2_CD_B	I	SD_A_VCC	Shared with WIFI
20	SD_A_DAT2	SD2_DATA2	I/O	SD_A_VCC	Shared with WIFI
22	SD_A_DAT3	SD2_DATA3	I/O	SD_A_VCC	Shared with WIFI
24	SD_A_CMD	SD2_CMD	O	SD_A_VCC	Shared with WIFI
26	SD_A_VCC		PWR	1.8V / 3.3V	Programmable with PMIC
28	SD_A_CLK	SD2_CLK	O	SD_A_VCC	Shared with WIFI
30	GND		PWR		
32	SD_A_DAT0	SD2_DATA0	I/O	SD_A_VCC	Shared with WIFI
34	SD_A_DAT1	SD2_DATA1	I/O	SD_A_VCC	Shared with WIFI
36	SD_A_RST	SD2_RESET_B	O	SD_A_VCC	Shared with WIFI
38	ADC_IN3	ADS1015: AIN3	I	3.3V	ADS1015 (option)
40	ADC_IN2	ADS1015: AIN2	I	3.3V	ADS1015 (option)
42	ADC_IN1	ADS1015: AIN1	I	3.3V	ADS1015 (option)
44	ADC_IN0	ADS1015: AIN0	I	3.3V	ADS1015 (option)
46	GND		PWR		

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
48	BOOTSEL		I		
50	SPI_B_MISO	ECSPI2_MISO		3.3V	
52	SPI_B_MOSI	ECSPI2_MOSI		3.3V	
54	SPI_B_SCLK	ECSPI2_SCLK		3.3V	
56	SPI_B_SS0	ECSPI2_SS0		3.3V	
58	SPI_B_SS1	NAND_READY_B		1.8V / 3.3V	Mounting Option; Default: 3.3V
60	SPI_B_IRQ1N	NAND_CE3_B		1.8V / 3.3V	Mounting Option; Default: 3.3V
62	SPI_B_IRQ2N	NAND_CE1_B		1.8V / 3.3V	Mounting Option; Default: 3.3V
64	GND		PWR		
66	SPI_A_MISO	UART2_RXD		3.3V	
68	SPI_A_MOSI	UART1_TXD		3.3V	
70	SPI_A_SCLK	UART1_RXD		3.3V	
72	SPI_A_SS0	UART2_TXD		3.3V	
74	SPI_A_SS1	NAND_CE0_B		1.8V / 3.3V	Mounting Option; Default: 3.3V
76	SPI_A_IRQ1N	NAND_DQS		1.8V / 3.3V	Mounting Option; Default: 3.3V
78	SPI_A_IRQ2N	NAND_ALE		1.8V / 3.3V	Mounting Option; Default: 3.3V
80	GND		PWR		
82	I2C_B_SDA	I2C4_SDA	I/O	3.3V	I2C B Data lane
84	I2C_B_SCL	I2C4_SCL	I/O	3.3V	I2C B Clock lane
86	I2C_B_IRQ	SAI3_RXC	I	3.3V	I2C B active low interrupt
88	I2C_B_RST	SAI3_RXFS	O	3.3V	I2C B reset out
90	GND		PWR		
92	UART_A_RXD	SAI2_RXC	I	3.3V	UART_A Data Receive
94	UART_A_TXD	SAI2_RXFS	O	3.3V	UART_A Data Transmit
96	UART_D_RXD	NAND_DATA00	I	1.8V / 3.3V	Mounting Option; Default: 3.3V
98	UART_D_TXD	NAND_DATA01	O	1.8V / 3.3V	Mounting Option; Default: 3.3V
100	GND		PWR		
102	UART_B_RXD	ECSPI1_SCLK	I	3.3V	UART_B Data Receive
104	UART_B_TXD	ECSPI1_MOSI	O	3.3V	UART_B Data Transmit
106	UART_B_RTS	ECSPI1_MISO	O	3.3V	UART_B Ready To Send
108	UART_B_CTS	ECSPI1_SS0	I	3.3V	UART_B Clear To Send
110	GND		PWR		
112	I2S_A_MCLK	SAI2_MCLK	O	3.3V	
114	GND		PWR		
116	I2S_A_TXFS	SAI2_TXFS	O	3.3V	
118	GND		PWR		
120	I2S_A_TXC	SAI2_TXC	O	3.3V	
122	GND		PWR		
124	I2S_A_RXD	SAI2_RXD0	O	3.3V	
126	I2S_A_TXD	SAI2_TXD0	I	3.3V	
128	GND		PWR		

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
130	I2C_C_SDA	HDMI_DDC_SDA	I/O	3.3V	I2C C Data lane
132	I2C_C_SCL	HDMI_DDC_SCL	I/O	3.3V	I2C C Clock lane
134	VDD_3V3		O	3.3V	
136	GND		PWR		
138	DISP_D2_P		O		HDMI or LVDS (mounting option)
140	DISP_D2_N		O		HDMI or LVDS (mounting option)
142	DISP_D1_P		O		HDMI or LVDS (mounting option)
144	DISP_D1_N		O		HDMI or LVDS (mounting option)
146	DISP_D0_P		O		HDMI or LVDS (mounting option)
148	DISP_D0_N		O		HDMI or LVDS (mounting option)
150	DISP_CLK_P		O		HDMI or LVDS (mounting option)
152	DISP_CLK_N		O		HDMI or LVDS (mounting option)
154	DISP_D3_P		O		
156	DISP_D3_N		I/O		
158	HDMI_HPD	HDMI_HPD	I		
160	GND		PWR		
162	ETH_B_D4N		I/O		LAN Phy RTL8211FD
164	ETH_B_D4P		I/O		LAN Phy RTL8211FD
166	ETH_B_ACTLEDN		O		Ethernet B Led Action
168	ETH_B_D3N		I/O		LAN Phy RTL8211FD
170	ETH_B_D3P		I/O		LAN Phy RTL8211FD
172	GND		PWR		
174	ETH_B_D2N		I/O		LAN Phy RTL8211FD
176	ETH_B_D2P		I/O		LAN Phy RTL8211FD
178	ETH_B_LINKLEDN		O		Ethernet B Led Link
180	ETH_B_D1N		I/O		LAN Phy RTL8211FD
182	ETH_B_D1P		I/O		LAN Phy RTL8211FD
184	GND		PWR		
186	ETH_CTREF		NC		Not connected
188	ETH_A_D4N		I/O		LAN Phy RTL8211FD
190	ETH_A_D4P		I/O		LAN Phy RTL8211FD
192	ETH_A_ACTLEDN		O		Ethernet A Led Action
194	ETH_A_D3N		I/O		LAN Phy RTL8211FD
196	ETH_A_D3P		I/O		LAN Phy RTL8211FD
198	VDD_3V3		PWR O	3.3V	Ethernet LEDs Supply Voltage
200	ETH_A_D2N		I/O		LAN Phy RTL8211FD
202	ETH_A_D2P		I/O		LAN Phy RTL8211FD
204	ETH_A_LINKLEDN		O		Ethernet A Led Link
206	ETH_A_D1N		I/O		LAN Phy RTL8211FD
208	ETH_A_D1P		I/O		LAN Phy RTL8211FD
210	GND		PWR		
212	USB_HOST_PWRN	GPIO1_IO12	O		
214	USB_HOST_DN	USB1_D_N	I/O		
216	USB_HOST_DP	USB1_D_P	I/O		
218	GND		PWR		
220	USB_HOST_SS_RXN		I/O		
222	USB_HOST_SS_RXP		I/O		
224	GND		PWR		

Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
226	USB_HOST_SS_TXN		I/O		
228	SB_HOST_SS_TXP		I/O		
230	GND		PWR		
232	GND		PWR		

Table 2: B2B Connector Pin Layout

4 Interfaces

4.1 Ethernet

efus™MX8MP board has two standard Gigabit Ethernet (Gbit LAN) connections. The LAN phy RealTek RTL8211FD is used. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm). LED signal can drive a 3.3V powered LED with 5mA directly to GND. If Ethernet is not used please leave signals unconnected.

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
192	ETH_A_ACTLEDN		O		Ethernet A Led Action
206	ETH_A_D1N		I/O		LAN Phy RTL8211FD
208	ETH_A_D1P		I/O		LAN Phy RTL8211FD
200	ETH_A_D2N		I/O		LAN Phy RTL8211FD
202	ETH_A_D2P		I/O		LAN Phy RTL8211FD
194	ETH_A_D3N		I/O		LAN Phy RTL8211FD
196	ETH_A_D3P		I/O		LAN Phy RTL8211FD
188	ETH_A_D4N		I/O		LAN Phy RTL8211FD
190	ETH_A_D4P		I/O		LAN Phy RTL8211FD
204	ETH_A_LINKLEDN		O		Ethernet A Led Link
166	ETH_B_ACTLEDN		O		Ethernet B Led Action
180	ETH_B_D1N		I/O		LAN Phy RTL8211FD
182	ETH_B_D1P		I/O		LAN Phy RTL8211FD
174	ETH_B_D2N		I/O		LAN Phy RTL8211FD
176	ETH_B_D2P		I/O		LAN Phy RTL8211FD
168	ETH_B_D3N		I/O		LAN Phy RTL8211FD
170	ETH_B_D3P		I/O		LAN Phy RTL8211FD
162	ETH_B_D4N		I/O		LAN Phy RTL8211FD
164	ETH_B_D4P		I/O		LAN Phy RTL8211FD
178	ETH_B_LINKLEDN		O		Ethernet B Led Link
186	ETH_CTREF		NC		Not connected
172	GND		PWR		
184	GND		PWR		
198	VDD_3V3		PWR O	3.3V	Ethernet LEDs Supply Voltage

Table 3: Ethernet Interface

4.2 WLAN and Bluetooth

The efus™MX8MP contains a certified high performance WLAN and Bluetooth module.

The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan pre-certificates.

Please contact support@fs-net.de for additional information about process of certification. The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used.

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: SDIO A Interface is used for onboard WLAN module. If WLAN module is mounted SD_A is not available on the B2B connector.

4.3 USB

efus™MX8MP provides 1x USB3.0 Host only and 1x USBOTG2.0 connection. The 90 Ohm differential pair of USB signals do not need any termination. For external ports EMV and ESD protection is required nearby the USB connector on the base board. If the USB port is not used please leave open.

Pin	Signal Name	CPU Pad	I/O	Description
217	USB_OTG_VBUS		I/O	USB OTG2.0 Supply Voltage (Input @Device Mode)
219	USB_OTG_PWRN	GPIO1_IO14	O	USB OTG2.0 Power On
221	USB_OTG_OC	GPIO1_IO15	I	
223	USB_OTG_ID	USB2_ID	I	USB OTG2.0 ID
225	USB_OTG_DN	USB2_D_N	I/O	USB OTG2.0 Data Lane-
227	USB_OTG_DP	USB2_D_P	I/O	USB OTG2.0 Data Lane+
212	USB_HOST_PWRN	GPIO1_IO12	O	USB3.0 Host Power On
214	USB_HOST_DN	USB1_D_N	I/O	USB3.0 Host Data Lane- (USB2.0)
216	USB_HOST_DP	USB1_D_P	I/O	USB3.0 Host Data Lane+ (USB2.0)
220	USB_HOST_SS_RXN		I/O	USB3.0 Host Receive Lane-
222	USB_HOST_SS_RXP		I/O	USB3.0 Host Receive Lane+
226	USB_HOST_SS_TXN		I/O	USB3.0 Host Transmit Lane-
228	USB_HOST_SS_TXP		I/O	USB3.0 Host Transmit Lane+

Table 4: USB Interface

4.4 Serial Interfaces

On efus™MX8MP board it is allowed for the users to use these serial interfaces, which are given below. All of these serial Interfaces are 3.3V compliant.

- UART: 2 x UART with RTS/CTS and 2 x UART without RTS/CTS
- I2C: 3 x I2C
- SPI: 2 x SPI
- CAN: 2 x CAN Bus

4.4.1 UART Interfaces

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
92	UART_A_RXD	SAI2_RXC	I	3.3V	UART_A Data Receive
94	UART_A_TXD	SAI2_RXFS	O	3.3V	UART_A Data Transmit
108	UART_B_CTS	ECSPI1_SS0	I	3.3V	UART_B Clear To Send
106	UART_B_RTS	ECSPI1_MISO	O	3.3V	UART_B Ready To Send
102	UART_B_RXD	ECSPI1_SCLK	I	3.3V	UART_B Data Receive
104	UART_B_TXD	ECSPI1_MOSI	O	3.3V	UART_B Data Transmit
21	UART_C_CTS	UART4_TXD	I	3.3V	UART_C Clear To Send
19	UART_C_RTS	UART4_RXD	O	3.3V	UART_C Ready To Send
15	UART_C_RXD	SAI3_TXFS	I	3.3V	UART_C Data Receive
17	UART_C_TXD	SAI3_TXC	O	3.3V	UART_C Data Transmit
96	UART_D_RXD	NAND_DATA00	I	1.8V / 3.3V	Mounting Option; Default: 3.3V
98	UART_D_TXD	NAND_DATA01	O	1.8V / 3.3V	Mounting Option; Default: 3.3V

Table 5: Serial Interfaces – UART

4.4.2 CAN Interfaces

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
29	CAN_A_TX	SPDIF_TX	O	3.3V	CAN A Transmit data
31	CAN_A_RX	SPDIF_RX	I	3.3V	CAN A Receive data
35	CAN_B_TX	UART3_RXD	O	3.3V	CAN B Transmit data
37	CAN_B_RX	UART3_TXD	I	3.3V	CAN B Receive data

**Can transceivers must be placed on Baseboard*

Table 6: Serial Interfaces – CAN

4.4.3 I2C Interfaces

The SOM offers three independent I2C interfaces on the MXM connector.

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
151	I2C_A_SDA	I2C3_SDA	I/O	3.3V	I2C A Data lane
153	I2C_A_IRQ	GPIO1_IO09	I	3.3V	I2C A active low interrupt
155	I2C_A_SCL	I2C3_SCL	I/O	3.3V	I2C A Clock lane
157	I2C_A_RST	GPIO1_IO08	O	3.3V	I2C A reset out
82	I2C_B_SDA	I2C4_SDA	I/O	3.3V	I2C B Data lane
84	I2C_B_SCL	I2C4_SCL	I/O	3.3V	I2C B Clock lane
86	I2C_B_IRQ	SAI3_RXC	I	3.3V	I2C B active low interrupt
88	I2C_B_RST	SAI3_RXFS	O	3.3V	I2C B reset out
130	I2C_C_SDA	HDMI_DDC_SDA	I/O	3.3V	I2C C Data lane
132	I2C_C_SCL	HDMI_DDC_SCL	I/O	3.3V	I2C C Vlock lane
--	I2C_E_SDA	I2C1_SDA	I/O	3.3V	Internal I2C bus; 2k49 pullup to 3.3V
--	I2C_E_SCL	I2C1_SCL	I/O	3.3V	Internal I2C bus; 2k49 pullup to 3.3V

Table 7: Serial Interfaces – I2C

All on board I2C device are connected to I2C_E.

I2C	Device	Address	Comment
I2C_E	EEPROM 24C02	0x50 (1010 000)	
I2C_E	ADS1015	0x49 (1001 001)	PCB Rev 100:0x48 and conflict with SE050.
I2C_E	LT9211	0x5A	
I2C_E	PCF852563ATL	0x51 (1010 001)	
I2C_E_	SE05x	0x48 (1001 000)	

Table 8: I2C Devices

4.4.4 SPI Interfaces

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
50	SPI_B_MISO	ECSPI2_MISO	I	3.3V	SPI B Master In Slave Out (Data In)
52	SPI_B_MOSI	ECSPI2_MOSI	O	3.3V	SPI B Master Out Slave In (Data Out)
54	SPI_B_SCLK	ECSPI2_SCLK	O	3.3V	SPI B Serial Peripheral Clock
56	SPI_B_SS0	ECSPI2_SS0	O	3.3V	SPI B Chip Select (Slave Select 0)
58	SPI_B_SS1	NAND_READY_B	O	1.8V / 3.3V	SPI B Chip Select (Slave Select 1) Mounting Option; Default: 3.3V
60	SPI_B_IRQ1N	NAND_CE3_B	I	1.8V / 3.3V	SPI B Active low interrupt 100k pull up Mounting Option; Default: 3.3V
62	SPI_B_IRQ2N	NAND_CE1_B	I	1.8V / 3.3V	SPI B Active low interrupt 100k pull up Mounting Option; Default: 3.3V
66	SPI_A_MISO	UART2_RXD	I	3.3V	SPI A Master In Slave Out (Data In)
68	SPI_A_MOSI	UART1_TXD	O	3.3V	SPI A Master Out Slave In (Data Out)
70	SPI_A_SCLK	UART1_RXD	O	3.3V	SPI A Serial Peripheral Clock
72	SPI_A_SS0	UART2_TXD	O	3.3V	SPI A Chip Select (Slave Select 0)
74	SPI_A_SS1	NAND_CE0_B	O	1.8V / 3.3V	SPI A Chip Select (Slave Select 0) Mounting Option; Default: 3.3V
76	SPI_A_IRQ1N	NAND_DQS	I	1.8V / 3.3V	SPI A Active low interrupt 100k pull up Mounting Option; Default: 3.3V
78	SPI_A_IRQ2N	NAND_ALE	I	1.8V / 3.3V	SPI A Active low interrupt 100k pull up Mounting Option; Default: 3.3V

Table 9: Serial Interfaces – SPI

4.5 SD Card

The interface is supporting an SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org. Pullups are not integrated on the module. Unused signals should be left unconnected. SD Interface supply voltage can be 3.3V or 1.8V.

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
16	SD_A_WP	SD2_WP	I	SD_A_VCC	Shared with WIFI
18	SD_A_CD	SD2_CD_B	I	SD_A_VCC	Shared with WIFI
28	SD_A_CLK	SD2_CLK	O	SD_A_VCC	Shared with WIFI
24	SD_A_CMD	SD2_CMD	O	SD_A_VCC	Shared with WIFI
32	SD_A_DAT0	SD2_DATA0	I/O	SD_A_VCC	Shared with WIFI
34	SD_A_DAT1	SD2_DATA1	I/O	SD_A_VCC	Shared with WIFI
20	SD_A_DAT2	SD2_DATA2	I/O	SD_A_VCC	Shared with WIFI
22	SD_A_DAT3	SD2_DATA3	I/O	SD_A_VCC	Shared with WIFI
26	SD_A_VCC		O	1.8V / 3.3V	Programmable with PMIC
36	SD_A_RST	SD2_RESET_B	O	SD_A_VCC	Shared with WIFI

Table 10: SD Card A Interface

Pin	Signal Name	CPU Pad	I/O	Voltage	Description
81	SD_B_WP	NAND_DATA03	I	SD_B_VCC	
83	SD_B_CD	NAND_DATA02	I	SD_B_VCC	
73	SD_B_CLK	NAND_WE_B	O	SD_B_VCC	
69	SD_B_CMD	NAND_WP_B	O	SD_B_VCC	
77	SD_B_DAT0	NAND_DATA04	I/O	SD_B_VCC	Shared with QSPI
79	SD_B_DAT1	NAND_DATA05	I/O	SD_B_VCC	Shared with QSPI
65	SD_B_DAT2	NAND_DATA06	I/O	SD_B_VCC	Shared with QSPI
67	SD_B_DAT3	NAND_DATA07	I/O	SD_B_VCC	Shared with QSPI
71	SD_B_VCC		O	1.8V / 3.3V	Mounting option. Default: 3.3V

Table 11: SD Card B Interface

4.6 Audio

efus™MX8MP board supports SAI Interface (Serial Audio Interface) which is including industry-standard codecs. There are no external audio codecs on this board.

Pin	Signal Name	CPU Pad	I/O	Description
126	I2S_DIN	SAI2_TXD0	I	I2S Data In
124	I2S_DOUT	SAI2_RXD0	O	I2S Data Out
116	I2S_LRCLK	SAI2_TXFS	O	I2S Frame Clock
112	I2S_MCLK	SAI2_MCLK	O	I2S System Master Clock
120	I2S_SCLK	SAI2_TXC	O	I2S Bit Clock

Table 12: Audio Interface

4.7 Display Interfaces

efus™MX8MP board support HDMI 2.0a, LVDS and RGB interface.

Efus has two connectors for display data: J2 and J3 (B2B)

J2 Connector Type: FI-X30SSLA-HF-R2500

Mating Connector (cable side): FI-X30H & FI-X30HL

4.7.1 JILI30 Connector: Dual Channel LVDS

In this configuration you can connect one display.

J2 Pin	Signal Name	CPU Pad	I/O	Description
1	LVDSA_TX0_M	LVDS0_D0_N	O	LVDSA | Data Lane 0-
2	LVDSA_TX0_P	LVDS0_D0_P	O	LVDSA | Data Lane 0+
3	LVDSA_TX1_M	LVDS0_D1_N	O	LVDSA | Data Lane 1-
4	LVDSA_TX1_P	LVDS0_D1_P	O	LVDSA | Data Lane 1+
5	LVDSA_TX2_M	LVDS0_D2_N	O	LVDSA | Data Lane 2-
6	LVDSA_TX2_P	LVDS0_D2_P	O	LVDSA | Data Lane 2+
7	GND		PWR	
8	LVDSA_CLK_M	LVDS0_CLK_N	O	LVDSB | Clock Signal-
9	LVDSA_CLK_P	LVDS0_CLK_P	O	LVDSB | Clock Signal+
10	LVDSA_TX3_M	LVDS0_D3_N	O	LVDSB | Data Lane 3-
11	LVDSA_TX3_P	LVDS0_D3_P	O	LVDSB | Data Lane 3+
12	LVDSB_TX0_M	LVDS1_D0_N	O	LVDSB | Data Lane 0-
13	LVDSB_TX0_P	LVDS1_D0_P	O	LVDSB | Data Lane 0+
14	GND		PWR	
15	LVDSB_TX1_M	LVDS1_D1_N	O	LVDSB | Data Lane 1-
16	LVDSB_TX1_P	LVDS1_D2_P	O	LVDSB | Data Lane 1+
17	GND		PWR	
18	LVDSB_TX2_M	LVDS1_D2_N	O	LVDSB | Data Lane 2-
19	LVDSB_TX2_P	LVDS1_D2_P	O	LVDSB | Data Lane 2+
20	LVDSB_CLK_M	LVDS1_CLK_N	O	LVDSB | Clock Signal-
21	LVDSB_CLK_P	LVDS1_CLK_P	O	LVDSB | Clock Signal+
22	LVDSB_TX3_M	LVDS1_D3_N	O	LVDSB | Data Lane 3-
23	LVDSB_TX3_P	LVDS1_D3_P	O	LVDSB | Data Lane 3+
24	GND		PWR	

25	I2C_LVDS_SDA	I2C2_SD	I/O	I2C Touch Control Serial Data; pullup 2k49 to 3.3V
26	I2C_LVDS_IRQ / VLCDON	NAND_RE_B	I/O	VLCD Enable
27	I2C_LVDS_SCL	I2C2_SCL	O	I2C Touch Control Serial Clock; pullup 2k49 to 3.3V
28	LVDS_RST / VLCD	GPIO1_IO06	O (PWR)	LVDS_RST (optional: VLCD 3.3V(default) / 5.0V)
29	VLCD		PWR O	3.3V(default) / 5.0V
30	VLCD		PWR O	3.3V(default) / 5.0V

Table 13: J2 Dual Channel LVDS Display Connector Pin Layout

4.7.2 JILI30 Connector: 2x Single Channel LVDS

Instead of using both LVDS channels of i.MX8M Plus, there is an option to use LVDS from on-board MIPI to LVDS converter IC LT9211. The advantage is, that we can drive two independent single channel LVDS displays.

Note: This function is a mounting option and not guaranteed for the final product. Ask support@fs-net.de for more information.

J2 Pin	Signal Name	CPU Pad	I/O	Description
1	LVDSA_TX0_M	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 0-
2	LVDSA_TX0_P	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 0+
3	LVDSA_TX1_M	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Lane 1-
4	LVDSA_TX1_P	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 1+
5	LVDSA_TX2_M	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 2-
6	LVDSA_TX2_P	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 2+
7	GND		PWR	
8	LVDSA_CLK_M	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Clock Signal-
9	LVDSA_CLK_P	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Clock Signal+
10	LVDSA_TX3_M	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 3-
11	LVDSA_TX3_P	LT9211	O	LVDSA | MIPI_DSI1 to LVDS Data Lane 3+
12	LVDSB_TX0_M	LVDS1_D0_N	O	LVDSB | MIPI_DSI1 to LVDS Data Lane 0-
13	LVDSB_TX0_P	LVDS1_D0_P	O	LVDSB | MIPI_DSI1 to LVDS Data Lane 0+
14	GND		PWR	

15	LVDSB_TX1_M	LVDS1_D1_N	O	LVDSB | MIPI_DSI1 Data Lane 1-
16	LVDSB_TX1_P	LVDS1_D2_P	O	LVDSB | MIPI_DSI1 Data Lane 1+
17	GND		PWR	
18	LVDSB_TX2_M	LVDS1_D2_N	O	LVDSB | MIPI_DSI1 Data Lane 2-
19	LVDSB_TX2_P	LVDS1_D2_P	O	LVDSB | MIPI_DSI1 Data Lane 2+
20	LVDSB_CLK_M	LVDS1_CLK_N	O	LVDSB | MIPI_DSI1 Clock Signal-
21	LVDSB_CLK_P	LVDS1_CLK_P	O	LVDSB | MIPI_DSI1 Clock Signal+
22	LVDSB_TX3_M	LVDS1_D3_N	O	LVDSB | MIPI_DSI1 Data Lane 3-
23	LVDSB_TX3_P	LVDS1_D3_P	O	LVDSB | MIPI_DSI1 Data Lane 3+
24	GND		PWR	
25	I2C_LVDS_SDA	I2C2_SD	I/O	I2C Touch Control Serial Data; pullup 2k49 to 3.3V
26	I2C_LVDS_IRQ / VLCDON	NAND_RE_B	I/O	VLCD Enable
27	I2C_LVDS_SCL	I2C2_SCL	O	I2C Touch Control Serial Clock; pullup 2k49 to 3.3V
28	LVDS_RST / VLCD	GPIO1_IO06	O (PWR)	LVDS_RST (optional: VLCD 3.3V(default) / 5.0V)
29	VLCD		PWR O	3.3V(default) / 5.0V
30	VLCD		PWR O	3.3V(default) / 5.0V

Table 14: J2 Single Channel LVDS Display Connector Pin Layout

4.7.3 MXM-2 Gold finger Connector J3: RGB Interface

efusMX8MP offers 18 Bit RGB interface on B2B connector J2. The display data is generated by using the MIPI to RGB converter LT9211.

J3 Pin	Signal Name	CPU Pad	I/O	Description
105	LCD_R1	LT9211	O	MIPI_DSI1 to RGB
107	LCD_R2	LT9211	O	MIPI_DSI1 to RGB
103	LCD_R0	LT9211	O	MIPI_DSI1 to RGB
109	LCD_R3	LT9211	O	MIPI_DSI1 to RGB
111	LCD_R4	LT9211	O	MIPI_DSI1 to RGB
113	LCD_R5	LT9211	O	MIPI_DSI1 to RGB
117	LCD_G0	LT9211	O	MIPI_DSI1 to RGB
119	LCD_G1	LT9211	O	MIPI_DSI1 to RGB

121	LCD_G2	LT9211	O	MIPI_DSI1 to RGB
123	LCD_G3	LT9211	O	MIPI_DSI1 to RGB
125	LCD_G4	LT9211	O	MIPI_DSI1 to RGB
127	LCD_G5	LT9211	O	MIPI_DSI1 to RGB
131	LCD_R0	LT9211	O	MIPI_DSI1 to RGB
133	LCD_R1	LT9211	O	MIPI_DSI1 to RGB
135	LCD_R2	LT9211	O	MIPI_DSI1 to RGB
137	LCD_R3	LT9211	O	MIPI_DSI1 to RGB
139	LCD_R4	LT9211	O	MIPI_DSI1 to RGB
141	LCD_R5	LT9211	O	MIPI_DSI1 to RGB
93	LCD_CLK	LT9211	O	MIPI_DSI1 to RGB
145	LCD_DE	LT9211	O	MIPI_DSI1 to RGB
97	LCD_HSYNC	LT9211	O	MIPI_DSI1 to RGB
99	LCD_VSYNC	LT9211	O	MIPI_DSI1 to RGB
149	VLCD_ON	GPIO1_IO05	O	VLCD Enable
89	VCFL_ON	GPIO1_IO01	O	Backlight Enable
97	BL_CTRL	GPIO1_IO06	O	Backlight PWM

Table 15: RGB Display Connector Pin Layout

If LT9211 is not mounted (no RGB), all contacts (except 149,89,79) are not connected (NC). This is different to efusA7UL/efusA9.

If the LVDS connector J2 is not assembled on the board, the LVDS signals will be optionally available on the HDMI pins of J3 (B2B). If the J2 is assembled on the board then J3 has HDMI signals as standard instead of LVDS signals. In this case LVDS signals can be reached via J2 connector.

4.7.4 MXM-2 Gold finger Connector J3: HDMI or LVDS Interface

J3 Pin	Signal Name	CPU Pad	I/O	Remark
107	LCD_R2	LVDS0_D2_P	O	LVDSA | Data Lane 2+*1*2
109	LCD_R3	LVDS0_D2_N	O	LVDSA | Data Lane 2-*1*2
111	LCD_R4	LVDS0_D1_P	O	LVDSA | Data Lane 1+*1*2
113	LCD_R5	LVDS0_D1_N	O	LVDSA | Data Lane 1-*1*2
117	LCD_G0	LVDS0_D0_P	O	LVDSA | Data Lane 0+*1*2
119	LCD_G1	LVDS0_D0_N	O	LVDSA | Data Lane 0-*1*2
121	LCD_G2	LVDS0_CLK_P	O	LVDSA | Clock Signal+*1*2
123	LCD_G3	LVDS0_CLK_N	O	LVDSA | Clock Signal-*1*2
125	LCD_G4	LVDS0_D3_P	O	LVDSA | Data Lane 3+*1*2
127	LCD_G5	LVDS0_D3_N	O	LVDSA | Data Lane 3-*1*2
134	V3.3		PWR O	HDMI_DDC_VOUT | LVDS_VOUT
138	HDMI_DATA2_P	LVDS1_D2_P	O	LVDSB | Data Lane 2+*3
140	HDMI_DATA2_N	LVDS1_D2_N	O	LVDSB | Data Lane 2-*3
142	HDMI_DATA1_P	LVDS1_D1_P	O	LVDSB | Data Lane 1+*3
144	HDMI_DATA1_N	LVDS1_D1_N	O	LVDSB | Data Lane 1-*3
146	HDMI_DATA0_P	LVDS1_D0_P	O	LVDSB | Data Lane 0+*3
148	HDMI_DATA0_N	LVDS1_D0_N	O	LVDSB | Data Lane 0-*3
150	HDMI_CLK_P	LVDS1_CLK_P	O	LVDSB | Clock Signal+*3
152	HDMI_CLK_N	LVDS1_CLK_N	O	LVDSB | Clock Signal-*3
154	HDMI_AUXP	LVDS1_D3_P	O	LVDSB | Data Lane 3+*3
156	HDMI_DDCCEC	LVDS1_D3_N	O	LVDSB | Data Lane 3-*3

Table 16: B2B Connector Display Signals Pin Layout

**1 not guaranteed feature for future HW Revision (NC on older revisions)*

**2 if J2 is assembled → NC, if J2 not assembled → LVDS Signals on the connector*

**3 if J2 is assembled → HDMI Signals, if J2 not assembled → LVDS Signals on the connector*

4.8 MIPI-CSI Camera Interface

The board supports one quad lane MIPI-CSI Interface.

J3 Pin	Signal Name	CPU Pads	I/O	Remarks
161	MIPI_CS_D0_N	MIPI_CSI0_DATA0_N	I	MIPI-CSI Data Lane 0-
163	MIPI_CS_D0_P	MIPI_CSI0_DATA0_P	I	MIPI-CSI Data Lane 0+
165	MIPI_CS_D1_N	MIPI_CSI0_DATA1_N	I	MIPI-CSI Data Lane 1-
167	MIPI_CS_D1_P	MIPI_CSI0_DATA1_P	I	MIPI-CSI Data Lane 1+
169	MIPI_CS_D2_N	MIPI_CSI0_DATA2_N	I	MIPI-CSI Data Lane 2-
171	MIPI_CS_D2_P	MIPI_CSI0_DATA2_P	I	MIPI-CSI Data Lane 2+
173	MIPI_CS_D3_N	MIPI_CSI0_DATA3_N	I	MIPI-CSI Data Lane 3-
175	MIPI_CS_D3_P	MIPI_CSI0_DATA3_P	I	MIPI-CSI Data Lane 3+
177	MIPI_CS_CLK_N	MIPI_CSI0_CLK_N	O	MIPI-CSI Clock-
179	MIPI_CS_CLK_P	MIPI_CSI0_CLK_P	O	MIPI-CSI Clock+

Table 17: MIPI-CSI Interface

4.9 PCIE Interface

The efus™MX8MP module supports single lane PCI Express Gen 2. The interface can work as root complex or endpoint (Dual mode operation).

J3 Pin	Signal	CPU Pad	I/O	Voltage	Remarks
41	MPCIE_CTX_P	PCIE_TXN_P	O	1.8V	
43	MPCIE_CTX_N	PCIE_TXN_N	O	1.8V	
47	MPCIE_CRX_P	PCIE_RXN_P	I	1.8V	
49	MPCIE_CRX_N	PCIE_RXN_N	I	1.8V	
53	MPCIE_CLK_P	PCIE_REF_PAD_CLK_P	O	1.8V	
55	MPCIE_CLK_N	PCIE_REF_PAD_CLK_N	O	1.8V	
59	MPCIE_PERST	SAI3_RXD	O	3.3V	mPCIe power reset; no pull-up/-down on module
61	MPCIE_WAKE	SAI3_TXD	I	3.3V	mPCIe wakeup; no pull-up/-down on module

Table 18: PCIE Interface

4.10 WLAN and Bluetooth Interface

The efus™MX8MP contains a certified high performance WLAN and Bluetooth module.

The module is based on NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID: D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: In case WLAN/BT module is mounted only one external SD card interface (SD_B) is available and SD_A is not available.

4.11 JTAG

Not soldered by default.

J1 Pin	Signal Name	I/O	Voltage	Description
1	+VDD_SNVS_1V8	PWR	1.8V	
2	JTAG_TMS	X	1.8V	JTAG Test Mode Select
3	GND	PWR	GND	
4	JTAG_TCK	X	1.8V	JTAG Test Clock
5	GND	PWR	GND	
6	JTAG_TDO	X	1.8V	JTAG Test Data Out
7	NC	X	X	
8	JTAG_TDI	X	1.8V	JTAG Test Data In
9	GND	PWR	GND	
10	JTAG_SRST	X	1.8V	JTAG System Reset

Table 19: JTAG Interface

- For debug only
- Leave unconnected, if you don’t use JTAG
- Don’t put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.12 Power and Power Control Pins

J3 Pin	Signal Name	I/O	Voltage	Description
1…6	VDD_VIN	PWR In	5.0V	Main Power Supply Input Please refer chapter “9 Electrical Characteristic”
9	VDD_VBAT	PWR In	3V	RTC Battery Input, leave open if not used Please refer Electrical characteristic (Ch6)
10	V33OUT / V33_ENABLE	PWR O	3.3V	20mA Output from on module DCDC powered from V5.0
12	!RESET_IN	I	3.3V	Power On Reset Input (active low)
26	SD_A_VCC	O	1.8V/3.3V	NC if WLAN/BT is mounted. Supply Voltage for NVCC_SD2. You need this voltage in case you want to connect external device with separate voltage for I/O.
134	HDMI_DDC_VOUT	O	3.3V	HDMI/LVDS Supply Voltage
149	VLCD_ON	I	3.3V	LCD Enable
198	ETH_VLEDOUT	O	3.3V	Ethernet LED Supply Voltage. Directly connected to 3.3V of PMIC.
217	USB_DEV_VBUS	PWR I/O	5.0V	USB (OTG) Power Supply (Input for Device Mode). This input is connected to USB2_VBUS of CPU.
	GND	PWR	GND	Connect all GND pins to a GND plane

Table 20: Power and Power Control Pins

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory.

V33OUT/V33_ENABLE is the DCDC power supply of the module powered from V5.0. Use as enable for carrier board power regulators.

!RESET_IN is a reset input for the module. It is connected to the PMIC_RST_B.

5 Boot Mode

The CPU of efusMX8MP has fuses to configure the default boot device. By default, it is eMMC or NAND, depending from the soldered mass storage flash memory.

With pin 48 of J3 “BOOTSEL” it is possible to switch between “boot from internal fuses” and “boot from USB serial download”.

So you have the following two boot options:

Boot Device Select	BOOTSEL pin of efus
Boot from internal fuses	Leave open
USB Serial Download	Connect to GND

Table 21: Boot Modes of efus

Additional boot modes such as booting from SD card or QSPI are possible, but soldering options.

6 Flash

6.1 eMMC Flash

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

The efusMX8MP module can support up to 64GB eMMC flash memory.

7 Real Time Clock (RTC)

There is a NXP PCF85263ATL or compatible RTC component implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds over the day.

8 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE050 offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

SE050 Quick start guide: https://www.nxp.com/docs/en/application-note/AN13027.pdf

This component is optional and not mounted in all configurations. Please contact sales to get more information.

9 Electrical Characteristic

9.1 Absolute maximum ratings

Description	Min	Max	Unit
I/O Voltage range for 1.8V IO pins	-0.3	2.1	V
I/O Voltage range for 3.3V IO pins	-0.3	3.6	V
Voltage on any IO with VIN off		0,3	V
I/O Voltage range for ADC pins	-0.1	2.1	V
USB_DEV_VBUS (USB OTG2.0)	-0.3	5.5	V
Maximum output current 3.3V		20	mA

Table 22: Absolute Maximum Ratings

9.2 DC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIN	efus™MX8MP input supply voltage	4.5	5	5.5	V
I_{IN}	Input Current			1.0	A
VBAT	RTC Power Supply	2.2	3.0	3.45	V
P_{VBAT}	Power Consumption @85°C		0.22	0.6	µA
USB_DEV_VBUS	USB supply voltage	4.4	5.0	5.5	V
I_{VBUS}	USB supply current		100		mA
V_{ih}	High Level Input Voltage	0.7*OVDD	OVDD		V
V_{il}	Low Level Input Voltage	0	0.3*OVDD		V
I_o	Output current IOs		5.0		mA

Table 23: DC Electrical Characteristics

10 Thermal Specification

The described Embedded Module is a high performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors like housing, power consumption, heat spreader, airflow and many others.

To keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
  To reduce heat, the CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS), as well as “Thermal throttling” by an integrated temperature sensor. The integrated sensor measures the temperature of the CPU die and lowers CPU clock or shut down CPU if needed.
  DVFS lowers CPU clock and voltage in accordance with the performance needed from the application.
  For optimal use of DVFS, modify your software to only use peak performance for short times.
- The housing has big influence on the heat dissipation. There are many points to analyze:
  - Is there the option of dissipating heat to the housing?
  - Is there a possibility that the air can circulates in the housing?
  - Is an active cooling possible?
- The surrounding temperatures has a big effect to the temperature of the system.
- Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction.

The following table shows nominal thermal specification of the module:

	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40[*2]		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40[*2]		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40[*2]		+105	°C
Junction to Package Top (ΨJT)		0.98		°C/W

Table 24: Thermal Specifications

Note 1: Maximum junction temperature of the CPU is 95°C/105°C. Cooling is a necessary and highly recommended for operations near the limits. See also: *Power Consumption and Cooling*

Note 2: WLAN/BT module is -30°C to +85° only. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13214 (https://www.nxp.com/webapp/Download?colCode=AN13214&location=null)

11 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

12 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decreases your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

13 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

14 Power Consumption and Cooling

Depending on the product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be t.b.d. **Watt**. These values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depending on your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend measuring the power consumption with your application. We see values between max. **t.b.d. Watt to t.b.d. Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling requirement, we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

For the optimal cooling performance, we recommend to use F&S heat spreader.

15 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

16 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

17 Packaging

All F&S ESD-sensitive products will be shipped either in trays or in bags.
These modules ship in trays. One tray can hold 10 boards. An empty tray will be used as top cover.

18 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

19 Appendix

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