Hardware Documentation

FS MX93 OSM™-SF
for HW Revision 1.00

Preliminary

Version 004
(2024-04-04)

Elektronik Systeme

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About This Document

This document describes how to use the FS MX93 OSM™-SF board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Note:
Please use our schematic review service!

FS MX93 OSM uses pre series NXP CPU and the module itself is under development.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
01.10.2023	001	All		-	Initial Version	HF
26.01.2023	002	All	A	2	Added Heat spreader	TM
28.02.2024	003	All	M	3.1, 4.10	Correct AB7 and AB8	MW
02.04.2024	004	All	M M	2 2.1, 2.1.2	add information regarding edge overhang mechanical dimensions changed	UK TM

V Version
A,M,R Added, Modified, Removed
Au Author

Table of Contents

1 Block Diagram

The picture below shows all interfaces that are compatible with the OSM standard. The maximum number of interfaces varies.

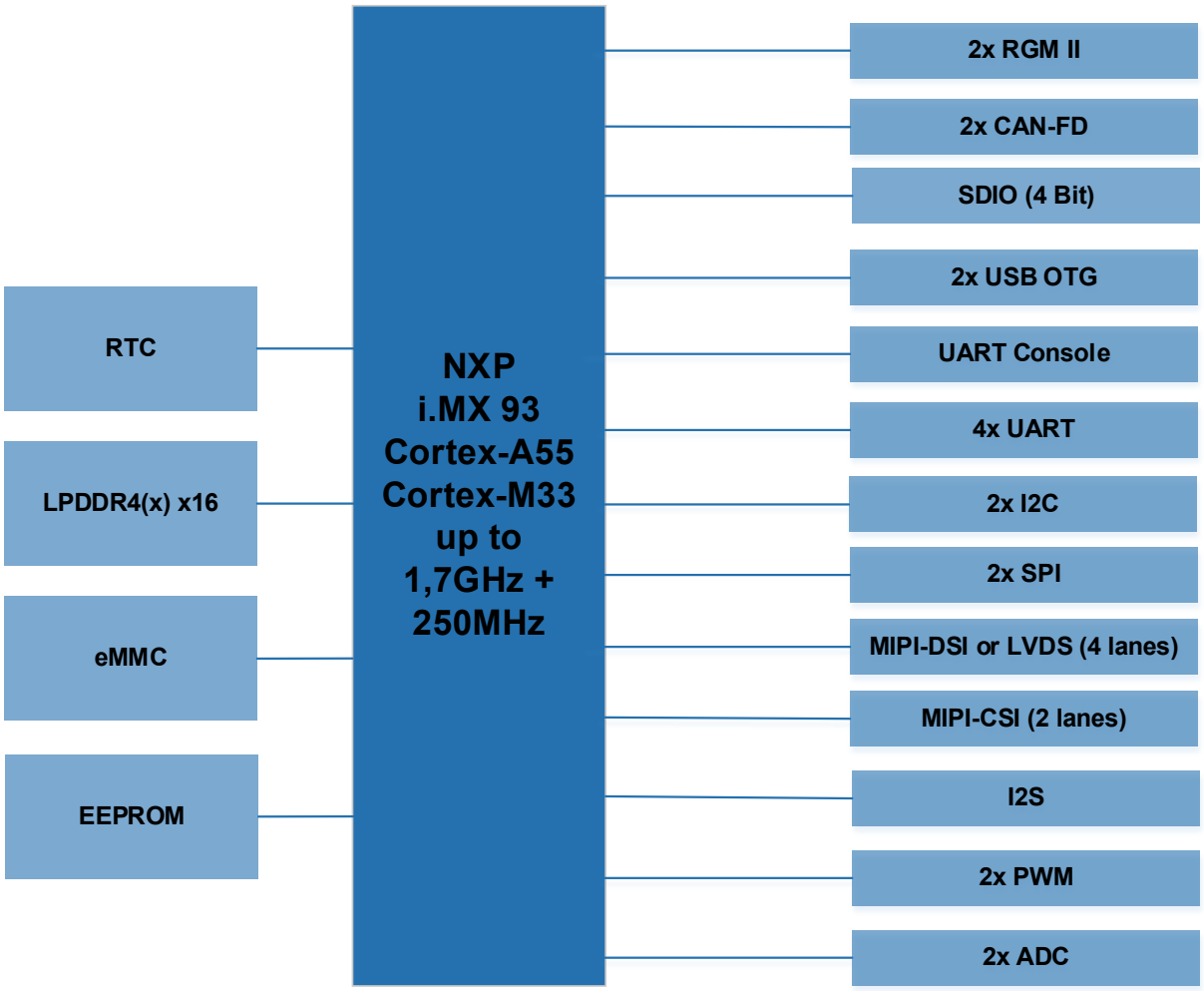
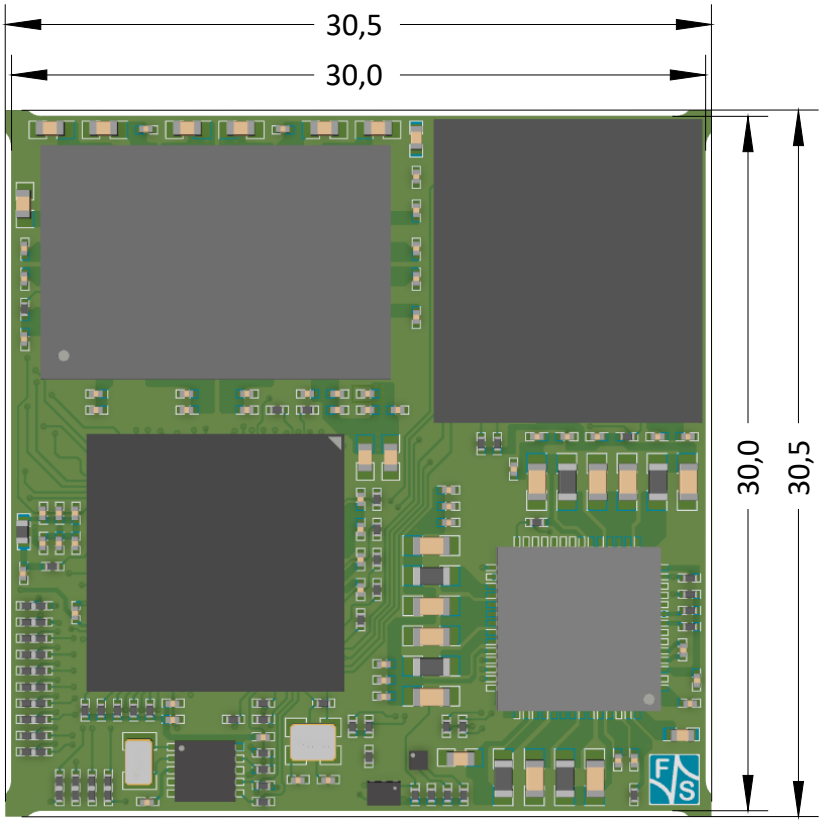


Figure 1: Block diagram

2 Mechanical Dimensions

This OSM module uses single side assembly. So, no cut-out is required on the carrier board. Due to the production process, the modules have an edge overhang which needs to be considered in the design.



all dimensions are in mm

Figure 2: Mechanical Dimensions

Note: Samples may have an overhang, slightly greater than specified above.

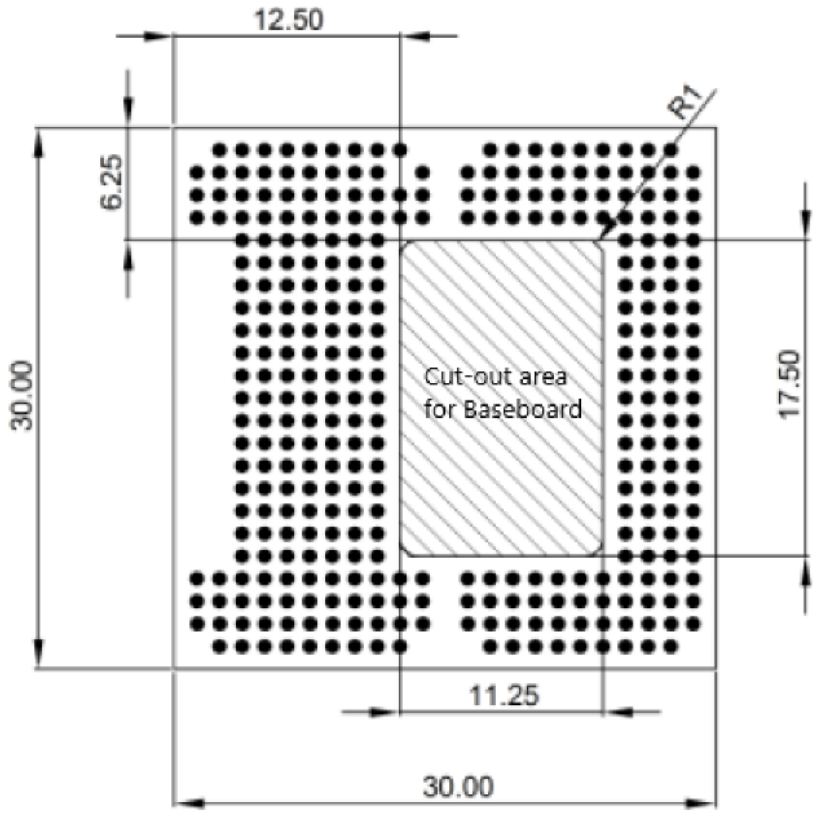


Figure 3: Mechanical Dimensions Bot + cut out area
No Cut-out area is needed for F&S OSM Modules!

Dimensions	Description
Size	30mm x 30mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 1.5mm
Height of the parts on the bottom side	no parts on bottom side
Weight	Max. 12gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of the spreader is **MHS.OSM.1** and can be ordered via F&S web shop. For more information see documentation for MHS.OSM.1.

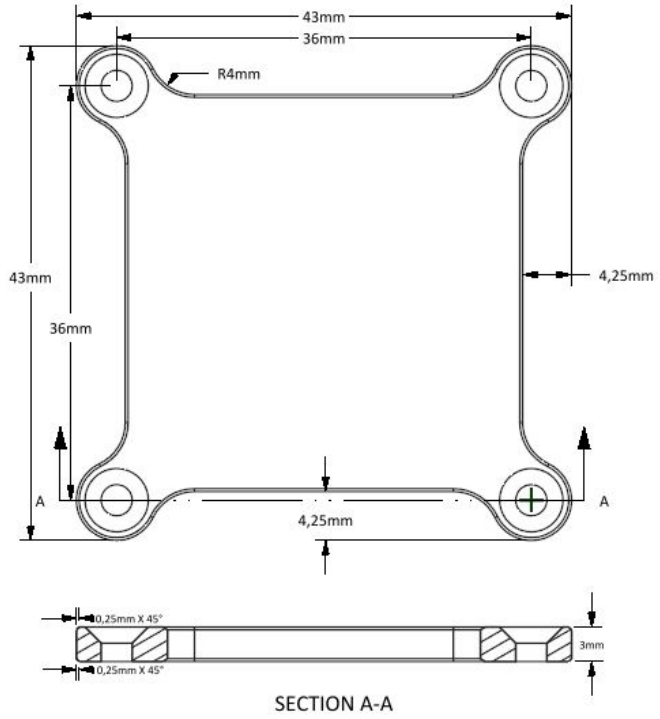


Figure 4: Heat Spreader Mechanical Dimensions

2.1.1 Recommended Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.34**.
This part is in F&S stock and can be ordered via F&S web shop.
The stack height of the spacer is 3.0mm. If a different stack height is needed, another spacer should be chosen. In this case also the thermal interface material must be adapted.

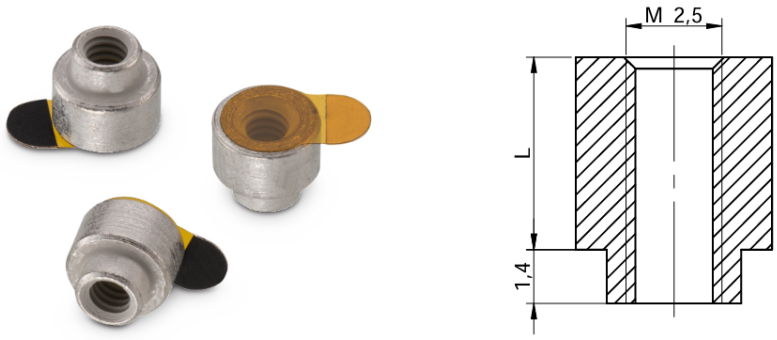


Figure 5: Recommended SMT Steel Spacer

2.1.2 Recommended Land Pattern

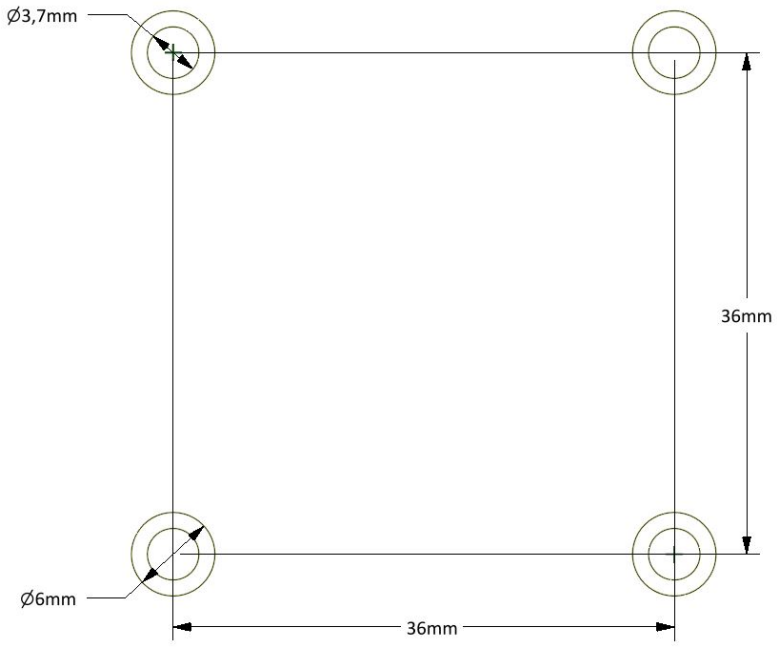


Figure 6: SMT Spacer Recommended Land Pattern

2.1.3 Stencil Suggestion

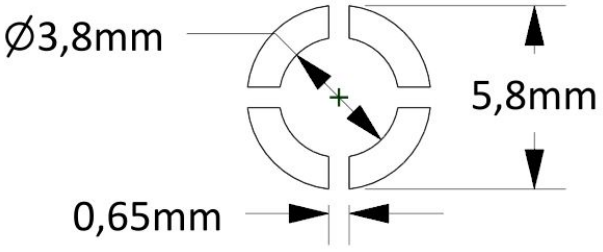


Figure 7: SMT Spacer Stencil Suggestion

3 Interface and Signal Description

3.1 Contact Grid

The FS MX93 OSM™-SF has to be soldered directly on the carrier board.

The FS MX93 OSM™-SF is using Fused Tin Grid Array (FTGA) for connecting the module PCB to the baseboard PCB.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
M18	ADC_0	ADC_IN0	I	1V8	Analog to digital converter.
N18	ADC_1	ADC_IN1	I	1V8	Analog to digital converter.
U19	BOOT_SEL0#		I	1V8	boot medium is choice of vendor
C2	CAM_MCK	CCM_CLKO1	O	1V8	
G3	CAM_PWR/ GPIO_C_6	CCM_CLKO2	I/O	1V8	
G4	CAM_RST#/ GPIO_C_7	CCM_CLKO3	I/O	1V8	
AB17	CAN_A_RX	PDM_BIT_STREAM 0	I	1V8	
AC17	CAN_A_TX	PDM_CLK	O	1V8	
AB19	CAN_B_RX	JTAG_TDO			This pin is shared with JTAG_TDO. Don't connect JTAG and CAN_B at the same time.
AC19	CAN_B_TX	JTAG_TDI	O	1V8	This pin is shared with JTAG_TDI. Don't connect JTAG and CAN_B at the same time.
V17	CARRIER_PWR_EN	SAI1_TXFS	O	1V8	10k pull-down, carrier board circuits should not be powered up until module asserts signal
B3	CSI_CLOCK_N	MIPI_CSI1_CLK_N			
B4	CSI_CLOCK_P	MIPI_CSI1_CLK_P			
C1	CSI_DATA0_N	MIPI_CSI1_D0_N			
B1	CSI_DATA0_P	MIPI_CSI1_D0_P			
A2	CSI_DATA1_N	MIPI_CSI1_D1_N			
A3	CSI_DATA1_P	MIPI_CSI1_D1_P			
AB8	DSI_CLOCK_N	MIPI_DSI_CLK_N/LVDS_CLK_N			soldering option, MIPI-DSi or LVDS
AB7	DSI_CLOCK_P	MIPI_DSI_CLK_P/LVDS_CLK_P			soldering option, MIPI-DSi or LVDS
AB11	DSI_DATA0_N	MIPI_DSI_D0_N/LVDS_D0_N			soldering option, MIPI-DSi or LVDS
AB10	DSI_DATA0_P	MIPI_DSI_D0_P/LVDS_D0_P			soldering option, MIPI-DSi or LVDS
AC9	DSI_DATA1_N	MIPI_DSI_D1_N/LVDS_D1_N			soldering option, MIPI-DSi or LVDS
AC8	DSI_DATA1_P	MIPI_DSI_D1_P/LVDS_D1_P			soldering option, MIPI-DSi or LVDS
AC6	DSI_DATA2_N	MIPI_DSI_D2_N/LVDS_D2_N			soldering option, MIPI-DSi or LVDS

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AC5	DSI_DATA2_P	MIPI_DSI_D2_P/LVDS_D2_P			soldering option, MIPI-DSi or LVDS
AB5	DSI_DATA3_N	MIPI_DSI_D3_N/LVDS_D3_N			soldering option, MIPI-DSi or LVDS
AB4	DSI_DATA3_P	MIPI_DSI_D3_P/LVDS_D3_P			soldering option, MIPI-DSi or LVDS
AA3	DSI_TE	CCM_CLKO4	I	1V8	
R15	ETH_A_(R)(G)MII	ENET1_RXC	I	1V8	
M15	ETH_A_(R)(G)MII	ENET1_RX_CTL	I	1V8	
N15	ETH_A_(R)(G)MII	ENET1_RD2	I	1V8	
P15	ETH_A_(R)(G)MII	ENET1_RD3	I	1V8	
J15	ETH_A_(R)(G)MII	ENET1_TXC	O	1V8	
K16	ETH_A_(R)(G)MII	ENET1_TX_CTL	O	1V8	
K15	ETH_A_(S)(R)(G)	ENET1_RD0	I	1V8	
L15	ETH_A_(S)(R)(G)	ENET1_RD1	I	1V8	
H15	ETH_A_(S)(R)(G)	ENET1_TD0	O	1V8	
G15	ETH_A_(S)(R)(G)	ENET1_TD1	O	1V8	
H16	ETH_A_(S)(R)(G)	ENET1_TD2	O	1V8	
G16	ETH_A_(S)(R)(G)	ENET1_TD3	O	1V8	
P1	ETH_B_(R)(G)MII	ENET2_RXC	I	1V8	
L1	ETH_B_(R)(G)MII	ENET2_RX_CTL	I	1V8	
M1	ETH_B_(R)(G)MII	ENET2_RD2	O	1V8	
N1	ETH_B_(R)(G)MII	ENET2_RD3	O	1V8	
H1	ETH_B_(R)(G)MII	ENET2_TXC	O	1V8	
J2	ETH_B_(R)(G)MII	ENET2_TX_CTL	O	1V8	
J1	ETH_B_(S)(R)(G)	ENET2_RD0	I	1V8	
K1	ETH_B_(S)(R)(G)	ENET2_RD1	I	1V8	
G1	ETH_B_(S)(R)(G)	ENET2_TD0	O	1V8	
F1	ETH_B_(S)(R)(G)	ENET2_TD1	O	1V8	
G2	ETH_B_(S)(R)(G)	ENET2_TD2	O	1V8	
F2	ETH_B_(S)(R)(G)	ENET2_TD3	O	1V8	
M17	ETH_IOPWR		O	1V8	Output IO voltage for Ethernet on carrier board.
T16	ETH_MDC	ENET1_MDC	O	1V8	
T15	ETH_MDIO	ENET1_MDIO	I/O	1V8	
T17	FORCE_RECOVERY#		I	1V8	If LOW, OSM enters recovery mode
A10	GND		PWR	GND	
A4	GND		PWR	GND	
A7	GND		PWR	GND	
AA1	GND		PWR	GND	
AA10	GND		PWR	GND	
AA11	GND		PWR	GND	
AA14	GND		PWR	GND	
AA17	GND		PWR	GND	
AA19	GND		PWR	GND	

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AA22	GND		PWR	GND	
AA4	GND		PWR	GND	
AA7	GND		PWR	GND	
AA8	GND		PWR	GND	
AB15	GND		PWR	GND	
AB21	GND		PWR	GND	
AB3	GND		PWR	GND	
AB6	GND		PWR	GND	
AB9	GND		PWR	GND	
AC4	GND		PWR	GND	
AC7	GND		PWR	GND	
B2	GND		PWR	GND	
B5	GND		PWR	GND	
B8	GND		PWR	GND	
B9	GND		PWR	GND	
C11	GND		PWR	GND	
D1	GND		PWR	GND	
D18	GND		PWR	GND	
D5	GND		PWR	GND	
D8	GND		PWR	GND	
E15	GND		PWR	GND	
E2	GND		PWR	GND	
E21	GND		PWR	GND	
F16	GND		PWR	GND	
F20	GND		PWR	GND	
H2	GND		PWR	GND	
H4	GND		PWR	GND	
J16	GND		PWR	GND	
J20	GND		PWR	GND	
L18	GND		PWR	GND	
L2	GND		PWR	GND	
L4	GND		PWR	GND	
M16	GND		PWR	GND	
M20	GND		PWR	GND	
P18	GND		PWR	GND	
P2	GND		PWR	GND	
P4	GND		PWR	GND	
R1	GND		PWR	GND	
R16	GND		PWR	GND	
R20	GND		PWR	GND	
U2	GND		PWR	GND	
U4	GND		PWR	GND	
V1	GND		PWR	GND	
V16	GND		PWR	GND	

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
V20	GND		PWR	GND	
W3	GND		PWR	GND	
Y18	GND		PWR	GND	
Y2	GND		PWR	GND	
AC10	GND		PWR	GND	
D17	GPIO_A_0	JTAG_TCK	I/O	1V8	This pin is shared with DAP_TCLK_SWCLK. Don't connect JTAG and GPIO_A_0 at the same time.
E17	GPIO_A_1	JTAG_TMS	I/O	1V8	This pin is shared with DAP_TMS_SWDIO. Don't connect JTAG and GPIO_A_1 at the same time.
F17	GPIO_A_2	NC/GPIO_IO15	I/O	1V8	soldering option, UART_C_RX or GPIO_A_2
G17	GPIO_A_3	NC/GPIO_IO14	I/O	1V8	soldering option, UART_C_TX or GPIO_A_3
H17	GPIO_A_4	NC/GPIO_IO13	I/O	1V8	soldering option, UART_D_RX or GPIO_A_4
J17	GPIO_A_5	NC/GPIO_IO12	/IO	1V8	soldering option, UART_D_TX or GPIO_A_5
K17	GPIO_A_6/ SPI_A_CS1#	ENET2_MDC	O	1V8	
L17	GPIO_A_7/ SPI_B_CS1#	GPIO_IO24	O	1V8	
F3	GPIO_C_4/ DISP_VDD_EN	ENET2_MDIO	O	1V8	
F4	GPIO_C_5/ DISP_BL_EN	GPIO_IO07	O	1V8	
AA15	I2C_A_SCL	I2C1_SCL	I/O	1V8	2k49 pull-up, OD
AA16	I2C_A_SDA	I2C1_SDA	I/O	1V8	2k49 pull-up, OD
AA20	I2C_B_SCL	GPIO_IO29	I/O	1V8	2k49 pull-up, OD
AA21	I2C_B_SDA	GPIO_IO28	I/O	1V8	2k49 pull-up, OD
C4	I2C_CAM_SCL	GPIO_IO23	I/O	1V8	2k49 pull-up, OD
C3	I2C_CAM_SDA	GPIO_IO22	I/O	1V8	2k49 pull-up, OD
V21	I2S_A_DATA_IN	GPIO_IO20	I	1V8	
W21	I2S_A_DATA_OUT	GPIO_IO21	O	1V8	
W20	I2S_BITCLK	GPIO_IO16	O	1V8	
W18	I2S_LRCLK	GPIO_IO26	O	1V8	
V18	I2S_MCLK	GPIO_IO17	O	1V8	
N17	JTAG_TCK (SWCLK)	DAP_TCLK_SWCLK		1V8	This pin is shared with GPIO_A_0. Don't connect JTAG and GPIO_A_0 at the same time.
P17	JTAG_TDI	DAP_TDI		1V8	This pin is shared with CAN_B_TX. Don't connect JTAG and CAN_B at the same time.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
R17	JTAG_TDO (SWO)	DAP_TDO_TRA-CESW		1V8	This pin is shared with CAN_B_RX. Don't connect JTAG and CAN_B at the same time.
N19	JTAG_TMS(SWDIO)	DAP_TMS_SWDIO		1V8	This pin is shared with GPIO_A_1. Don't connect JTAG and GPIO_A_1 at the same time.
E18	PWM_0/ DISP_BL_PWM	GPIO_IO06	O	1V8	
F18	PWM_1	GPIO_IO04	O	1V8	
G18	PWM_2	GPIO_IO05	O	1V8	
AA9	PWR_BTN#	ONOFF	I	1V8	100k pull-up, active low
W17	RTC_PWR		I	3V0	power supply for RTC
J21	SDIO_A_CD#	SD2_CD_B	I	SDIO_A_IOPWR	10k pull-up
F21	SDIO_A_CLK	SD2_CLK	O	SDIO_A_IOPWR	
E20	SDIO_A_CMD	SD2_CMD	I/O	SDIO_A_IOPWR	
G20	SDIO_A_D0	SD2_DATA0	I/O	SDIO_A_IOPWR	
G21	SDIO_A_D1	SD2_DATA1	I/O	SDIO_A_IOPWR	
H20	SDIO_A_D2	SD2_DATA2	I/O	SDIO_A_IOPWR	
H21	SDIO_A_D3	SD2_DATA3	I/O	SDIO_A_IOPWR	
C20	SDIO_A_IOPWR	NVCC_SD2	O	1V8 or 3V3	
D21	SDIO_A_PWR_EN	SD2_RESET_B	O	SDIO_A_IOPWR	
D20	SDIO_A_WP	GPIO_IO25	I	SDIO_A_IOPWR	
W15	SPI_A_HOLD# / QSPI_IO3	SD3_DATA3	I/O	1V8	
W16	SPI_A_WP# / QSPI_IO2	SD3_DATA2	I/O	1V8	
Y15	SPI_A_CS0#	SD3_CMD	O	1V8	
U16	SPI_A_SCK	SD3_CLK	O	1V8	
U15	SPI_A_SDI / QSPI_IO0	SD3_DATA0	I/O	1V8	
V15	SPI_A_SDO / QSPI_IO1	SD3_DATA1	I/O	1V8	
AA23	SPI_B_CS0#	GPIO_IO08	O	1V8	
Y21	SPI_B_SCK	GPIO_IO11	O	1V8	
Y22	SPI_B_SDI	GPIO_IO09	I	1V8	
Y23	SPI_B_SDO	GPIO_IO10	O	1V8	
U17	SYS_RST#	PMIC_RST_B	I	1V8	100k pull-up, active low
C14	UART_A_CTS	SAI1_TXC	I	1V8	
C13	UART_A_RTS	SAI1_TXD0	O	1V8	10k pull-down

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
A14	UART_A_RX	UART2_RXD	I	1V8	
B13	UART_A_TX	UART2_TXD	O	1V8	10k pull-down
D16	UART_B_CTS	GPIO_IO02	I	1V8	
D15	UART_B_RTS	GPIO_IO03	O	1V8	
D14	UART_B_RX	GPIO_IO01	I	1V8	
D13	UART_B_TX	GPIO_IO00	O	1V8	
A22	UART_C_RX	NC/GPIO_IO15	I	1V8	soldering option, UART_C_RX or GPIO_A_2
B23	UART_C_TX	NC/GPIO_IO14	O	1V8	soldering option, UART_C_TX or GPIO_A_3
D22	UART_CON_RX	UART1_RXD	I	1V8	
D23	UART_CON_TX	UART1_TXD	O	1V8	10k pull-down
C22	UART_D_RX	NC/GPIO_IO13	I	1V8	soldering option, UART_D_RX or GPIO_A_4
C23	UART_D_TX	NC/GPIO_IO12	O	1V8	soldering option, UART_D_TX or GPIO_A_5
AB13	USB_A_D_N	USB1_D_N			
AC14	USB_A_D_P	USB1_D_P			
AC16	USB_A_EN	GPIO_IO19	O	1V8	
AB14	USB_A_ID	USB1_ID	I	1V8	10k pull-up
AC15	USB_A_OC#	PDM_BIT_STREAM 1	I	1V8	10k pull-up
AB16	USB_A_VBUS		I	5V0	
AB23	USB_B_D_N	USB2_D_N			
AC22	USB_B_D_P	USB2_D_P			
AC20	USB_B_EN	GPIO_IO18	O	1V8	
AB22	USB_B_ID	USB2_ID	I	1V8	10k pull-up
AC21	USB_B_OC#	GPIO_IO27	I	1V8	10k pull-up
AB20	USB_B_VBUS		I	5V0	
M19	VCC_2_TEST		O	1V8	Test ouptut from 1V8 regulator.
Y16	VCC_3_TEST	VDD_USB_3P3	O	3V3	Test ouptut from 3V3 regulator.
Y20	VCC_4_TEST	NVCC_BBSM_1P8	O	1V8	Test ouptut from 1V8 regulator.
Y3	VCC_5_TEST	VDDQ_DDR	O	1V1	Test output DRAM supply voltage 1V1.
C5	VCC_6_TEST	VDD2_DDR	O	1V1	Test output from 1V1 regulator.
Y10	VCC_IN_5V_Y10		I	5V0	
Y11	VCC_IN_5V_Y11		I	5V0	
Y17	VCC_IN_5V_Y17		I	5V0	
Y8	VCC_IN_5V_Y8		I	5V0	
Y9	VCC_IN_5V_Y9		I	5V0	
U18	VCC_OUT_IO		O	1V8	Output IO voltage for peripherals on carrier board.

Table 2: B2B connector

*[1]: The module does not support the RGB-Interface.

*[2]: Please see Chapter 7 for further information about these power & control contacts.

4 Interfaces

4.1 ADC Interface

FS MX93 OSM-SF board with support 2x ADC outputs:

- 12 bit resolution
- 1MS/s

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
M18	ADC_0	ADC_IN0	I	1V8	Analog to digital converter.
N18	ADC_1	ADC_IN1	I	1V8	Analog to digital converter.

Table 3: ADC Interfaces

4.2 USB 2.0 Interfaces

The module supports two USB 2.0 controllers and PHYs. The can be configured as USB host or as USB device.

The 90 Ohm differential pair of USB signals doesn´t need any termination.
For external ports on carrier board ESD and EMV protection is required nearby the USB connectors.
If the USB will be used in Host Mode, contact USB_ID must be connected to GND. Otherwise it must be directly connected to the USB connector.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AB13	USB_A_D_N	USB1_D_N			
AC14	USB_A_D_P	USB1_D_P			
AC16	USB_A_EN	GPIO_IO19	O	1V8	
AB14	USB_A_ID	USB1_ID	I	1V8	10k pull-up
AC15	USB_A_OC#	PDM_BIT_STREAM1	I	1V8	10k pull-up
AB16	USB_A_VBUS		I	5V0	
AB23	USB_B_D_N	USB2_D_N			
AC22	USB_B_D_P	USB2_D_P			
AC20	USB_B_EN	GPIO_IO18	O	1V8	
AB22	USB_B_ID	USB2_ID	I	1V8	10k pull-up
AC21	USB_B_OC#	GPIO_IO27	I	1V8	10k pull-up
AB20	USB_B_VBUS		I	5V0	

Table 4: USB A/B Interface Connections

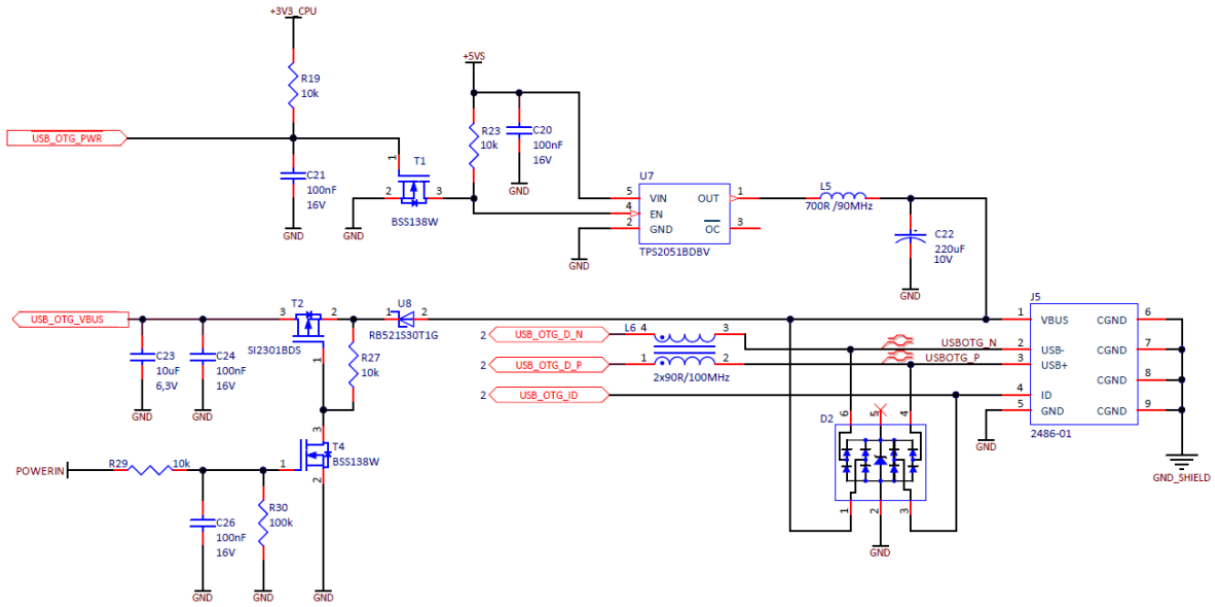


Figure 8: USB OTG example connection on carrier board

4.3 SD/MMC Interface

The module supports one SD/MMC/eMMC/SDHC interface with 4 data bits.

For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The supply voltage of SD_A (SD_A_VCC) is switched by software between 1.8V and 3.3V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
C20	SDIO_A_IOPWR	NVCC_SD2	O	1V8 or 3V3	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA
J21	SDIO_A_CD#	SD2_CD_B	I	SDIO_A_IOPWR	Active low, card detect, onboard pull-up 10k
F21	SDIO_A_CLK	SD2_CLK	O	SDIO_A_IOPWR	
E20	SDIO_A_CMD	SD2_CMD	I/O	SDIO_A_IOPWR	
G20	SDIO_A_D0	SD2_DATA0	I/O	SDIO_A_IOPWR	
G21	SDIO_A_D1	SD2_DATA1	I/O	SDIO_A_IOPWR	
H20	SDIO_A_D2	SD2_DATA2	I/O	SDIO_A_IOPWR	
H21	SDIO_A_D3	SD2_DATA3	I/O	SDIO_A_IOPWR	
D21	SDIO_A_PWR_EN	SD2_RESET_B	O	SDIO_A_IOPWR	
D20	SDIO_A_WP	GPIO_IO25	I	SDIO_A_IOPWR	If not used on carrier board, pull-down pin or disable in software

Table 5: SD Card A Interface

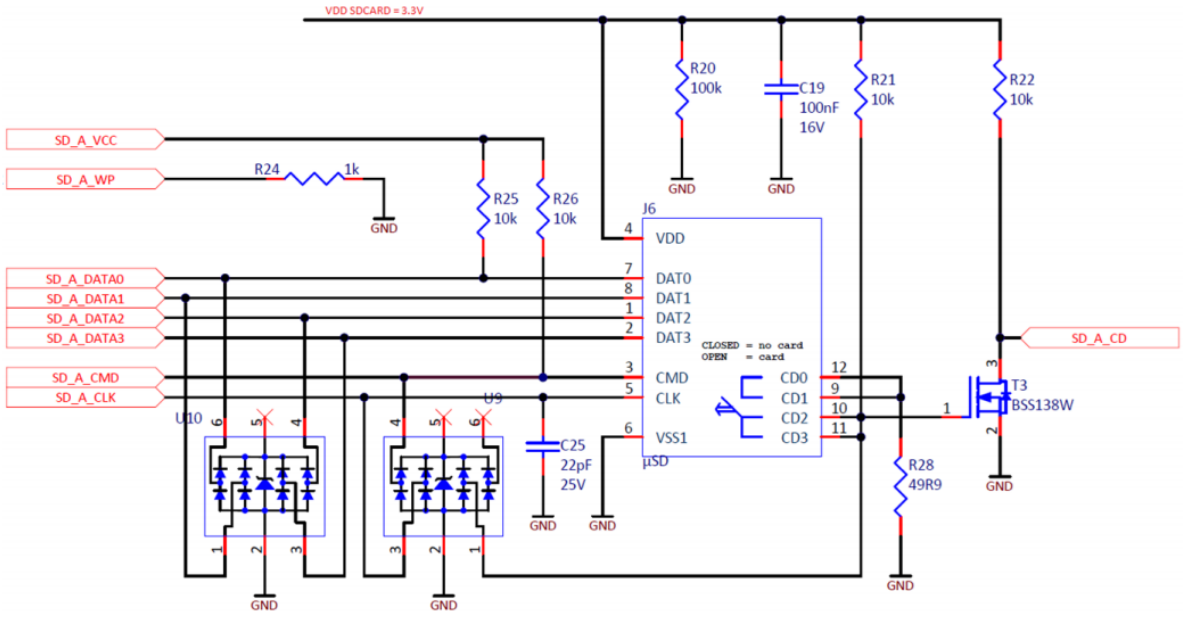


Figure 9: SD Card Connector example connection on carrier board

4.4 QSPI Interface

T.B.D.

4.5 SPI Interface

The module supports two SPIs (Serial Peripheral Interface). All signals are 1.8V compliant. Devices on carrier board with other voltage levels need a level shifter.
Signals don´t have Pull-Ups on module.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
W15	SPI_A_/HOLD_(IO	SD3_DATA3	I/O	1V8	
W16	SPI_A_/WP_(IO2)	SD3_DATA2	I/O	1V8	
Y15	SPI_A_CS0#	SD3_CMD	O	1V8	
U16	SPI_A_SCK	SD3_CLK	O	1V8	
U15	SPI_A_SDI_(IO0)	SD3_DATA0	I/O	1V8	
V15	SPI_A_SDO_(IO1)	SD3_DATA1	I/O	1V8	
AA23	SPI_B_CS0#	GPIO_IO08	O	1V8	
Y21	SPI_B_SCK	GPIO_IO11	O	1V8	
Y22	SPI_B_SDI	GPIO_IO09	I	1V8	
Y23	SPI_B_SDO	GPIO_IO10	O	1V8	

Table 6: SPI Interface

4.6 I2C

The modules supports up to 3 I2C Interfaces. Devices on baseboard with other voltage need a level shifter.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AA15	I2C_A_SCL	I2C1_SCL	I/O	1V8	2k49 pull-up, OD
AA16	I2C_A_SDA	I2C1_SDA	I/O	1V8	2k49 pull-up, OD
AA20	I2C_B_SCL	GPIO_IO29	I/O	1V8	2k49 pull-up, OD
AA21	I2C_B_SDA	GPIO_IO28	I/O	1V8	2k49 pull-up, OD
C4	I2C_CAM_SCL/CSI	GPIO_IO23	I/O	1V8	2k49 pull-up, OD
C3	I2C_CAM_SDA/CSI	GPIO_IO22	I/O	1V8	2k49 pull-up, OD

Table 7: I2C Interface

4.7 Serial Interface (UART)

FS MX93 OSM-SF module provides 5 UART channels:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 5 Mbps
- 2x UART with flow control signals RTS and CTS, 3x standard RX and TX.

We recommend to use UART_CON for debugging and service only.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
C14	UART_A_CTS	SAI1_TXC	I	1V8	
C13	UART_A_RTS	SAI1_TXD0	O	1V8	10k pull-down
A14	UART_A_RX	UART2_RXD	I	1V8	
B13	UART_A_TX	UART2_TXD	O	1V8	10k pull-down
D16	UART_B_CTS	GPIO_IO02	I	1V8	
D15	UART_B_RTS	GPIO_IO03	O	1V8	
D14	UART_B_RX	GPIO_IO01	I	1V8	
D13	UART_B_TX	GPIO_IO00	O	1V8	
A22	UART_C_RX	NC/GPIO_IO15	I	1V8	soldering option, UART_C_RX or GPIO_A_0
B23	UART_C_TX	NC/GPIO_IO14	O	1V8	soldering option, UART_C_TX or GPIO_A_1
D22	UART_CON_RX	UART1_RXD	I	1V8	
D23	UART_CON_TX	UART1_TXD	O	1V8	10k pull-down
C22	UART_D_RX	NC/GPIO_IO13	I	1V8	soldering option, UART_D_RX or GPIO_A_2
C23	UART_D_TX	NC/GPIO_IO12	O	1V8	soldering option, UART_D_TX or GPIO_A_3

Table 8: UART Interface Signals

4.8 Ethernet

The FS MX93 OSM-SF supports two 10/100/1000Mbit LAN interface via RGMII signals.

An external Ethernet-PHY (i.e. AR8035-AL1A…) or an external switch (i.e. KSZ9893R…) is required.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
R15	ETH_A_(R)(G)MII	ENET1_RXC	I	1V8	
M15	ETH_A_(R)(G)MII	ENET1_RX_CTL	I	1V8	
N15	ETH_A_(R)(G)MII	ENET1_RD2	I	1V8	
P15	ETH_A_(R)(G)MII	ENET1_RD3	I	1V8	
J15	ETH_A_(R)(G)MII	ENET1_TXC	O	1V8	
K16	ETH_A_(R)(G)MII	ENET1_TX_CTL	O	1V8	
K15	ETH_A_(S)(R)(G)	ENET1_RD0	I	1V8	
L15	ETH_A_(S)(R)(G)	ENET1_RD1	I	1V8	
H15	ETH_A_(S)(R)(G)	ENET1_TD0	O	1V8	
G15	ETH_A_(S)(R)(G)	ENET1_TD1	O	1V8	
H16	ETH_A_(S)(R)(G)	ENET1_TD2	O	1V8	
G16	ETH_A_(S)(R)(G)	ENET1_TD3	O	1V8	
P1	ETH_B_(R)(G)MII	ENET2_RXC	I	1V8	
L1	ETH_B_(R)(G)MII	ENET2_RX_CTL	I	1V8	
M1	ETH_B_(R)(G)MII	ENET2_RD2	O	1V8	
N1	ETH_B_(R)(G)MII	ENET2_RD3	O	1V8	
H1	ETH_B_(R)(G)MII	ENET2_TXC	O	1V8	
J2	ETH_B_(R)(G)MII	ENET2_TX_CTL	O	1V8	
J1	ETH_B_(S)(R)(G)	ENET2_RD0	I	1V8	
K1	ETH_B_(S)(R)(G)	ENET2_RD1	I	1V8	
G1	ETH_B_(S)(R)(G)	ENET2_TD0	O	1V8	
F1	ETH_B_(S)(R)(G)	ENET2_TD1	O	1V8	
G2	ETH_B_(S)(R)(G)	ENET2_TD2	O	1V8	
F2	ETH_B_(S)(R)(G)	ENET2_TD3	O	1V8	
M17	ETH_IOPWR	NVCC_WAKEUP3	O	1V8	
T16	ETH_MDC	ENET1_MDC	O	1V8	
T15	ETH_MDIO	ENET1_MDIO	I/O	1V8	

Table 9: RGMII Interface (no Ethernet PHY)

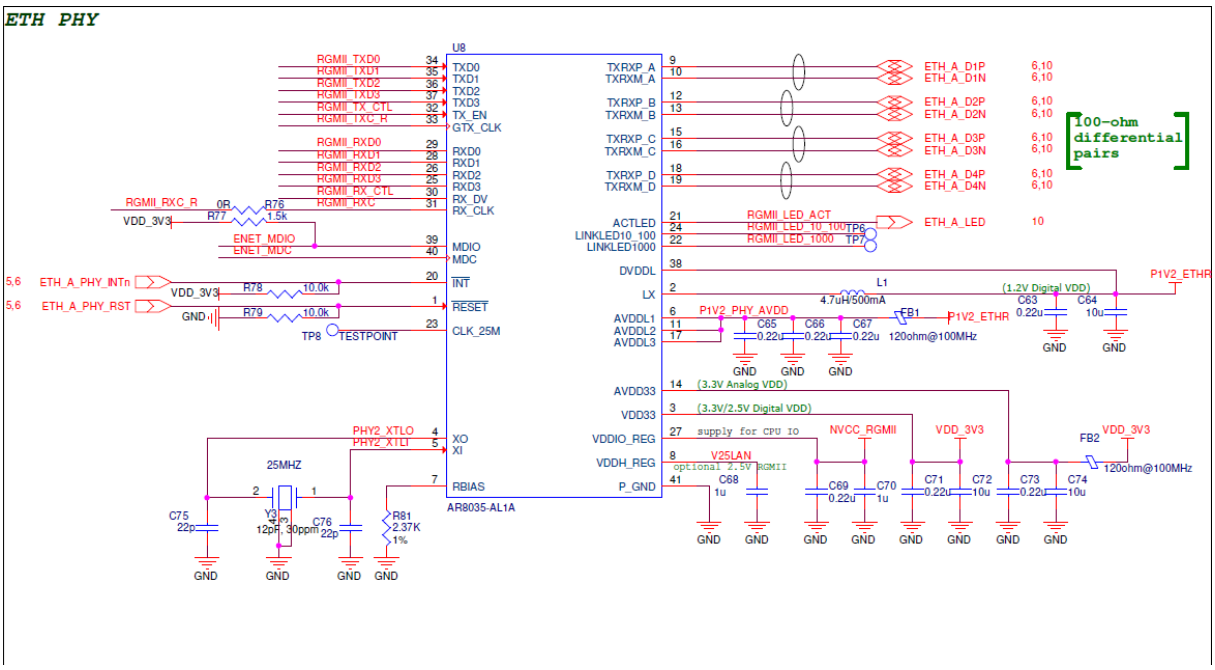


Figure 10 RGMII to Ethernet PHY example

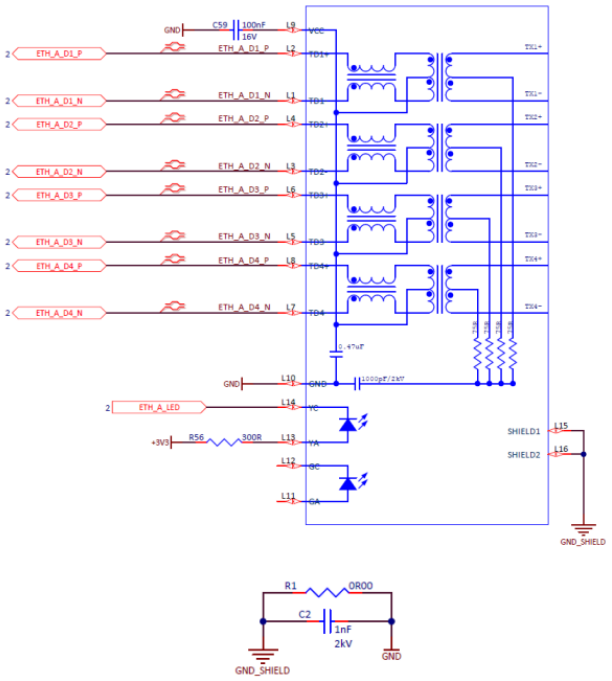


Figure 11 Ethernet PHY to LAN connector example

4.9 Audio (I2S)

The module supports only I2S signals. An external audio codec IC (i.e. SGTL500…) on the carrier board is needed for Audio output.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
V21	I2S_A_DATA_IN	GPIO_IO20	I	1V8	
W21	I2S_A_DATA_OUT	GPIO_IO21	O	1V8	
W20	I2S_BITCLK	GPIO_IO16	O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU act in Slave Mode
W18	I2S_LRCLK	GPIO_IO26	O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
V18	I2S_MCLK	GPIO_IO17	O	1V8	

Table 10: Audio Interface (without Codec)

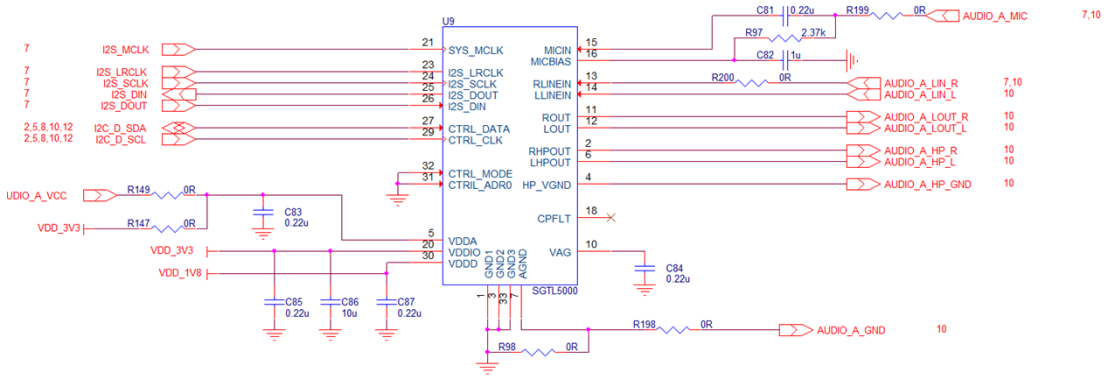


Figure 12 SGTL5000 Codec circuit example for carrier board

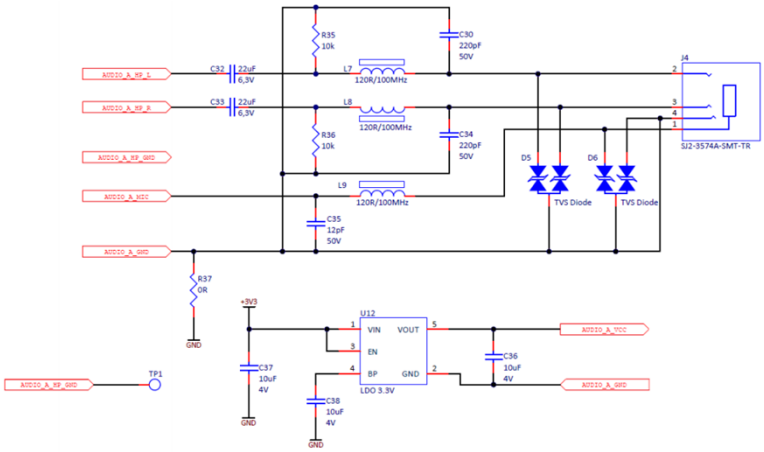


Figure 13 Headphone-Out Mic-In example circuit for carrier board

4.10 MIPI DSI

The module supports one quad lane MIPI DSI interface with following features:

- Support one 4-lane MIPI DSI display with pixels from the LCDIF
- Compliant to MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- The maximum pixel clock is 200 MHz and active pixel rate of 140 Mpixel/s with 24-bit RGB. This includes resolutions such as 1080p60 or 1920x1200p60.
- The maximum data rate per lane is 1.5 Gbps.

The signals can be connected directly to a MIPI compliant display.

The contacts are shared with LVDS interface. **LVDS is a soldering option.**

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AB8	DSI_CLOCK_N	MIPI_DSI_CLK_N/LVDS_CLK_N	O	1.2V/200mV*1	
AB7	DSI_CLOCK_P	MIPI_DSI_CLK_P/LVDS_CLK_P	O	1.2V/200mV*1	
AB11	DSI_DATA0_N	MIPI_DSI_D0_N/LVDS_D0_N	O	1.2V/200mV*1	
AB10	DSI_DATA0_P	MIPI_DSI_D0_P/LVDS_D0_P	O	1.2V/200mV*1	
AC9	DSI_DATA1_N	MIPI_DSI_D1_N/LVDS_D1_N	O	1.2V/200mV*1	
AC8	DSI_DATA1_P	MIPI_DSI_D1_P/LVDS_D1_P	O	1.2V/200mV*1	
AC6	DSI_DATA2_N	MIPI_DSI_D2_N/LVDS_D2_N	O	1.2V/200mV*1	
AC5	DSI_DATA2_P	MIPI_DSI_D2_P/LVDS_D2_P	O	1.2V/200mV*1	
AB5	DSI_DATA3_N	MIPI_DSI_D3_N/LVDS_D3_N	O	1.2V/200mV*1	
AB4	DSI_DATA3_P	MIPI_DSI_D3_P/LVDS_D3_P	O	1.2V/200mV*1	
AA3	DSI_TE	CCM_CLKO4	I	1V8	
F3	DISP_VDD_EN/ GPIO_C_4	ENET2_MDIO	O	1V8	
F4	DISP_BL_EN / GPIO_C_5	GPIO_IO07	O	1V8	
E18	DISP_BL_PWM/ PWM0	GPIO_IO06	O	1V8	

Table 11: MIPI-DSI Interface

*1 : 1.2V in single-ended mode, approx. 200mV in differential mode

4.11 MIPI CSI Interface

The module supports one dual lance MIPI CSI interface with following features:

- Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2
- Support up to 2 Rx data lanes (plus 1 Rx clock lane)
- MIPI CSI-2 supports: – Pixel clock up to 200 MHz (at both nominal and overdrive voltage) – Up to approximately 150 Mpixel/s supported – 80 Mbps to 1.5 Gbps per lane data rate in high speed operation
- Support 10 Mbps data rate in low power operation

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
B3	CSI_CLOCK_N	MIPI_CSI1_CLK_N	I		
B4	CSI_CLOCK_P	MIPI_CSI1_CLK_P	I		
C1	CSI_DATA0_N	MIPI_CSI1_D0_N	I		
B1	CSI_DATA0_P	MIPI_CSI1_D0_P	I		
A2	CSI_DATA1_N	MIPI_CSI1_D1_N	I		
A3	CSI_DATA1_P	MIPI_CSI1_D1_P	I		
C4	I2C_CAM_SCL	GPIO_IO23	I/O	1V8	2k49 pull-up
C3	I2C_CAM_SDA	GPIO_IO22	I/O	1V8	2k49 pull-up
C2	CAM_MCK	CCM_CLKO1	O	1V8	Master clock output
G3	CAM_PWR	CCM_CLKO2	I/O	1V8	Camera power enable. Active high output.
G4	CAM_RST#	CCM_CLKO3	I/O	1V8	Camera reset. Active low output

Table 12: MIPI-CSI Interface

4.12 CAN FD Interface

The FS MX93 OSM-SF supports two CAN FD interfaces.

CAN_B is shared with JTAG interface. Don’t connect JATG and CAN-B at the same time.

Contact	Contact Name	Internal Pad	I/O	Vendor	Remarks
AB17	CAN_A_RX	PDM_BIT_STREAM0	I	1V8	
AC17	CAN_A_TX	PDM_CLK	O	1V8	
AB19	CAN_B_RX	DAP_TDO_TRACESWO			This pin is shared with JTAG_TDO. Don’t connect JTAG and CAN_B at the same time.
AC19	CAN_B_TX	DAP_TCLK_SWCLK	O	1V8	This pin is shared with JTAG_TDI. Don’t connect JTAG and CAN_B at the same time.

Table 13: CAN Interface

4.13 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it´s not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced I/O power is not allowed.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
D17	GPIO_A_0	JTAG_TCK	I/O	1V8	Shared pad: This pin is shared with DAP_TCLK_SWCLK. Don't connect JTAG and GPIO_A_0 at the same time.
E17	GPIO_A_1	JTAG_TMS	I/O	1V8	Shared pad: This pin is shared with DAP_TMS_SWDIO. Don't connect JTAG and GPIO_A_1 at the same time.
F17	GPIO_A_2	NC/GPIO_IO15	I/O	1V8	Soldering option: UART_C_RX or GPIO_A_0
G17	GPIO_A_3	NC/GPIO_IO14	I/O	1V8	Soldering option: UART_C_TX or GPIO_A_1
H17	GPIO_A_4	NC/GPIO_IO13	I/O	1V8	Soldering option: UART_D_RX or GPIO_A_2
J17	GPIO_A_5	NC/GPIO_IO12	/IO	1V8	Soldering option: UART_D_TX or GPIO_A_3
K17	GPIO_A_6/ SPI_A_CS1#	ENET2_MDC	I/O	1V8	Dual function: SPI_A_CS1#
L17	GPIO_A_7/ SPI_B_CS1#	GPIO_IO24	I/O	1V8	Dual function: SPI_A_CS2#
F3	GPIO_C_4/ DISP_VDD_EN	ENET2_MDIO	I/O	1V8	Dual function: DISP_VDD_EN
F4	GPIO_C_5/ DISP_BL_EN	GPIO_IO07	I/O	1V8	Dual function: DISP_BL_EN
G3	GPIO_C_6 / CAM_PWR	CCM_CLKO2	I/O	1V8	Dual function: CAM_PWR
G4	GPIO_C_7 / CAM_RST#	CCM_CLKO3	I/O	1V8	Dual function: CAM_RST#

Table 14: GPIO Interface

4.14 JTAG

JTAG is for debug only.

Leave unconnected, if you don´t use JTAG.

Note:
Leave GPIO_A_4, GPIO_A5, CAN_B_TX and CA_B_RX unconnected, when you use JTAG.

Don´t put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
N17	DAP_TCLK_SWCLK	JTAG_TCK (SWCLK)	I	1V8	This pin is shared with GPIO_A_0. Don’t connect JTAG and GPIO_A_0 at the same time.
P17	DAP_TDI	JTAG_TDI	I	1V8	This pin is shared with CAN_B_TX. Don’t connect JTAG and CAN_B at the same time.
R17	DAP_TDO_TRACESW	JTAG_TDO (SWO)	O	1V8	This pin is shared with CAN_B_RX. Don’t connect JTAG and CAN_B at the same time.
N19	DAP_TMS_SWDIO	JTAG_TMS(SWDIO)	I	1V8	This pin is shared with GPIO_A_1. Don’t connect JTAG and GPIO_A_1 at the same time.

Table 15: JTAG Interface

4.15 PWM

PWMs are free programmable. On a non-powered board it´s not allowed to have a voltage on one of the PWM contacts. Also a higher voltage as the announced I/O power is not allowed.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
E18	PWM_0/ DISP_BL_PWM	GPIO_IO06	O	1V8	Dual function: DISP_BL_PWM
F18	PWM_1	GPIO_IO04	O	1V8	
G18	PWM_2	GPIO_IO05	O	1V8	

Table 16: PWM Interface

4.16 Vendor defined contacts

No vendor defined contacts.

5 eMMC

The module supports eMMC v4.41 or higher from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 RTC

There is an external RTC (PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 Power and Power Control Pins

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
U19	BOOT_SEL0#		I	1V8	If LOW, OSM boots from external QSPI-Flash; Leave open if boot from eMMC
V17	CARRIER_PWR_EN	SAI1_TXFS	O	1V8	10k pull-down, carrier board circuits should not be powered up until module asserts signal
T17	FORCE_RECOVERY#		I	1V8	If LOW, OSM enters recovery mode
A10, A4, A7, AA1, AA10, AA11, AA14, AA17, AA19, AA22, AA4, AA7, AA8, AB15, AB21, AB3, AB6, AB9, AC4, AC7, B2, B5, B8, B9, C11, D1, D18, D5, D8, E15, E2, E21, F16, F20, H2, H4, J16, J20, L18, L2, L4, M16, M20, P18, P2, P4, R1, R16, R20, U2, U4, V1, V16, V20, W3, Y18, Y2, AC10	GND	GND	PWR	GND	Main Power supply Ground input; Connect all GND-Pins on your carrier board.
AA9	PWR_BTN#	ONOFF	I	1V8	Power-button from Carrier board. Carrier to float the line in in-active state. Active low,

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
					level sensitive. 100k pull-up, active low
W17	RTC_PWR		I	3V0	RTC battery input; tie to 3.0V. Please refer chapter 8.2DC Electrical Characteristics.
C20	SDIO_A_IOPWR	NVCC_SD2	O	1V8 or 3V3	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA.
U17	SYS_RST#	PMIC_RST_B	I	1V8	Reset input from carrier board. Carrier drives low to force a Module reset, floats the line otherwise. 100k pull-up, active low.
AB16	USB_A_VBUS		I	5V0	
AB20	USB_B_VBUS		I	5V0	
M19	VCC_2_TEST		O	1V8	Module power voltage test point. Leave open (N.C.)
Y16	VCC_3_TEST		O	3V3	Module power voltage test point. Leave open (N.C.)
Y20	VCC_4_TEST		O	1V8	Module power voltage test point. Leave open (N.C.)
Y3	VCC_5_TEST		O	1V1/0V6	Module power voltage test point. Leave open (N.C.)
C5	VCC_6_TEST		O	1V1	Module power voltage test point. Leave open (N.C.)
Y10	VCC_IN_5V	---	I	5V0	Main Power supply input. Please refer chapter 8.2 DC Electrical Characteristics for more information.
Y11	VCC_IN_5V	---	I	5V0	
Y17	VCC_IN_5V	---	I	5V0	
Y8	VCC_IN_5V	---	I	5V0	
Y9	VCC_IN_5V	---	I	5V0	
U18	VCC_OUT_IO		O	1V8	Output IO voltage for peripherals on carrier board. Maximum current 100mA, leave open if not used.
C6, C7, D6, D7, N2, R18, T17, T18, T19, Y13, Y14, AA2, AA13	RESERVED				Leave these pins floating (N.C.)

Table 17: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test Laboratory. It's possible to use a super-capacitor instead.

VCC_OUT_IO is a 1V8 @100mA output. It´s generated from the internal PMIC and powered from VIN. Can be used as "Enable Signal" for the power regulators on baseboard. Please do not use VCC_OUT_IO as power supply for carrier board.

PWR_BTN# is the reset input for the module. PWR_BTN# only resets the CPU. In the event of a power failure, VCC_IN must be switched off and on to avoid latch-up effects.

The GND contacts which are given in the table above are the power ground contacts for VCC_IN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

SD_A_VCC is switched dynamically by software.

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Typ	Max	Unit
Input Voltage range 3.3V IOs	-0.3	3.3	3.6	V
Input Voltage range 1.8V IOs	-0.3	1.8	2.1	V
Voltage on any IO with VDD_VIN off			0.3	V
USB VBUS	-0.3	5	5.6	V
Maximum power consumption VDD_VBAT at 85°C			0.6	µA
Maximum output current VCC_IO			100	mA

Table 18: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
VCC_VIN	Module main power		2.7	5	5.5	V
RTC_PWR	RTC power		0.9	3	5.5	V
USB1/2_VBUS	USB supply voltage		4.4	5	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_VIN		3.15	3.3	3.45	V
VDD_1V8	1.8V output for power enable on carrier board		1.71	1.8	1.89	V
V_{ih}	High Level Input Voltage		0.7*OVDD		OVDD	V
V_{il}	Low Level Input Voltage		0		0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15			V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA			0.15	V
I_o	Output current IOs 1V8	1.8V			10	mA
I_o	Output current IOs 3V3	3.3V			5	mA
I_{VBAT}	Current consumption VBAT				0.22[*1]	µA

Table 19: DC Electrical Characteristics

[*1] Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Grade Operating Temperature	0		+70	°C
Industrial Grade Operating Temperature	-20		+85	°C
Extended Industrial Grade Operating Temperature	-40		t.b.d	°C
Junction Temperature i.MX93 (C-Temp)	0		+95	°C
Junction Temperature i.MX93 (I-Temp)	-40		+105	°C
Junction Temperature i.MX93 (XI-Temp)	-40		+125	°C
Junction to Package TOP (Ψ_{JT}) – i.MX93*[2]		t.b.d		°C/W

Table 20: Thermal Specification

Note 1: Maximum junction temperature of the CPU is 105°C.
In this case cooling is necessary and highly recommended.
See also: Power consumption and cooling

Please get in touch with our engineers for F&S recommended cooling solutions.

Note 2: *Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN12468* (https://www.nxp.com/docs/en/application-note/AN12468.pdf)

10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. t.b.d **Watt** to t.b.d **Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity:	6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity:	12 months

For longer storage we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %. Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 14: Matrix Code Sticker

18 Appendix

Important Notice

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