Hardware Documentation
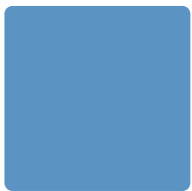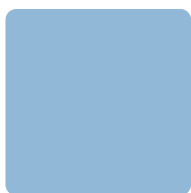
SolderCoreBBHD – Ethernet Adapter
ADP-SC8ULP-ETH
for HW Revision 1.10

preliminary

Version 002
(2023-09-22)

About This Document

This document describes how to use the SolderCoreBBHD – Ethernet Adapter (further named as ethernet adapter) with mechanical and electrical information. The latest version of this document can be found at: http://www.fs-net.de.

This document is written for the variants of the ethernet adapter, listed in the table below.

Related Boards
SolderCoreBBHD – Ethernet Adapter Rev.1.00

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
22.09.23	001	-	-	All	Initial Version	SM
22.09.23	002	-	M	All	Update to Rev 1.10	SM

V	Version
A, M, R	Added, Modified, Removed
Au	Author

Table of Contents

1   Overview

The ethernet adapter (Part No. ADP-SC8ULP-ETH) gives the possibility to add an ethernet port to the SolderCoreBBHD (further called baseboard). It can also be used as an example for other designs.
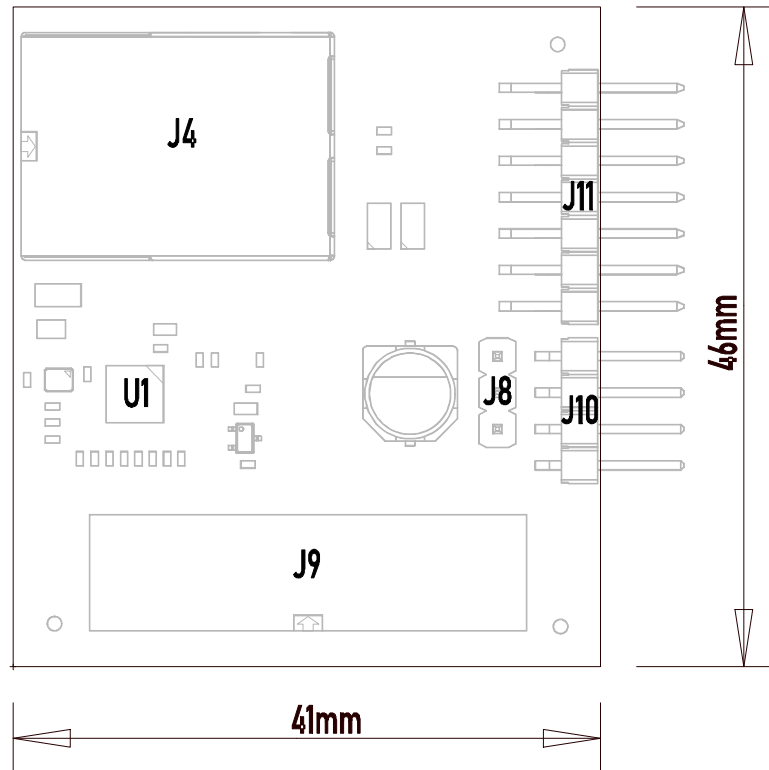

Figure 1: Top side, all dimesions in mm

Ref.	Description	I/O	No. of Pins	Connector Type
J4	100Base-TX Ethernet	I/O	8	RJ45
J8	I/O voltage selection	PWR	3	Pin Header (2.54 mm)
J9	Supply voltage (1.8V, 3.3V)	PWR	4	Pin Header (2.54 mm)
J10	PTE I/O (PTE0…PTCE3)	I/O	24	Socket 90° (2.54 mm)
J11	PTE I/O (PTC0-2, 4-13)	I/O	14	Pin Header (2.54 mm)

Table 1: Connector List and Types

2   Additional Documentation

Due to the fact, that the ethernet adapter is designed to be directly connected to the SolderCoreBBHD baseboard, it is recommended to read the SolderCoreBBHD baseboard documentation previously.

3   Detailed Description

3.1   Connection

The ethernet adapter is mounted on the PTE domain connector of the baseboard, like shown in figure 2. In addition you must wire the power supply from connector J10 to the PTE supply connector on the baseboard.
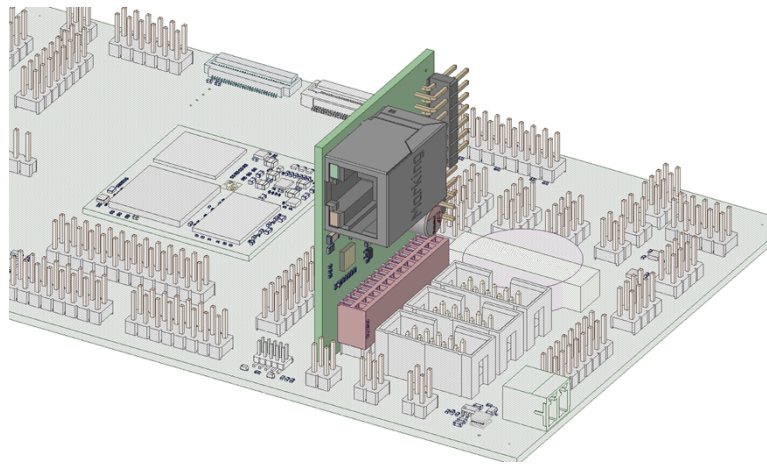

Figure 2: Ethernet adapter mounting position on baseboard

3.2   Supply

The ethernet adapter needs a main supply voltage of 3.3V. The I/Os of the ethernet adapter and the SolderCore8ULP can be driven by 1.8V or 3.3V. The I/O voltage is selected with a jumper on J8, as in figure 5 shown.
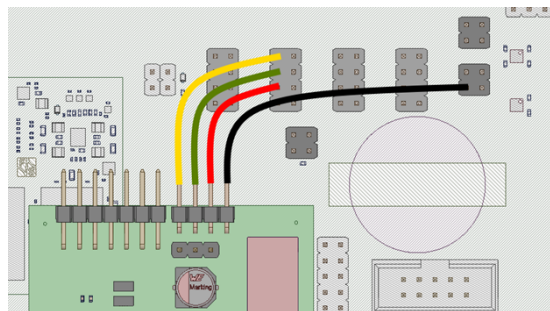
Figure 3: Wiring of power supply

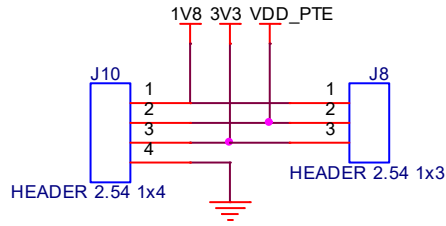| Color	Pin	Signal	Description
yellow	1	1V8	Optional I/O voltage supply
green	2	VDD_PTE	I/O voltage input
red	3	3V3	Main supply
black	4	GND	

Table 2: Connector J10

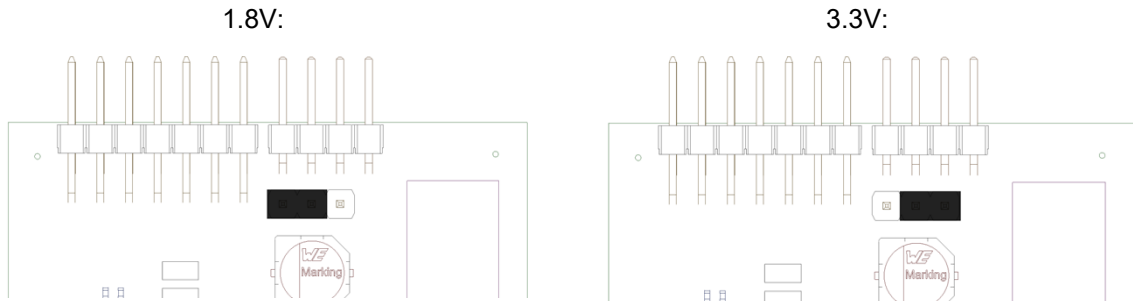*Figure 4: Schematic of J10&J8*

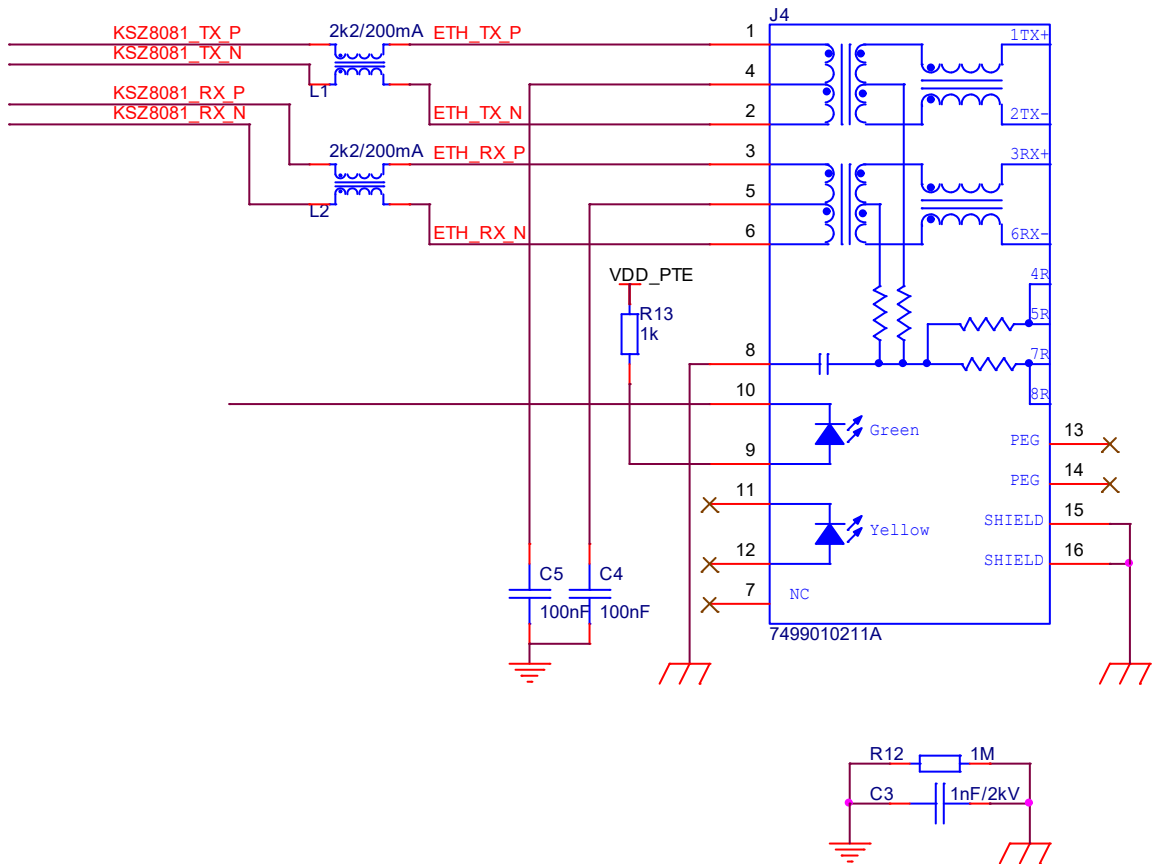*Figure 5: I/O voltage selection*

3.3 Connector RJ45

Figure 6: Schematic of the RJ45 connector

3.4 Connector PTE I/O

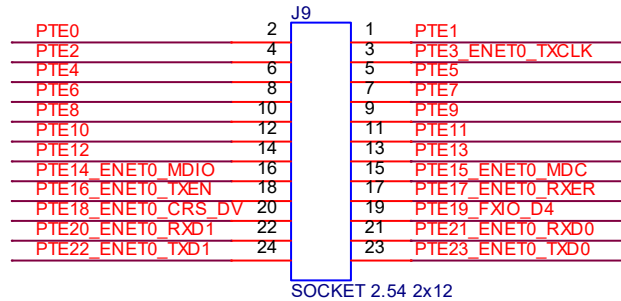The ethernet adapter is connected to the PTE domain of the baseboard. All unused signals are routed to connector J11.

Figure 6: Schematic of connector J9
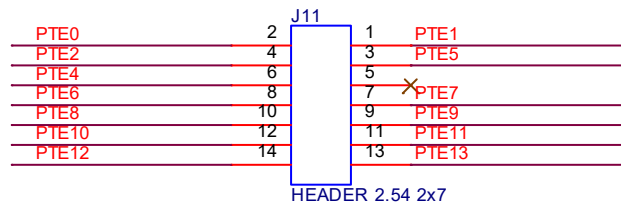
Figure 7: Schematic of connector J11

Signal Name	I/O	Voltage	Description
PTE0			Not used
PTE1			Not used
PTE2	O	1.8V/3.3V	RMII Transmit clock
PTE3	I/O	1.8V/3.3V	I/O D20 (Reset)
PTE4			Not used
PTE5			Not used
PTE6			Not used
PTE7			Not used
PTE8			Not used
PTE9			Not used
PTE10			Not used
PTE11			Not used
PTE12			Not used
PTE13			Not used
PTE14	I/O	1.8V/3.3V	RMII Management data
PTE15	I	1.8V/3.3V	RMII Management clock
PTE16	I	1.8V/3.3V	RMII Transmit enable
PTE17	O	1.8V/3.3V	RMII Receive error
PTE18	O	1.8V/3.3V	RMII Carrier sense/Data valid

PTE19	O	1.8V/3.3V	Reference Clock
PTE20	O	1.8V/3.3V	RMII Receive data bit 1
PTE21	O	1.8V/3.3V	RMII Receive data bit 0
PTE22	I	1.8V/3.3V	RMII Transmit data bit 1
PTE23	I	1.8V/3.3V	RMII Transmit data bit 0

Table 3: PTE I/O connector (J9)pin description

3.5 Ethernet PHY

The ethernet adapter uses the KSZ8081 ethernet PHY from Microchip. The chip supports 10/100Base-TX IEEE 802.3 applications and uses a RMII v1.2 interface to the CPU. The default PHY Address is 0x0.
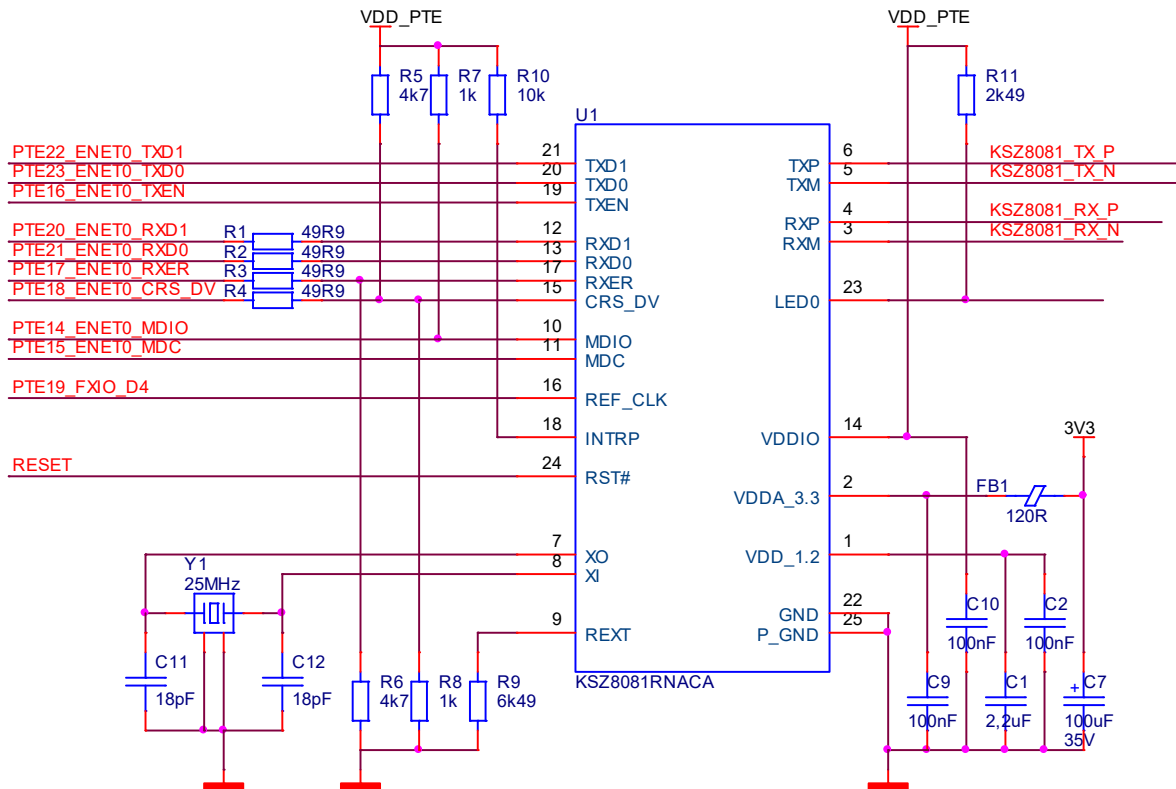

Figure 8: Schematic of the KSZ8081

3.6 Reset

The reset is triggerd on two ways:
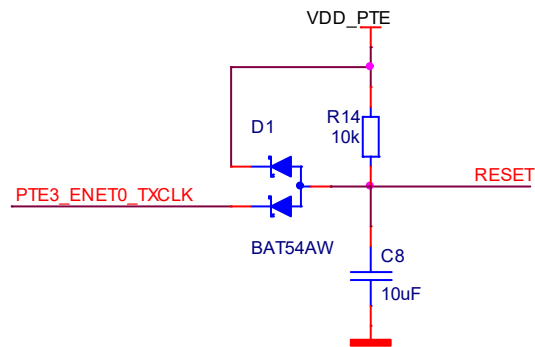1. On power up
2. Via external I/O signal PTE D20

Figure 9: Reset schematic

4 Electrical Characteristics

The ethernet adapter is a part of the SolderCoreBBHD with no intention to connect external voltages. Therefore, please see the SolderCoreBBHD documentation for the electrical characteristics.

5 ESD and EMI Implementation

The connectors do not have any ESD protection. We highly recommend using the adapter board with wires as short as possible.

A helpful guide is available from TI; just search for slva680 at ti.com.

6 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

7 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

8 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

9 Packaging

All F&S ESD-sensitive products will be shipped either in trays or in bags.

10 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 10: Matrix Code Sticker

11 Appendix

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