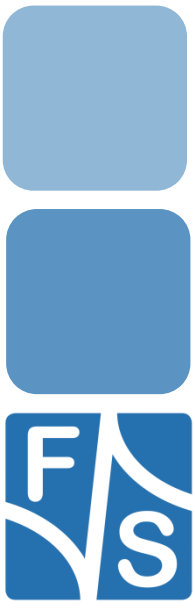
Hardware Documentation

PicoCore™MX8ULP
for HW Revision 1.10

Version 002
(2024-03-05)



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About This Document

This document describes how to use the PicoCore™MX8ULP board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Note:
Please use our schematic review service!

PicoCore™MX8ULP uses pre series NXP CPU and the module itself is under development.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
07.08.2023	001	All		-	Initial Version	HF, MW
05.03.2024	002	All	M	3.1, 4.8.1, 4.12	Change for Revision 1.10	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block Diagram

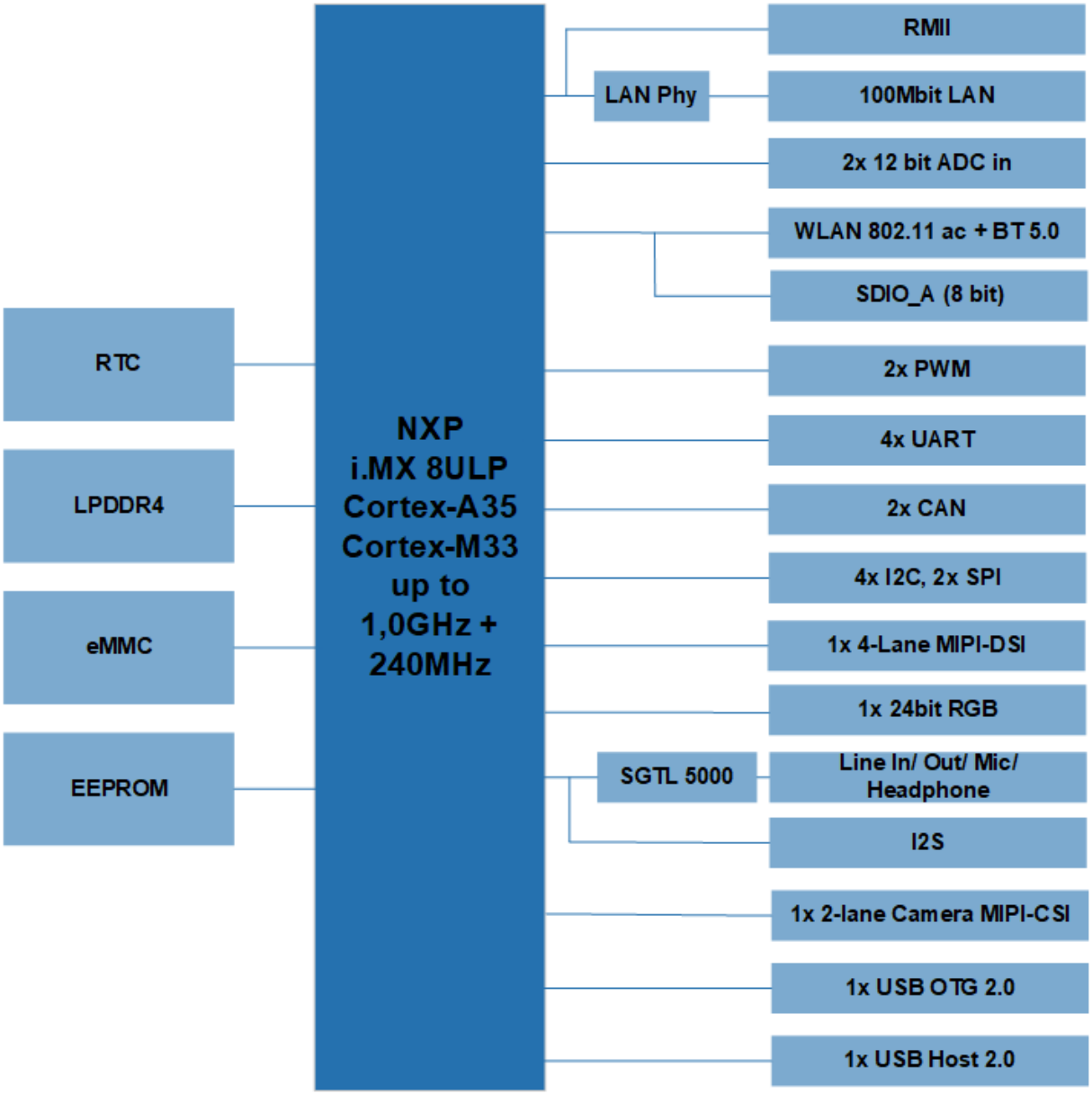

Figure 1: Block Diagram

2 Mechanical Dimension

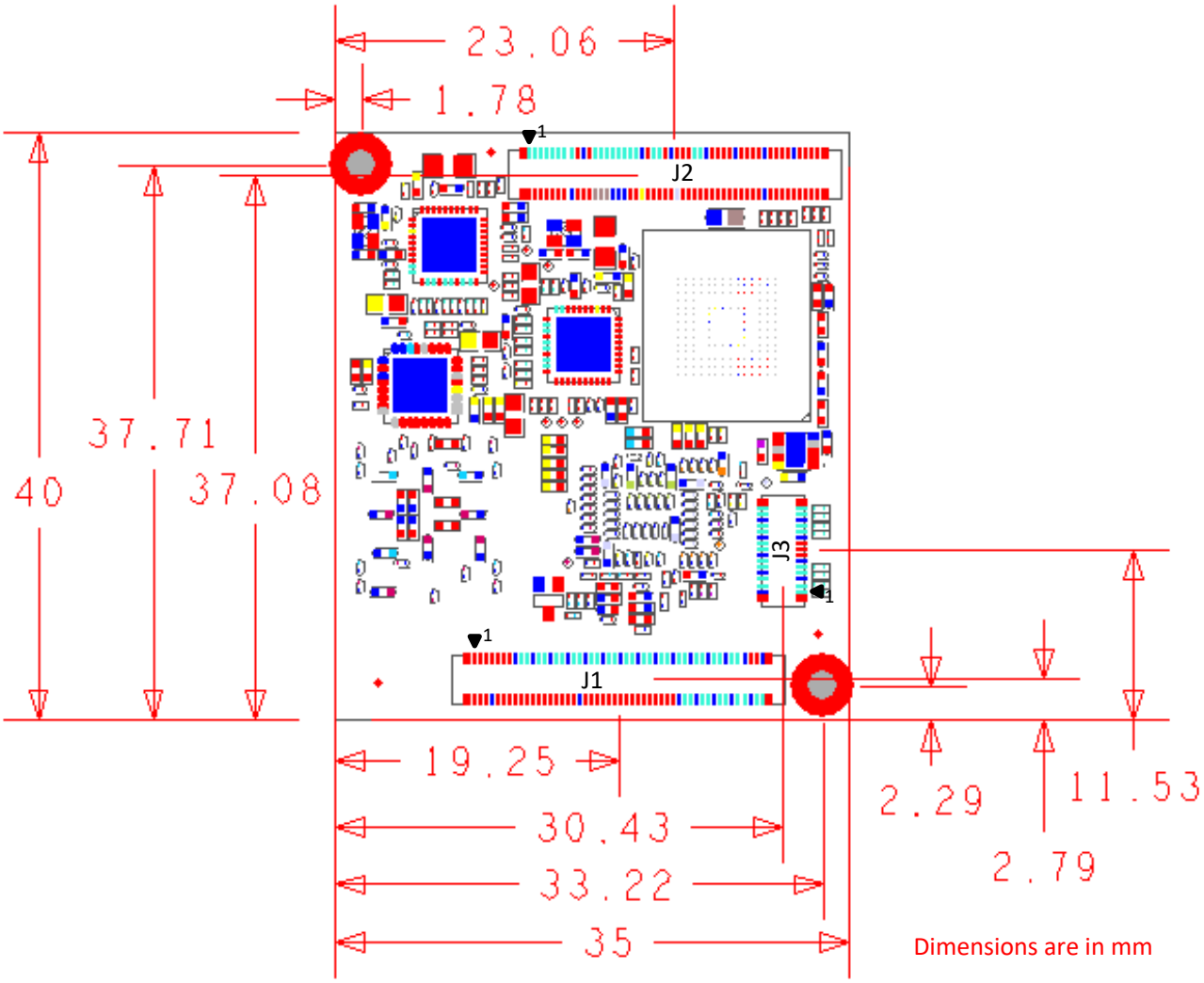

Figure 2: Mechanical Dimension from bottom side (dimensions in imm)

Dimensions	Description
Size	40mm x 35mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	13gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 SMT Steel Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.22.** This part is in F&S stock and can be ordered via F&S web shop.

The stack height of the space is 1.5mm. If a different stack height is needed, another spacer should be chosen.

Data sheet and 3D model (STP) is available on our website.

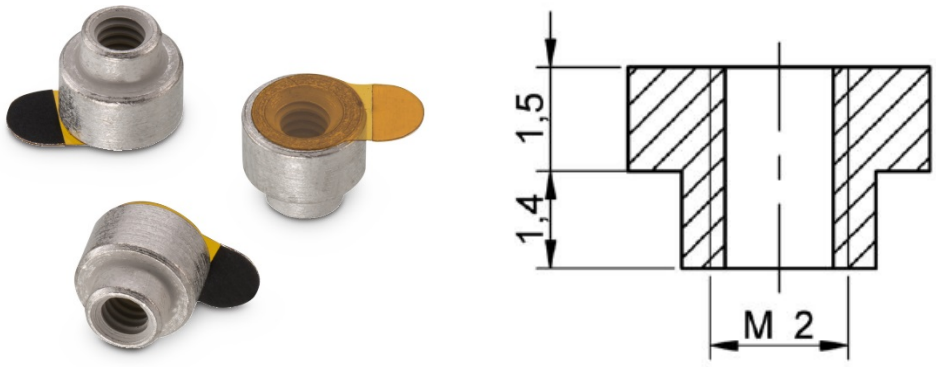

Figure 3: SMT Steel Spacer

2.2 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of heat spreader is **MHS.PC100.1** and can be ordered via F&S web shop.

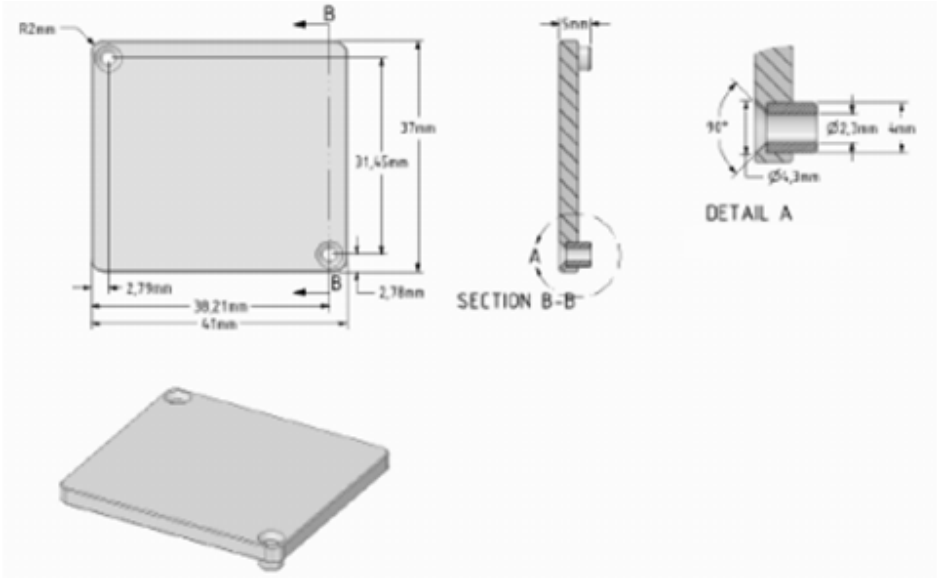

Figure 4: Heat Spreader (Images are not to scale)

3 Interface and Signal Description

3.1 B2B Connectors

PicoCore™MX8ULP uses two 100 pin connectors (J1/J2) from manufacturer Hirose.

Part number J1/J2: DF40C-100DP-0.4V.

Part number for the counterpart *J1/J2*: DF40C-100DS-0.4V

With this combination you get minimal stacking height of 1,5mm. Other possible stacking height by using different counterpart connector is: 3mm. The connector with 1,5mm stacking height is available at F&S and can be ordered in web shop.

Connector J1/J2 is compatible to J1/J2 of PicoCore™MX8MP (NXP i.MX8M Plus) and PicoCore™MX8MM (NXP i.MX8M Mini) and PicoCore™MX8MN (NXP i.MX8M Nano) and PicoCore™MX6UL100 (NXP i.MX6UL) and PicoCore™MX93 (NXP i.MX93).

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1						
J1	1	I2C_B_IRQ	PTA18	I	3.3V	
J1	3	I2C_B_SCL	PTE8	I/O	3.3V	2k49 PU
J1	5	I2C_B_SDA	PTE9	I/O	3.3V	2k49 PU
J1	7	GPIO_J1_7	PTF1	I/O	3.3V	2nd Fctn: RGB_D22 ⓘ 4.9 Display Interface
J1	9	BL_ON	PTF28	O	3.3V	Display Backlight Enable
J1	11	BL_PWM	PTF29	O	3.3V	Display Backlight PWM
J1	13	VLCD_ON	PTF30	O	3.3V	Display Power Enable
J1	15	GND	-	PWR	GND	
J1	17	DISP_A_CLK_P	DSI_CLK_P 2nd Fctn: PTF18	O	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D05 ⓘ 4.9 Display Interface
J1	19	DISP_A_CLK_N	DSI_CLK_N 2nd Fctn: PTF19	O	1.8V	4 Lane MIPI-DSI 2nd Fctn: DGB_D04 ⓘ 4.9 Display Interface
J1	21	GND	-	PWR	GND	
J1	23	DISP_A_DATA0_P	DSI_DATA0_P 2nd Fctn: PTF27	O	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_DE ⓘ 4.9 Display Interface
J1	25	DISP_A_DATA0_N	DSI_DATA0_N 2nd Fctn: PTF24	O	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_CLK ⓘ 4.9 Display Interface
J1	27	GND	-	PWR	GND	
J1	29	DISP_A_DATA1_P	DSI_DATA1_P 2nd Fctn: PTF22	O	1.8V	4 Lan MIPI-DSI 2nd Fctn: RGB_D01 ⓘ 4.9 Display Interface
J1	31	DISP_A_DATA1_N	DSI_DATA1_N 2nd Fctn: PTF23	O	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D00 ⓘ 4.9 Display Interface
J1	33	GND	-	PWR	GND	

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1	35	DISP_A_DATA2_P	DSI_DATA2_P 2nd Fctn: PTF20	I	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D03 ⓘ 4.9 Display Interface
J1	37	DISP_A_DATA2_N	DSI_DATA2_N 2nd Fctn: PTF21	I	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D02 ⓘ 4.9 Display Interface
J1	39	GND	-	PWR	GND	
J1	41	DISP_A_DATA3_P	DSI_DATA3_P 2nd Fctn: PTF16	I	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D07 ⓘ 4.9 Display Interface
J1	43	DISP_A_DATA3_N	DSI_DATA3_N 2nd Fctn: PTF17	I	1.8V	4 Lane MIPI-DSI 2nd Fctn: RGB_D06 ⓘ 4.9 Display Interface
J1	45	GND	-	PWR	GND	
J1	47	DISP_B_CLK_P	2nd Fctn: PTF8	O	1.8V	2nd Fctn: RGB_D15 ⓘ 4.9 Display Interface
J1	49	DISP_B_CLK_N	2nd Fctn: PTF9	O	1.8V	2nd Fctn: RGB_D14 ⓘ 4.9 Display Interface
J1	51	GND	-	PWR	GND	
J1	53	DISP_B_DATA0_P	2nd Fctn: PTF14	O	1.8V	2nd Fctn: RGB_D09 ⓘ 4.9 Display Interface
J1	55	DISP_B_DATA0_N	2nd Fctn: PTF15	O	1.8V	2nd Fctn: RGB_D08 ⓘ 4.9 Display Interface
J1	57	GND	-	PWR	GND	
J1	59	DISP_B_DATA1_P	2nd Fctn: PTF12	O	1.8V	2nd Fctn: RGB_D11 ⓘ 4.9 Display Interface
J1	61	DISP_B_DATA1_N	2nd Fctn: PTF13	O	1.8V	2nd Fctn: RGB_D10 ⓘ 4.9 Display Interface
J1	63	GND	-	PWR	GND	
J1	65	DISP_B_DATA2_P	2nd Fctn: PTF10	O	1.8V	2nd Fctn: RGB_D13 ⓘ 4.9 Display Interface
J1	67	DISP_B_DATA2_N	2nd Fctn: PTF11	O	1.8V	2nd Fctn: RGB_D12 ⓘ 4.9 Display Interface
J1	69	GND	-	PWR	GND	
J1	71	DISP_B_DATA3_P	2nd Fctn: PTF6	O	1.8V	2nd Fctn: RGB_D17 ⓘ 4.9 Display Interface
J1	73	DISP_B_DATA3_N	2nd Fctn: PTF7	O	1.8V	2nd Fctn: RGB_D16 ⓘ 4.9 Display Interface
J1	75	GND	-	PWR	GND	
J1	77	mPCIE_CTX_P	N.C.	N.C.	-	
J1	79	mPCIE_CTX_N	N.C.	N.C.	-	
J1	81	GND	-	PWR	GND	
J1	83	mPCIE_CRX_P	N.C.	N.C.	-	
J1	85	mPCIE_CRX_N	N.C.	N.C.	-	
J1	87	GND	-	PWR	GND	
J1	89	mPCIE_CLK_P	N.C.	N.C.	-	
J1	91	mPCIE_CLK_N	N.C.	N.C.	-	

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1	93	GND	-	PWR	GND	
J1	95	mPCIE_PERST	N.C.	N.C.	-	
J1	97	mPCIE_WAKE	N.C.	N.C.	-	
J1	99	GND	-	PWR	GND	
J1	2	GPIO_J1_2	PTF0	I/O	3.3V	2nd Fctn: RGB_D23 ⓘ 4.9 Display Interface
J1	4	I2C_A_SCL	PTE12	I/O	3.3V	No 2nd Fctn! I2C serial clock 2k49 PU
J1	6	I2C_A_SDA	PTE13	I/O	3.3V	No 2nd Fctn! I2C serial data 2k49 PU
J1	8	GND	-	PWR	GND	
J1	10	CAN_A_RX	PTA13	I	3.3V	CAN data receive
J1	12	CAN_A_TX	PTA12	O	3.3V	CAN data transmit
J1	14	UART_A_RTS	PTE5	O	3.3V	
J1	16	UART_A_CTS	PTE4	I	3.3V	
J1	18	UART_A_RXD	PTE7	I	3.3V	
J1	20	UART_A_TXD	PTE6	O	3.3V	
J1	22	UART_B_RTS	PTA17	O	3.3V	
J1	24	UART_B_CTS	PTA16	I	3.3V	
J1	26	UART_B_RXD	PTA3	I	3.3V	100k PU
J1	28	UART_B_TXD	PTA2	O	3.3V	
J1	30	UART_C_RXD	PTE11	I	3.3V	10k PU
J1	32	UART_C_TXD	PTE10	O	3.3V	
J1	34	UART_D_RXD	PTA11	I	3.3V	100k PU
J1	36	UART_D_TXD	PTA10	O	3.3V	
J1	38	GND	-	PWR	GND	
J1	40	I2C_C_SCL	PTA8	I/O	3.3V	2k49 PU
J1	42	I2C_C_SDA	PTA9	I/O	3.3V	2k49 PU
J1	44	GPIO_J1_44	PTA0	I/O	3.3V	2nd Fctn: CAN_B_TX 3rd Fctn: WLAN_WAKE ⓘ 4.6 CAN Interface
J1	46	GPIO_J1_46	PTA24	I/O	3.3V	2nd Fctn: CAN_B_RX 3rd Fctn: BT_WAKE ⓘ 4.6 CAN Interface
J1	48	I2C_D_SCL	PTA14	I/O	3.3V	No 2nd Fctn! ⓘ 0 I2C Interface 2k49 PU
J1	50	I2C_D_SDA	PTA15	I/O	3.3V	No 2nd Fctn! ⓘ 0 I2C Interface 2k49 PU
J1	52	GPIO_J1_52	PTF26	I/O	3.3V	2nd Fctn: RGB_HSYNC ⓘ 4.9 Display Interface

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1	54	GPIO_J1_54	PTF25	I/O	3.3V	2nd Fctn: RGB_ VSYNC ⓘ 4.9 Display Interface
J1	56	SPI_B_SS0	PTA7	I	3.3V	SPI slave select
J1	58	SPI_B_MISO	PTA5	I	3.3V	SPI master in slave out
J1	60	SPI_B_MOSI	PTA4	O	3.3V	SPI master out slave in
J1	62	SPI_B_SCLK	PTA6	O	3.3V	SPI serial clock
J1	64	SPI_A_SS0	PTF11	I	3.3V	SPI slave select Shared with RGB_D12 /DSI_B_DATA2_N Mounting option!
J1	66	SPI_A_MISO	PTF9	I	3.3V	SPI master in slave out Shared with RGB_D14 /DSI_B_CLK_N Mounting option!
J1	68	SPI_A_MOSI	PTF8	O	3.3V	SPI master out slave in Shared with RGB_D15 /DSI_B_CLK_P Mounting option!
J1	70	SPI_A_SCLK	PTF10	O	3.3V	SPI serial clock Shared with RGB_D13 /DSI_B_DATA2_P Mounting option!
J1	72	GND	-	PWR	GND	
J1	74	CSI_CLK_P	CSI_CLK_P	I/O	1.8V	ⓘ Camera Serial Interface
J1	76	CSI_CLK_N	CSI_CLK_N	I/O	1.8V	ⓘ Camera Serial Interface
J1	78	GND	-	PWR	GND	
J1	80	CSI_DATA0_P	CSI_DATA0_P	I	1.8V	ⓘ Camera Serial Interface
J1	82	CSI_DATA0_N	CSI_DATA0_N	I	1.8V	ⓘ Camera Serial Interface
J1	84	GND	-	PWR	GND	
J1	86	CSI_DATA1_P	CSI_DATA1_P	I	1.8V	ⓘ Camera Serial Interface
J1	88	CSI_DATA1_N	CSI_DATA1_N	I	1.8V	ⓘ Camera Serial Interface
J1	90	GND	-	PWR	GND	
J1	92	CSI_DATA2_P	N.C.	N.C.	-	
J1	94	CSI_DATA2_N	N.C.	N.C.	-	
J1	96	GND	-	PWR	GND	
J1	98	CSI_DATA3_P	N.C.	N.C.	-	
J1	100	CSI_DATA3_N	N.C.	N.C.	-	
J2						
J2	1	ETH_A_D1_P	KSZ8081: TXP 2nd Fctn: PTE15	Analog	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_ETH_MDC

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J2	3	ETH_A_D1_N	KSZ8081: TXN 2nd Fctn: PTE14	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_ETH_MDIO
J2	5	ETH_A_D2_P	KSZ8081: RXP 2nd Fctn: PTE16	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_TXEN
J2	7	ETH_A_D2_N	KSZ8081: RXN 2nd Fctn: N.C.	Ana-log		ⓘ 4.7 Ethernet 2nd Fctn: RMII -> N.C.
J2	9	ETH_A_D3_P	N.C. 2nd Fctn: PTE23	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_TXD0
J2	11	ETH_A_D3_N	N.C. 2nd Fctn: PTE22	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_TXD1
J2	13	ETH_A_D4_P	N.C. 2nd Fctn: PTE3	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_TXCLK
J2	15	ETH_A_D4_N	N.C.	Ana-log	-	ⓘ 4.7 Ethernet 2nd Fctn: RMII -> N.C.
J2	17	ETH_A_LED	KSZ8081: LED0	O	3.3V	ⓘ 4.7 Ethernet Default: link LED 2k49 PU
J2	19	GND	-	PWR	GND	
J2	21	ETH_B_LED	N.C.	N.C.	-	
J2	23	ETH_B_D1_P	N.C. 2nd Fctn: PTE18	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_CRS_DV
J2	25	ETH_B_D1_N	N.C. 2nd Fctn: PTE17	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_RXER
J2	27	ETH_B_D2_P	N.C. 2nd Fctn: PTE21	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_RXD0
J2	29	ETH_B_D2_N	N.C. 2nd Fctn: PTE20	Ana-log	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_RXD1
J2	31	ETH_B_D3_P	N.C.	Ana-log		
J2	33	ETH_B_D3_N	N.C.	Ana-log		
J2	35	ETH_B_D4_P	N.C. 2nd Fctn: PTE2	I/O	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_ETH_IRQ
J2	37	ETH_B_D4_N	N.C. 2nd Fctn: PTF31	I/O	3.3V	ⓘ 4.7 Ethernet 2nd Fctn: RMII_ETH_RST
J2	39	GND	-	PWR	GND	
J2	41	USB_HOST_VBUS	USB1_VBUS_DE-TECT	I	5V	10k PD ⓘ 4.1 USB 2.0 Interface
J2	43	USB_HOST_D_P	USB1_DP	I/O		ⓘ 4.1 USB 2.0 Interface
J2	45	USB_HOST_D_N	USB1_DN	I/O		ⓘ 4.1 USB 2.0 Interface
J2	47	USB_HOST_PWR	PTD11	O	3.3V	ⓘ 4.1 USB 2.0 Interface USB Host Power Enable
J2	49	GND	-	PWR	GND	
J2	51	USB_OTG_VBUS	USB0_VBUS_DE-TECT	I	5V	10k PD ⓘ 4.1 USB 2.0 Interface
J2	53	USB_OTG_PWR	PTD13	O	3.3V	ⓘ 4.1 USB 2.0 Interface USB Power Enable
J2	55	USB_OTG_ID	PTD12	I	3.3V	ⓘ 4.1 USB 2.0 Interface

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J2	57	USB_OTG_D_P	USB1_DP	I/O		ⓘ 4.1 USB 2.0 Interface
J2	59	USB_OTG_D_N	USB1_DN	I/O		ⓘ 4.1 USB 2.0 Interface
J2	61	GND	-	PWR	GND	
J2	63	PWM	PTC12	O	3.3V	
J2	65	GPIO_J2_65	PTC10 2nd Fctn: PTF2	I/O	3.3V	AUDIO_B_I2S_MCLK ⓘ 4.8 Audio Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio2nd Fctn: RGB_D21 ⓘ 4.9 Display Interface
J2	67	GPIO_J2_67	PTC9 2nd Fctn: PTF3	I/O	3.3V	AUDIO_B_I2S_TXFS ⓘ 4.8 Audio 2nd Fctn: RGB_D20 ⓘ 4.9 Display Interface
J2	69	GPIO_J2_69	PTC8	I/O	3.3V	AUDIO_B_I2S_TXC ⓘ 4.8 Audio
J2	71	GND	-	PWR	GND	
J2	73	GPIO_J2_73	PTC7	I/O	3.3V	AUDIO_B_I2S_TXD ⓘ 4.8 Audio
J2	75	GPIO_J2_75	PTC4	I/O	3.3V	AUDIO_B_I2S_RXD ⓘ 4.8 Audio
J2	77	GPIO_J2_77	PTC3	I/O	3.3V	AUDIO_B_I2S_RXFS ⓘ 4.8 Audio
J2	79	GPIO_J2_79	PTC2	I/O	3.3V	AUDIO_B_I2S_RXC ⓘ 4.8 Audio
J2	81	GND	-	PWR	GND	
J2	83	GPIO_J2_83	PTC16	I/O	3.3V	SPI_C_SS0
J2	85	GPIO_J2_85	PTC14	I/O	3.3V	SPI_C_MISO
J2	87	GPIO_J2_87	PTC13	I/O	3.3V	SPI_C_MOSI
J2	89	GPIO_J2_89	PTC15	I/O	3.3V	SPI_C_SCLK
J2	91	GND	-	PWR	GND	
J2	93	JTAG_TCK	PTA21	I	3.3V	
J2	95	JTAG_TMS	PTA20	I	3.3V	
J2	97	JTAG_TDI	PTA23	I	3.3V	
J2	99	JTAG_TDO	PTA22	O	3.3V	
J2	2	AUDIO_A_VCC	-	PWR	3V ~ 3.3V	ⓘ 4.8 Audio
J2	4	AUDIO_A_GND	-	PWR		ⓘ 4.8 Audio
J2	6	AUDIO_A_LOUT_L	SGTL5000: LOUT 2nd Fctn: PTC21 3rd Fctn: PTF15	O		ⓘ 4.8 Audio 2nd Fctn: I2S_SCLK
J2	8	AUDIO_A_LOUT_R	SGTL5000: ROUT 2nd Fctn: PTC22 3rd Fctn: PTF16	O		ⓘ 4.8 Audio 2nd Fctn: I2S_LRCLK
J2	10	AUDIO_A_MIC	SGTL5000: MICIN			ⓘ 4.8 Audio

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J2	12	AUDIO_A_LIN_L	SGTL5000: LLINEIN 2nd Fctn: PTC23 3rd Fctn: PTF14			ⓘ 4.8 Audio 2nd Fctn: I2S_MCLK
J2	14	AUDIO_A_LIN_R	SGTL5000: RLINEIN			ⓘ 4.8 Audio
J2	16	GND	-	PWR	GND	
J2	18	AUDIO_A_HP_L	SGTL5000: LHPOUT 2nd Fctn: PTC20 3rd Fctn: PTF17	O		ⓘ 4.8 Audio 2nd Fctn: I2S_DOUT
J2	20	AUDIO_A_HP_R	SGTL5000: RHPOUT 2nd Fctn: PTC17 3rd Fctn: PTF12	O		ⓘ 4.8 Audio 2nd Fctn: I2S_DIN
J2	22	AU- DIO_A_HP_GND	SGTL5000: HP_VGND	PWR		ⓘ 4.8 Audio
J2	24	VDD_VIN	VSYS	PWR	5.0V	ⓘ 4.15 Power and Power Control Pins
J2	26	VDD_VIN	VSYS	PWR	5.0V	ⓘ 4.15 Power and Power Control Pins
J2	28	VDD_VIN	VSYS	PWR	5.0V	ⓘ 4.15 Power and Power Control Pins
J2	30	GND	-	PWR	GND	
J2	32	GND	-	PWR	GND	
J2	34	GND	-	PWR	GND	
J2	36	VDD_BAT_IN	-	PWR	0.9V .. 5.5V	ⓘ 4.15 Power and Power Control Pins RTC battery backup supply voltage
J2	38	RESERVED	N.C.	N.C:	-	
J2	40	VDD_3V3	VIO	O	3.3V	20mA output from on module DCDC powered from VDD_VIN
J2	42	RESET_IN	PMIC_RST_B	I	1.8V	ⓘ 4.15 Power and Power Control Pins
J2	44	PMIC_STBY	PMIC_STBY_REQ	O	1.8V	ⓘ 4.15 Power and Power Control Pins
J2	46	PMIC_ON_REQ	PMIC_ON_REQ	O	1.8V	ⓘ 4.15 Power and Power Control Pins
J2	48	ON_OFF	ONOFF	I	1.8V	ⓘ 4.15 Power and Power Control Pins Toggle state from ON to OFF 100k PU to 1.8V
J2	50	BOOTSEL	-	I	3.3V	ⓘ 5 Boot Mode Service jumper, normally left open
J2	52	SD_A_VCC	PMIC: LDO5	O	3.3V	ⓘ 4.2 SD Card Interface SD_A Supply Voltage, 150mA max Output
J2	54	RESERVED	-	N.C:	-	
J2	56	SD_A_RST	PTF0	O	3.3V	ⓘ 4.2 SD Card Interface

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J2	58	SD_A_WP	PTF1		3.3V	ⓘ 4.2 SD Card Interface No write protect pin available.
J2	60	SD_A_CD	PTF2	I	3.3V	ⓘ 4.2 SD Card Interface SD card detect
J2	62	SD_A_CMD	PTD23	O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	64	SD_A_CLK	PTD22	O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	66	SD_A_DATA0	PTD21	I/O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	68	SD_A_DATA1	PTD20	I/O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	70	SD_A_DATA2	PTD19	I/O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	72	SD_A_DATA3	PTD18	I/O	3.3V	ⓘ 4.2 SD Card Interface N.C. if WLAN/BT mounted
J2	74	SD_A_DATA4	PTD17	I/O	3.3V	ⓘ 4.2 SD Card Interface
J2	76	SD_A_DATA5	PTD16	I/O	3.3V	ⓘ 4.2 SD Card Interface
J2	78	SD_A_DATA6	PTD15	I/O	3.3V	ⓘ 4.2 SD Card Interface
J2	80	SD_A_DATA7	PTD14	I/O	3.3V	ⓘ 4.2 SD Card Interface
J2	82	GND	GND	PWR	GND	
J2	84	SD_B_RST	PTC0	I/O	3.3V	No SD Card B Interface
J2	86	SD_B_WP	PTC1	I/O	3.3V	No SD Card B Interface
J2	88	SD_B_CD	PTC5	I/O	3.3V	No SD Card B Interface
J2	90	SD_B_CMD	PTC6	I/O	3.3V	No SD Card B Interface
J2	92	SD_B_CLK	PTC11	O	3.3V	No SD Card B Interface
J2	94	SD_B_DATA0	PTF4	I/O	3.3V	No SD Card B Interface 2nd Fctn: RGB_D19 ⓘ 4.9 Display Interface
J2	96	SD_B_DATA1	PTF5	I/O	3.3V	No SD Card B Interface 2nd Fctn: RGB_D18 ⓘ 4.9 Display Interface
J2	98	SD_B_DATA2	PTC18	I/O	3.3V	No SD Card B Interface
J2	100	SD_B_DATA3	PTC19	I/O	3.3V	No SD Card B Interface

Table 2: B2B connector

4 Interfaces

4.1 USB 2.0 Interface

PicoCore™MX8ULP module can support 2x USB 2.0 OTG. The USB OTG can also support USB-Type C connection.

The 90 Ohm differential pairs of USB signals needs no termination.

For external ports ESD and EMV protection is required nearby the USB connectors.

If the USB OTG will be used in Host Mode, the **USB_OTG_ID** pin should be pulled down to GND with a resistor. Otherwise, it must be directly connected to the USB connector.

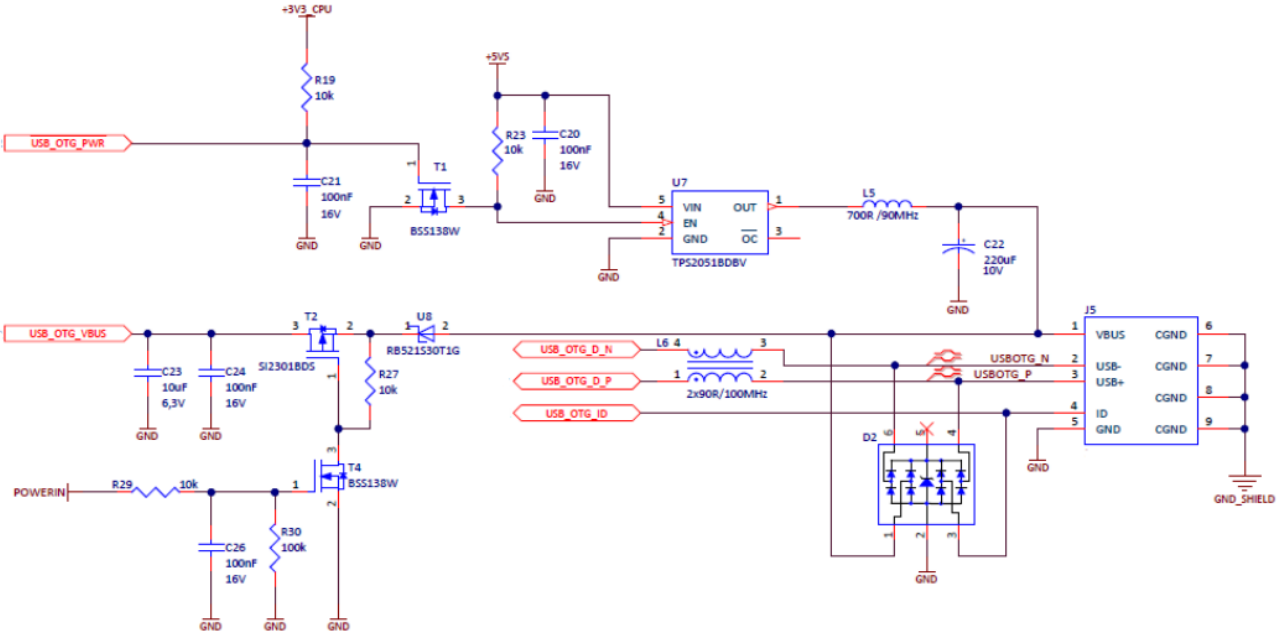

Figure 5: USB OTG example connection

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
USB Host 2.0						
J2	41	USB_HOST_VBUS	USB2_VBUS	I	5.0V	USB Host voltage detection. There is a resistance divider to scale 5V to 3.3V CPU input. N.C. for USB host function.
J2	43	USB_HOST_D_P	USB2_D_P	I/O	3.3V	90Ohm differential pair
J2	45	USB_HOST_D_N	USB2_D_N	I/O	3.3V	90Ohm differential pair
J2	47	USB_HOST_PWR	GPIO1_IO28	O	3.3V	**No pull-up/down on module**
USB OTG 2.0						
J2	51	USB_OTG_VBUS	USB1_VBUS	I	5.0V	USB OTG Voltage detection. There is a resistance divider to scale 5V to 3.3V CPU input. N.C. for USB host function.
J2	53	USB_OTG_PWR	GPIO1_IO29	O	3.3V	**No pull-up/down on module**
J2	55	USB_OTG_ID	USB1_ID	I	3.3V	Should be pulled down to GND for Host Mode, otherwise connect directly to the connector
J2	57	USB_OTG_D_P	USB1_D_P	I/O	3.3V	90Ohm differential pair
J2	59	USB_OTG_D_N	USB1_D_N	I/O	3.3V	90Ohm differential pair

Table 3: USB Host & OTG Interface

4.2 SD Card Interface

The PicoCore™MX8ULP module can support one SD Card Interfaces (SD_A). For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The SD_A interface support 8 bit with card detect and reset. There is no dedicated write protect pin. SD_A_VCC is fixed to 3.3V for SD_A Interface. The current output is limited to 150mA. The SD_A interface is shared with the WLAN/BT module. This interface is only available if WLAN/BT isn't mounted on module.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
SDIO_A [optional without WLAN/BT]						
J2	52	SD_A_VCC	-	O	3.3V	Selectable; max 150mA output
J2	54	NC	NC	NC	3.3V	
J2	56	SD_A_RST	PTF0	O	3.3V	active low; 100k pull-up on module
J2	58	SD_A_WP	PTF1	NC	3.3V	No dedicated I/O available.
J2	60	SD_A_CD	PTF2	I	3.3V	
J2	62	SD_A_CMD	PTD23	O	3.3V	100k pull-up on module
J2	64	SD_A_CLK	PTD22	O	3.3V	
J2	66	SD_A_DATA0	PTD21	I/O	3.3V	100k pull-up on module
J2	68	SD_A_DATA1	PTD20	I/O	3.3V	
J2	70	SD_A_DATA2	PTD19	I/O	3.3V	
J2	72	SD_A_DATA3	PTD18	I/O	3.3V	
J2	74	SD_A_DATA4	PTD17	I/O	3.3V	
J2	76	SD_A_DATA5	PTD16	I/O	3.3V	
J2	78	SD_A_DATA6	PTD15	I/O	3.3V	
J2	80	SD_A_DATA7	PTD14	I/O	3.3V	

Table 4: SD Card Interface Pinout

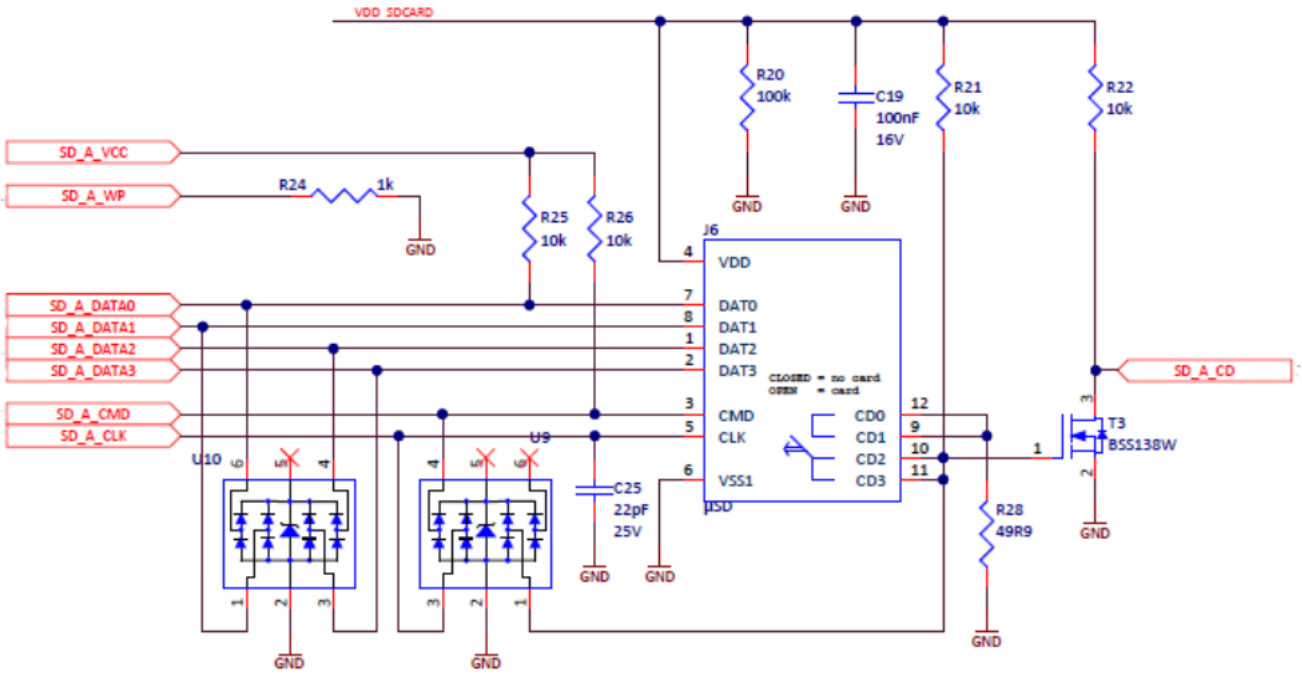

Figure 6: SD Card connector example connection

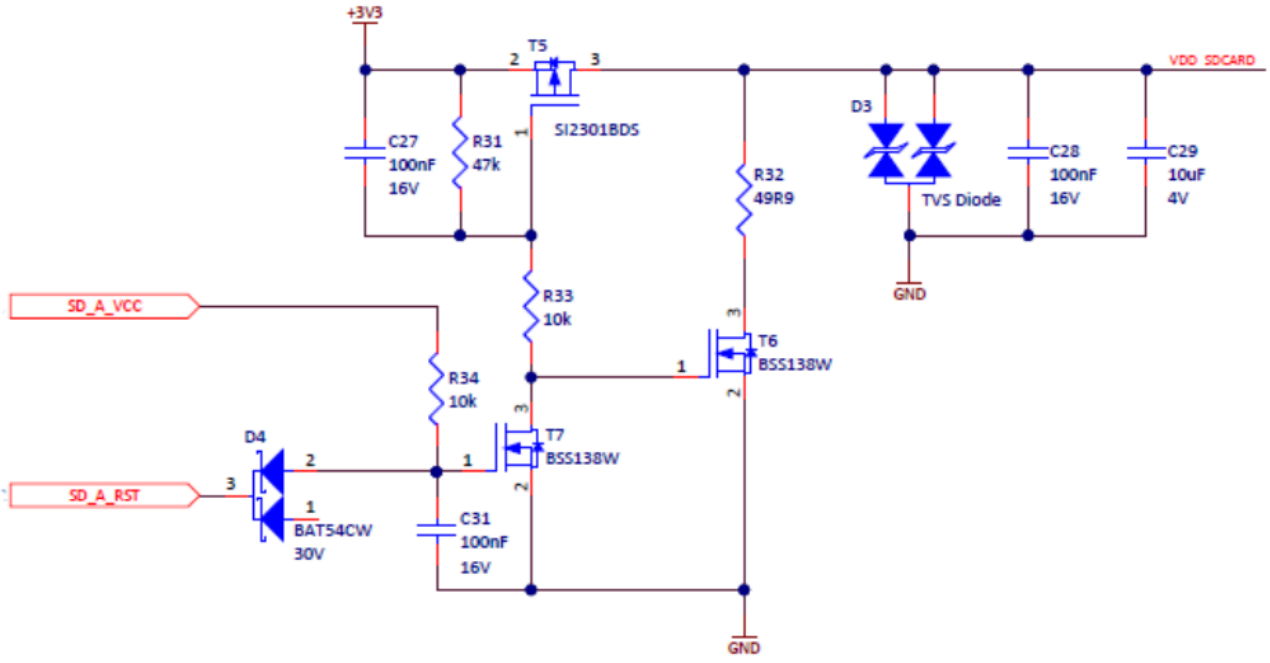

Figure 7: SD_A supply voltage switching circuit

4.3 Serial Peripheral Interface (SPI)

The module support three Hi-Speed SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage levels need a level shifter.

Signals don't have pull-ups on module.

The SPI_A is shared with RGB. This interface is only available if the RGB option isn't mounted on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*	MM*	Voltage	Remarks
SPI_A							
J1	64	SPI_A_SS0	PTF11	I	O	3.3V	SPI slave select Shared with RGB_D12 /DSI_B_DATA2_N Mounting option!
J1	66	SPI_A_MISO	PTF9	O	I	3.3V	SPI master in slave out Shared with RGB_D14 /DSI_B_CLK_N Mounting option!
J1	68	SPI_A_MOSI	PTF8	I	O	3.3V	SPI master out slave in Shared with RGB_D15 /DSI_B_CLK_P Mounting option!
J1	70	SPI_A_SCLK	PTF10	I	O	3.3V	SPI serial clock Shared with RGB_D13 /DSI_B_DATA2_P Mounting option!
SPI_B							
J1	56	SPI_B_SS0	PTA7	I	O	3.3V	SPI slave select
J1	58	SPI_B_MISO	PTA5	O	I	3.3V	SPI master in slave out
J1	60	SPI_B_MOSI	PTA4	I	O	3.3V	SPI master out slave in
J1	62	SPI_B_SCLK	PTA6	I	O	3.3V	SPI serial clock
SPI_C							
J1	56	SPI_C_SS0	PTC16	I	O	3.3V	SPI slave select Not compatible with other PicoCores!
J1	58	SPI_C_MISO	PTC14	O	I	3.3V	SPI master in slave out Not compatible with other PicoCores!
J1	60	SPI_C_MOSI	PTC13	I	O	3.3V	SPI master out slave in Not compatible with other PicoCores!
J1	62	SPI_C_SCLK	PTC15	I	O	3.3V	SPI serial clock Not compatible with other PicoCores!

**SM: PicoCore™MX8ULP used in Slave Mode, MM: PicoCore™MX8ULP used in Master Mode*

Table 5: Serial Peripheral Interface (SPI) Pinout

4.4 I2C Interface

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter.

For more chip selects, interrupts and other signals GPIOs can be used and the driver can be modified.

Note:
I2C_A is used to control a I2C EEPROM on module. Therefore it's not possible to use this contacts as GPIO or any other function. On the EEPROM the Board information is stored.

Note:
I2C_D is used to control several peripherals on module (i.e. RTC, EEPROM, Audio Codec, PMIC, GPIO expander…). Therefore it's not possible to use this contacts as GPIO or any other function. For I2C_D, PicoCore™ is always the bus master. Please use I2C_A/B/C before using I2C_D.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
I2C_A						
J1	4	I2C_A_SCL	PTE12	O	3.3V	2.49k pull-up on module
J1	6	I2C_A_SDA	PTE13	I/O	3.3V	2.49k pull-up on module
I2C_B						
J1	1	I2C_B_IRQ	PTA18	I	3.3V	
J1	3	I2C_B_SCL	PTE8	O	3.3V	2.49k pull-up on module
J1	5	I2C_B_SDA	PTE9	I/O	3.3V	2.49k pull-up on module
I2C_C						
J1	40	I2C_C_SCL	PTA8	O	3.3V	2.49k pull-up on module
J1	42	I2C_C_SDA	PTA9	I/O	3.3V	2.49k pull-up on module
I2C_D						
J1	48	I2C_D_SCL	PTA14	O	3.3V	2.49k pull-up on module
J1	50	I2C_D_SDA	PTA15	I/O	3.3V	2.49k pull-up on module

Table 6: I2C Interface Pinout

I2C	Address	Device	Function
I2C_A	0x50	N24S64B	EEPROM
I2C_D	0x51	PCF85263ATL	Low Power RTC
I2C_D	0x0A	SGTL5000	Audio Codec
Internal I2C	0x32	PCA9451A	PMIC

Table 7: On Module I2C Devices

4.5 Serial Interface (UART)

	Pin	Default Function	CPU Pad	I/O	Voltage	Remarks
UART_A						
J1	14	UART_A_RTS	PTE5	O	3.3V	
J1	16	UART_A_CTS	PTE4	I	3.3V	
J1	18	UART_A_RXD	PTE7	I	3.3V	100k pull-up on module
J1	20	UART_A_TXD	PTE6	O	3.3V	
UART_B						
J1	22	UART_B_RTS	PTA17	O	3.3V	
J1	24	UART_B_CTS	PTA16	I	3.3V	
J1	26	UART_B_RXD	PTA3	I	3.3V	100k pull-up on module
J1	28	UART_B_TXD	PTA2	O	3.3V	
UART_C						
J1	30	UART_C_RXD	PTE11	I	3.3V	100k pull-up on module
J1	32	UART_C_TXD	PTE10	O	3.3V	
UART_D						
J1	34	UART_D_RXD	PTA11	I	3.3V	100k pull-up on module
J1	36	UART_D_TXD	PTA10	O	3.3V	

Table 8: UART Interface Pin Out

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

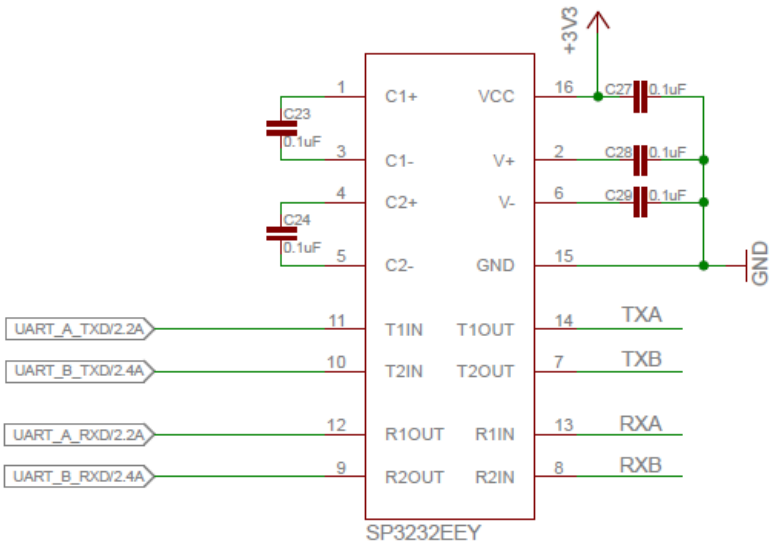

Figure 8: UART transceiver example

4.6 CAN Interface

PicoCore™MX8ULP module can support two CAN buses, which are shared with other interfaces or signals. With the CAN bus usage, the other interfaces cannot be used.

There are no on-module pull-up or pull-downs for the CAN signals.

The CAN_B interface is shared with the WLAN/BT module. This interface is only available if WLAN/BT isn't mounted on module.

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
CAN_A						
J1	10	CAN_A_RX	PTA13	I	3.3V	CAN data receive
J1	12	CAN_A_TX	PTA12	O	3.3V	CAN data transmit
CAN_B						
J1	44	GPIO_J1_44	PTA0	I/O	3.3V	CAN_B_TX
J1	46	GPIO_J1_46	PTA24	I/O	3.3V	CAN_B_RX

Table 9: CAN Interface Pinout

4.7 Ethernet

4.7.1 Ethernet Interface with 100Mbit PHY

The module supports one 10/100 Mbit LAN interface via Microchip KSZ8081RNAIA Ethernet PHY. There is a mounting option to route one RMII to the pins of ETH_A and ETH_B.

ETH_B is only used for RMII. There is no second Phy on the PicoCoreMX8ULP, only one Ethernet Interface is available.

	Pin	Pin Name	RT8211 Pad	I/O	Voltage	Remarks
Ethernet A (PHY_1: KSZ8081RNAIA)						
J2	1	ETH_A_D1_P	MDIP0	I/O		
J2	3	ETH_A_D1_N	MDIN0	I/O		
J2	5	ETH_A_D2_P	MDIP1	I/O		
J2	7	ETH_A_D2_N	MDIN1	I/O		
J2	17	ETH_A_LED	LED1	O		Activity LED (RX/TX)

Table 10: Ethernet A Signals

4.7.2 Ethernet RMII Interface

Without Ethernet PHY: The module supports one 10/100Mbit LAN interface via RMII signals. The RMII signals can be reached from the B2B Connector.

An external Ethernet-PHY or an external Ethernet switch is required on baseboard/carrier board.

	Pin	Pin Name	RMII Function Pad	CPU Pad	I/O	Voltage	Remarks
		RGMII Interface [optional]					
J2	1	ETH_A_D1_P	ENET1_MDC	PTE15	O	3.3V	
J2	3	ETH_A_D1_N	ENET1_MDIO	PTE14	I/O	3.3V	
J2	5	ETH_A_D2_P	ENET1_TXEN	PTE16	O	3.3V	
J2	9	ETH_A_D3_P	ENET1_TD0	PTE23	O	3.3V	
J2	11	ETH_A_D3_N	ENET1_TD1	PTE22	O	3.3V	
J2	13	ETH_A_D4_P	ENET1_TXCLK	PTE3	O	3.3V	
J2	23	ETH_B_D1_P	ENET1_CRS_DV	PTE18	I	3.3V	
J2	25	ETH_B_D1_N	ENET1_RXER	PTE17	I	3.3V	
J2	27	ETH_B_D2_P	ENET1_RD0	PTE21	I	3.3V	
J2	29	ETH_B_D2_N	ENET1_RD1	PTE20	I	3.3V	
J2	35	ETH_B_D4_P	ENET1_IRQ	PTE2	I	3.3V	
J2	37	ETH_B_D4_N	ENET1_RST	PTF31	O	3.3V	

Table 11: RGMII Interface Signals

4.8 Audio

The PicoCore™MX8ULP module can support two audio interfaces.

4.8.1 Audio_A

AUDIO_A interface can either be directly I2S signals or with an external audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support the MIC function.

AUDIO_A_VCC is supplied from the PMIC on PicoCore™ Module as default. For a better and smoother audio quality an external low-noise power supply (e.g. LDO) is highly recommended (3V~3.3V – 5mA). In this case, the intern voltage source must be separated from the audio circuitry. Please contact us to have the correct jumper configuration for the external-supplied AUDIO_A_VCC.

The I2S signale can be routed from two different CPU domains (PTC & PTF). The PTF pins are shared with RGB. This interface is only available if the RGB option isn't mounted on module.

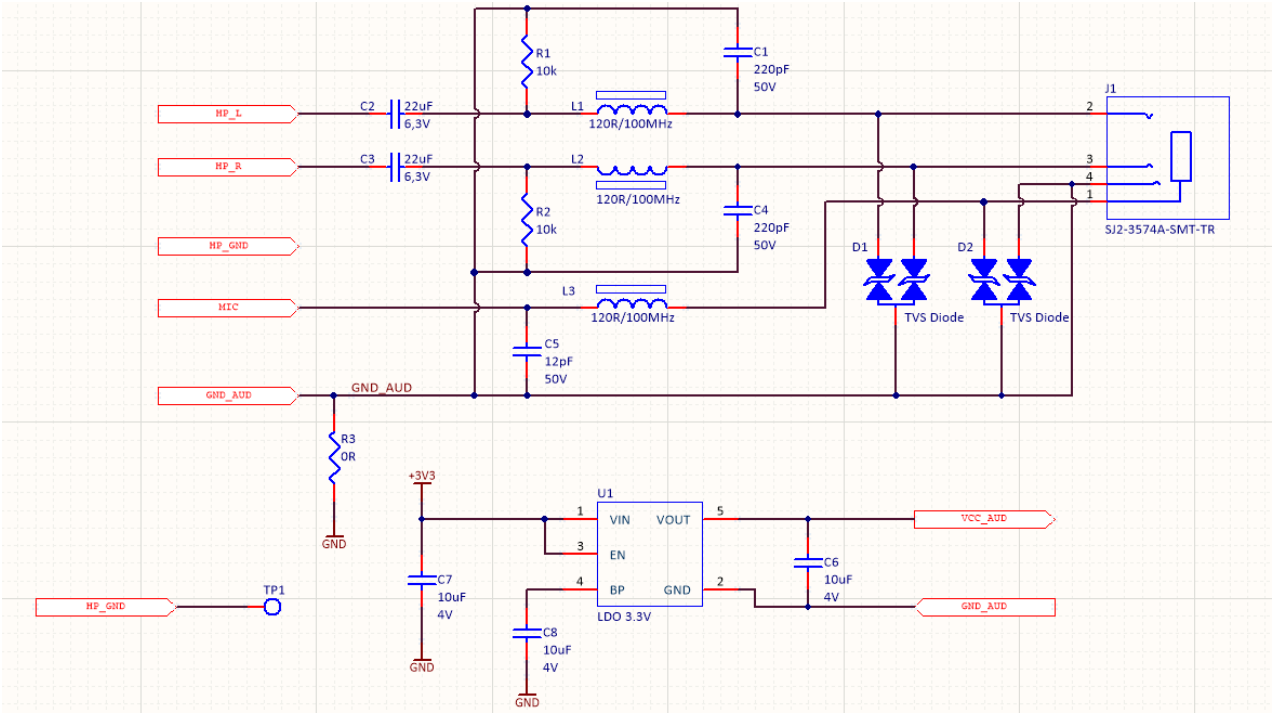

Figure 9: Headphone-Out Mic-In Example Circuit

	Pin	Signal	CPU Pad	I/O	Voltage*	Remarks
Audio A – with Audio Codec (SGTL5000) [optional]						
J2	2	AUDIO_A_VCC	VDDA	PWR	3V/3.3V	max 16.50mW power consumption
J2	4	AUDIO_A_GND	AGND	PWR	GND	
J2	6	AUDIO_A_LOUT_L	LOUT	O	3V/3.3V	
J2	8	AUDIO_A_LOUT_R	ROUT	O	3V/3.3V	
J2	10	AUDIO_A_MIC	MICIN	I	3V/3.3V	
J2	12	AUDIO_A_LIN_L	LLINEIN	I	3V/3.3V	
J2	14	AUDIO_A_LIN_R	RLINEIN	I	3V/3.3V	
J2	18	AUDIO_A_HP_L	LHPOUT	O	3V/3.3V	
J2	20	AUDIO_A_HP_R	RHPOUT	O	3V/3.3V	
J2	22	AUDIO_A_HP_GND	HP_VGND	O	GND	
Audio A – I2S Option (without Audio Codec) [PTC]						
J2	2	AUDIO_A_VCC	N.C.	-	-	Do Not Connect! Leave open
J2	4	AUDIO_A_GND	N.C.	-	-	Do Not Connect! Leave open
J2	6	AUDIO_A_LOUT_L	PTC21	I/O	3.3V	I2S_A_SCLK
J2	8	AUDIO_A_LOUT_R	PTC22	I/O	3.3V	I2S_A_LRCLK
J2	10	AUDIO_A_MIC	N.C.	-	-	Do Not Connect! Leave open
J2	12	AUDIO_A_LIN_L	PTC23	O	3.3V	I2S_A_MCLK
J2	14	AUDIO_A_LIN_R	N.C.	-	-	Do Not Connect! Leave open
J2	18	AUDIO_A_HP_L	PTC17	I	3.3V	I2S_A_DIN
J2	20	AUDIO_A_HP_R	PTC20	O	3.3V	I2S_A_DOUT
J2	22	AUDIO_A_HP_GND	N.C.	-	-	Do Not Connect! Leave open
Audio A – I2S Option (without Audio Codec) [PTF]						
J2	2	AUDIO_A_VCC	N.C.	-	-	Do Not Connect! Leave open
J2	4	AUDIO_A_GND	N.C.	-	-	Do Not Connect! Leave open
J2	6	AUDIO_A_LOUT_L	PTF15	I/O	3.3V	I2S_A_SCLK
J2	8	AUDIO_A_LOUT_R	PTF16	I/O	3.3V	I2S_A_LRCLK
J2	10	AUDIO_A_MIC	N.C.	-	-	Do Not Connect! Leave open
J2	12	AUDIO_A_LIN_L	PTF14	O	3.3V	I2S_A_MCLK
J2	14	AUDIO_A_LIN_R	N.C.	-	-	Do Not Connect! Leave open
J2	18	AUDIO_A_HP_L	PTF12	I	3.3V	I2S_A_DIN
J2	20	AUDIO_A_HP_R	PTF17	O	3.3V	I2S_A_DOUT
J2	22	AUDIO_A_HP_GND	N.C.	-	-	Do Not Connect! Leave open

**Depends on the AUDIO_A_VCC source*

Table 12: Audio A Interface

4.8.2 Audio_B

AUDIO_B can only be I2S signals. The I2S signals can be routed from two different CPU domains (PTC & PTF). The PTF pins are shared with RGB. This interface is only available if the RGB option isn't mounted on module.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
Audio B – I2S Option (without Audio Codec)						
J2	2	GPIO_J2_65	PTC10 / PTF2	O	3.3V	AUDIO_B_I2S_MCLK 2nd Fctn: RGB_D21
J2	4	GPIO_J2_67	PTC9 / PTF3	O	3.3V	AUDIO_B_I2S_TXFS 2nd Fctn: RGB_D20
J2	6	GPIO_J2_69	PTC8	O	3.3V	AUDIO_B_I2S_TXC
J2	8	GPIO_J2_73	PTC7	O	3.3V	AUDIO_B_I2S_TXD
J2	10	GPIO_J2_75	PTC4	I	3.3V	AUDIO_B_I2S_RXD
J2	12	GPIO_J2_77	PTC3	I	3.3V	AUDIO_B_I2S_RXFS
J2	14	GPIO_J2_79	PTC2	I	3.3V	AUDIO_B_I2S_RXC

Table 13: Audio B Interface

4.9 Display Interface

The PicoCore™MX8ULP module support MIPI DSI interface and RGB interface.

On the module there are 2 display channels. Display interfaces can be reached via those channels optionally. For the RGB interface some other functions are not available:

- Audio A I2S Option (PTF)
- GPIO_J2_65(PTF), GPIO_J2_67(PTF)
- MIPI DSI
- SD_A_RST, SD_A_WP, SD_A_CD
- SPI_A

4.9.1 MIPI-DSI Interface

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
J1	17	DISP_A_CLK_P	DSI1_CLK_P	O	1.8V	
J1	19	DISP_A_CLK_N	DSI1_CLK_N	O	1.8V	
J1	23	DISP_A_DATA0_P	DSI1_D0_P	O	1.8V	
J1	25	DISP_A_DATA0_N	DSI1_D0_N	O	1.8V	
J1	29	DISP_A_DATA1_P	DSI1_D1_P	O	1.8V	
J1	31	DISP_A_DATA1_N	DSI1_D1_N	O	1.8V	
J1	35	DISP_A_DATA2_P	DSI1_D2_P	O	1.8V	
J1	37	DISP_A_DATA2_N	DSI1_D2_N	O	1.8V	
J1	41	DISP_A_DATA3_P	DSI1_D3_P	O	1.8V	
J1	43	DISP_A_DATA3_N	DSI1_D3_N	O	1.8V	

Table 14: MIPI DSI Interface

4.9.2 RGB Interface

Refer to the CPU documentation for details of the color coding of the RGB Signals.

	Pin	Function	CPU Pad	I/O	Voltage	Remarks
J1	23	DISP_A_DATA0_P	PTF27	O	3.3V	RGB_DE
J1	52	GPIO_J1_52	PTF26	I/O	3.3V	RGB_HSYNC
J1	54	GPIO_J1_54	PTF25	I/O	3.3V	RGB_VSYNC
J1	25	DISP_A_DATA0_N	PTF24	O	3.3V	RGB_CLK
J1	31	DISP_A_DATA1_N	PTF23	O	3.3V	RGB_D00
J1	29	DISP_A_DATA1_P	PTF22	O	3.3V	RGB_D01
J1	37	DISP_A_DATA2_N	PTF21	O	3.3V	RGB_D02
J1	35	DISP_A_DATA2_P	PTF20	O	3.3V	RGB_D03
J1	19	DISP_A_CLK_N	PTF19	O	3.3V	RGB_D04
J1	17	DISP_A_CLK_P	PTF18	O	3.3V	RGB_D05
J1	43	DISP_A_DATA3_N	PTF17	O	3.3V	RGB_D06
J1	41	DISP_A_DATA3_P	PTF16	O	3.3V	RGB_D07
J1	55	DISP_B_DATA0_N	PTF15	O	3.3V	RGB_D08
J1	53	DISP_B_DATA0_P	PTF14	O	3.3V	RGB_D09
J1	61	DISP_B_DATA1_N	PTF13	O	3.3V	RGB_D10
J1	59	DISP_B_DATA1_P	PTF12	O	3.3V	RGB_D11
J1	67	DISP_B_DATA2_N	PTF11	O	3.3V	RGB_D12
J1	65	DISP_B_DATA2_P	PTF10	O	3.3V	RGB_D13
J1	49	DISP_B_CLK_N	PTF9	O	3.3V	RGB_D14
J1	47	DISP_B_CLK_P	PTF8	O	3.3V	RGB_D15
J1	73	DISP_B_DATA3_N	PTF7	O	3.3V	RGB_D16
J1	71	DISP_B_DATA3_P	PTF6	O	3.3V	RGB_D17
J2	96	SD_B_DATA1	PTF5	O	3.3V	RGB_D18
J2	94	SD_B_DATA0	PTF4	O	3.3V	RGB_D19
J2	67	GPIO_J2_67	PTF3	O	3.3V	RGB_D20
J2	65	GPIO_J2_65	PTF2	O	3.3V	RGB_D21
J1	7	GPIO_J1_7	PTF1	O	3.3V	RGB_D22
J1	2	GPIO_J1_2	PTF0	O	3.3V	RGB_D23

Table 15: RGB Interface

4.9.3 Display Control Signals

	Pin	Default Function	Internal Pad	I/O	Voltage	Remarks
J1	9	BL_ON	PTF28	O	3.3V	Display Backlight Enable
J1	11	BL_PWM	PTF29	O	3.3V	Display Backlight PWM
J1	13	VLCD_ON	PTF30	O	3.3V	Display Power Enable

Table 16: Display Control Signals

4.10 Camera Serial Interface (MIPI-CSI)

The module supports up to one dual-lane MIPI-CSI interface.

Pin		Signal	CPU Pad	I/O	Voltage	Remarks
MIPI-CSI Channel A						
J1	74	CSI_CLK_P	CSI_CLK_P	I	1.8V	
J1	76	CSI_CLK_N	CSI_CLK_N	I	1.8V	
J1	80	CSI_DATA0_P	CSI_DATA0_P	I	1.8V	
J1	82	CSI_DATA0_N	CSI_DATA0_N	I	1.8V	
J1	86	CSI_DATA1_ P	CSI_DATA1_P	I	1.8V	
J1	88	CSI_DATA1_ N	CSI_DATA1_N	I	1.8V	
J1	80	CSI_DATA2_P	N.C.	N.C.	-	Only two lanes. Not connected.
J1	82	CSI_DATA2_N	N.C.	N.C.	-	Only two lanes. Not connected.
J1	86	CSI_DATA3_ P	N.C.	N.C.	-	Only two lanes. Not connected.
J1	88	CSI_DATA3_ N	N.C.	N.C.	-	Only two lanes. Not connected.

Table 17: MIPI CSI Interface

4.11 WLAN and Bluetooth Interface

The PicoCore™MX8ULP contains a certified high performance WI-FI 6 and Bluetooth 5.2 module.

The module is based on NXP IW611 chip, having Europe (RED), US (FCC), Canada (ISED), Japan (Giteki) certificates. Please contact support@fs-net.de for additional information about process of certification.

The module offers:

- IEEE802.11 ax/ac/a/b/g/n
- Bluetooth 5.2 BR/EDR and LE long range (supports low Energy)

Note: In case WLAN/BT module is mounted the external SD card interface (SD_A) is not available.

4.12 GPIO / PWM

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-up's or pull-down's are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

	Pin	Standard	CPU Pad	I/O	Voltage	Remarks
J1	2	GPIO_J1_2	PTF0	I/O	3.3V	2nd Fctn: RGB_D23 ⓘ 4.9 Display Interface
J1	7	GPIO_J1_7	PTF1	I/O	3.3V	2nd Fctn: RGB_D22 ⓘ 4.9 Display Interface
J1	44	GPIO_J1_44	PTA0	I/O	3.3V	2nd Fctn: CAN_B_TX 3rd Fctn: WLAN_WAKE ⓘ 4.6 CAN Interface
J1	46	GPIO_J1_46	PTA24	I/O	3.3V	2nd Fctn: CAN_B_RX 3rd Fctn: BT_WAKE ⓘ 4.6 CAN Interface
J1	52	GPIO_J1_52	PTF26	I/O	3.3V	2nd Fctn: RGB_HSYNC ⓘ 4.9 Display Interface
J1	54	GPIO_J1_54	PTF25	I/O	3.3V	2nd Fctn: RGB_ VSYNC ⓘ 4.9 Display Interface
J2	63	PWM	PTC12	O	3.3V	
J2	65	GPIO_J2_65	PTC10 2nd Fctn: PTF2	I/O	3.3V	AUDIO_B_I2S_MCLK ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio 2nd Fctn: RGB_D21 ⓘ 4.9 Display Interface
J2	67	GPIO_J2_67	PTC9 2nd Fctn: PTF3	I/O	3.3V	AUDIO_B_I2S_TXFS ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio2nd Fctn: RGB_D20 ⓘ 4.9 Display Interface
J2	69	GPIO_J2_69	PTC8	I/O	3.3V	AUDIO_B_I2S_TXC ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio
J2	73	GPIO_J2_73	PTC7	I/O	3.3V	AUDIO_B_I2S_TXD ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio
J2	75	GPIO_J2_75	PTC4	I/O	3.3V	AUDIO_B_I2S_RXD

						ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio
J2	77	GPIO_J2_77	PTC3	I/O	3.3V	AUDIO_B_I2S_RXFS ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio
J2	79	GPIO_J2_79	PTC2	I/O	3.3V	AUDIO_B_I2S_RXC ⓘ 4.8 Audio The PicoCore™MX8ULP module can support two audio interfaces. Audio
J2	83	GPIO_J2_83	PTC16	I/O	3.3V	SPI_C_SS0
J2	85	GPIO_J2_85	PTC14	I/O	3.3V	SPI_C_MISO
J2	87	GPIO_J2_87	PTC13	I/O	3.3V	SPI_C_MOSI
J2	89	GPIO_J2_89	PTC15	I/O	3.3V	SPI_C_SCLK
J2	84	SD_B_RST	PTC0	I/O	3.3V	No SD Card B Interface
J2	86	SD_B_WP	PTC1	I/O	3.3V	No SD Card B Interface
J2	88	SD_B_CD	PTC5	I/O	3.3V	No SD Card B Interface
J2	90	SD_B_CMD	PTC6	I/O	3.3V	No SD Card B Interface
J2	92	SD_B_CLK	PTC11	O	3.3V	No SD Card B Interface
J2	94	SD_B_DATA0	PTF4	I/O	3.3V	No SD Card B Interface 2nd Fctn: RGB_D19 ⓘ 4.9 Display Interface
J2	96	SD_B_DATA1	PTF5	I/O	3.3V	No SD Card B Interface 2nd Fctn: RGB_D18 ⓘ 4.9 Display Interface
J2	98	SD_B_DATA2	PTC18	I/O	3.3V	No SD Card B Interface
J2	100	SD_B_DATA3	PTC19	I/O	3.3V	No SD Card B Interface

Table 18: GPIO Interface

For the alternative usages of all Pins please refer to GPIO Reference Card.

4.13 ADC

The NXP i.MX8 ULP offer 2x 12bit ADC. Please see i.MX 8ULP Processor Reference Manual and Data Sheet for detailed pin descriptions.

For questions please contact F&S sales department.

4.14 JTAG

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	93	JTAG_TCK	PTA21	I	3.3V	
J2	95	JTAG_TMS	PTA20	I	3.3V	
J2	97	JTAG_TDI	PTA23	I	3.3V	
J2	99	JTAG_TDO	PTA22	O	3.3V	

Table 19: JTAG Interface

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

4.15 Power and Power Control Pins

	Pin	Signal	I/O	Description
J2	24 26 28	VDD_VIN	I	Main Power supply input please refer chapter 0 Electrical characteristic
J2	30 32 34	GND[*5]	I	Main Power supply Ground input
J2	36	VDD_VBAT[*1]	I	RTC battery input; tie to 3.0V please refer chapter 0 Electrical characteristic
J2	40	VDD_3V3[*2]	O	20mA output from on module DCDC powered from VDD_VIN
J2	52	SD_A_VCC	I	SDHC power output; 3.3V or 1.8V; max 150mA
J2	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J2	41	USB_HOST_VBUS	I	USB Phy voltage input; 5V
J2	42	RESET_IN[*3]	I	Power on reset input; 100k Pull-Up to 1.8V
J2	44	PMIC_STBY[*4]	O	Active high for going to SUSPEND state
J2	46	PMIC_ON_REQ	O	Active high for going to RUN state
J2	48	ON_OFF	I	CPU On/Off control pin, can be used with an external button. A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
J2	2	AUDIO_A_VCC	I	External supply for audio codec; 3~3.3V – 5mA

Table 20: Power and Power Control

[*1] By using a battery for VBAT the regulation rules have to be followed. Please check with your test laboratory. It's possible to use a supercap instead.

[*2] VDD_3V3 is the 3.3V @20mA power supply of the module generated from PMIC and powered from VDD_VIN. Can be used as an "Enable Signal" for the power regulators on baseboard. Please do not use VDD_3V3 pin as a power supply for carrier board.

[*3] RESET_IN is a Reset Input for the module. Will just reset the CPU. Button or an Open Collector/Open Drain output will restart the CPU. On power fail VDD_VIN has to be switched off and on to avoid latch up effects.

[*4] PMIC_STBY is going to high, if the CPU is going in standby. This allows switch of peripheral functions and save more power. Wakeup needs support by the driver, you have to check.

[*5] The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

5 Boot Mode

The CPU of PicoCore™ has fuses to configure the default boot device. By default it is eMMC.

With pin 50 of J2 “BOOTSEL” it is possible to switch between “boot from internal fuses” and “boot from USB serial download”.

So you have the following two boot options:

Boot Device Select	BOOTSEL pin of PicoCore™
Boot from internal fuses	Leave open
USB Serial Download	Connect to GND

Table 21: Boot Modes of PicoCore™

6 Flash

6.1 eMMC Flash

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

The eMMC can be configured to pseudo SLC mode to increase the erase cycles and data retention.

The PicoCore™MX8ULP module can support up to 64GB eMMC flash memory.

7 Real Time Clock (RTC)

There is a NXP PCF85263ATL or a compatible RTC component implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD+0.3	V
Input Voltage range 1.8V IO pins	-0.3	2.15	V
Voltage on any IO with VIN off		0.3	V
USB_*_VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 22: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
+5VS	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_*_VBUS	USB supply voltage		4.5	5.5	
OVDD	On module 3.3V DCDC		3.15	3.45	V
VDD_3V3	3.3V output for power enable on carrier board		OVDD	OVDD	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

Table 23: DC Electrical Characteristics

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Description	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top **(Ψ_{JT})**		0.98		°C/W

Table 24: Thermal Specs

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. Cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

10 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMC Implementing

Like all other COM modules on the market there is no ESD protection on any signal out from the COM module. ESD protection has to be placed as near as possible to the ESD source - this is the connector with external access on the COM baseboard.

A helpful guide is available from TI: ESD Protection Layout Guide

The module supports spread spectrum in order to reduce the electromagnetic interference (EMI). This will normally reduce the EMI between 9 and 12 dB and so this can decrease your shielding requirements. We highly recommend to have controlled impedances and wires as short as possible in your layout designs.

12 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power Consumption and Cooling

Depending on your product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d.** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d.** and **t.b.d.** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

For the optimal cooling performance we recommend to use F&S heat spreader set MHS.PC100.1. For more information please contact with us.

14 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

15 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags. The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 10: Matrix Code Sticker

18 Appendix

Important Notice

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