Hardware Documentation

NetDCU™A7

Version 1.00
(2023-03-29)

Elektronik Systeme

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About This Document

This document describes how to use the NetDCU™A7 board with mechanical and electrical information. The latest version of this document can be found at:

https://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
18.12.2023	1				Initial Release	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block diagram

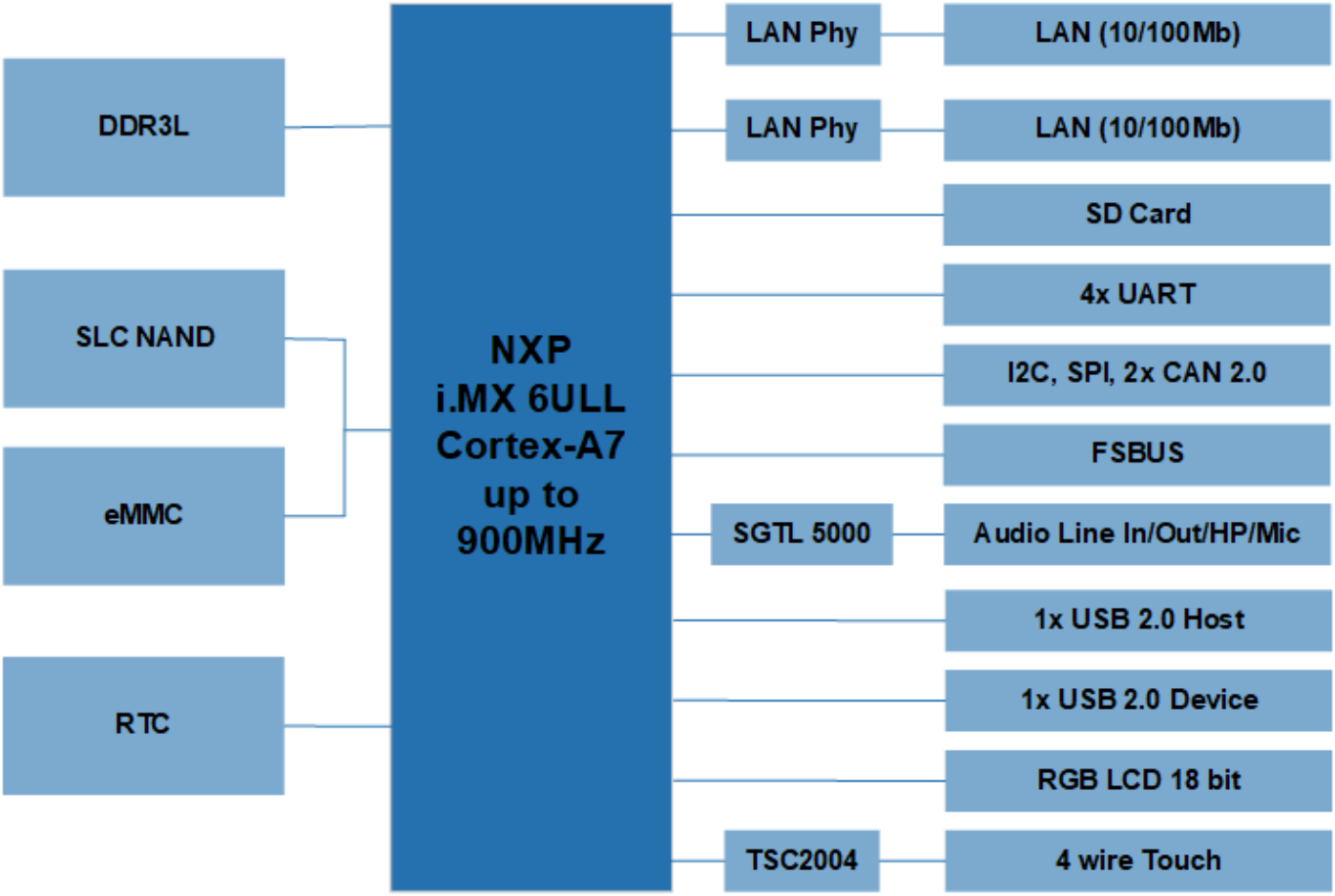

Figure 1: Block Diagram

2 Connector Layout

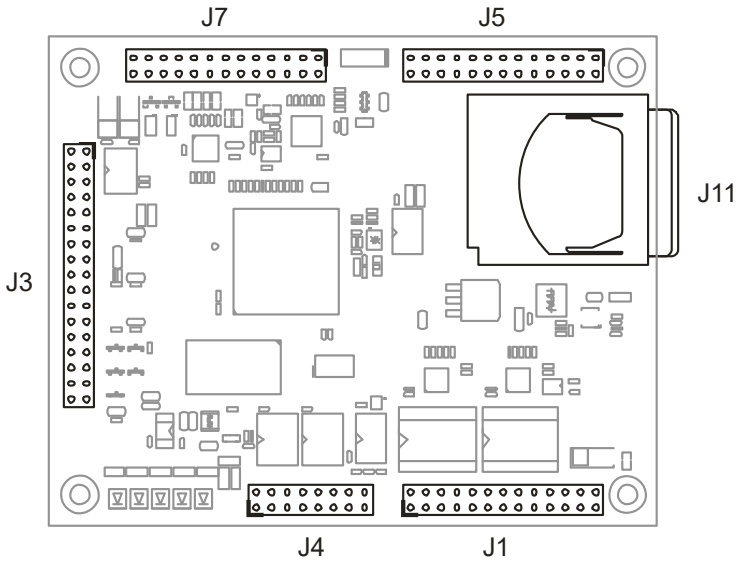

Figure 2: Connector Layout Top

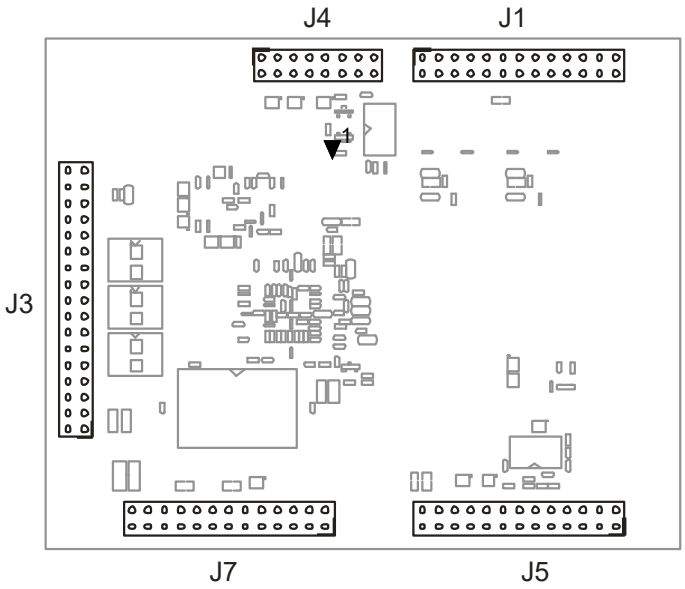

Figure 3: Connector Bottom

Dimensions	Description
Size	100mm x 80mm
PCB Thickness	1.6mm ± 0.1mm
Height of the parts on the top side	Max. 7mm
Height of the parts on the bottom side	Max. 9mm
Weight	45gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 Counting of the connector pins

All connections prepared for two-row connectors on the NetDCUA7 are treated as follows.

The row with pin 1 contains all odd-numbered pins (1, 3, 5, 7, etc.), and, corresponding to this, the row without pin 1 contains all even-numbered pins (2, 4, 6, 8, etc.).

Pin 1 is marked with a small triangle on the PCB

3.2 Connector types

Connectors J1, J3, J4, J5, and J7 are 2.54mm pitch dual row holes for THT connectors.

All of them are on the same 2.54mm grid.

Customer specific connectors can be soldered by F&S.

Ask sales (sales@fs-net.de) for a quote.

3.3 J1

J1 on NetDCUA7 combines J1 and J2 on older NetDCUs.

	Pin	Signal	CPU Pad	I/O	Voltage	Pins on older NetDCU	Remarks
J1	1	LAN1_RX+	-	I/Odiff		J2 Pin2	
J1	2	LAN1_RX-	-	I/Odiff		J2 Pin1	
J1	3	RTS0	UART3_TX_DATA	O	TTL/RS232	J2 Pin4	
J1	4	RXD0	UART2_RX_DATA	I	TTL/RS232	J2 Pin3	
J1	5	CTS0	UART3_RX_DATA	I	TTL/RS232	J2 Pin6	
J1	6	TXD0	UART2_TX_DATA	O	TTL/RS232	J2 Pin5	
J1	7	LAN1_TX+	-	I/Odiff		J2 Pin8	
J1	8	LAN1_TX-	-	I/Odiff		J2 Pin7	
J1	9	V50-OUT	-	O	5.0V	J2 Pin10	
J1	10	GND		PWR	-	J2 Pin9	
J1	11	CAN1-TX	UART3_CTS	O	5.0V	J2 Pin12	
J1	12	CAN1-RX	UART3_RTS	I	5.0V	J2 Pin11	
J1	13	CAN2-TX	UART2_CTS	O	5.0V	-	
J1	14	CAN2-RX	UART2_RTS	I	5.0V	-	
J1	15	LAN2_RX+	-	I/Odiff		-	
J1	16	LAN2_RX-	-	I/Odiff		-	
J1	17	LAN2_TX+	-	I/Odiff		-	
J1	18	LAN2_TX-	-	I/Odiff		-	
J1	19	VCFL-IN		PWR	5.0 – 20V	J1 Pin1	
J1	20	n.c.	-	-	-	J1 Pin2	
J1	21	V50-IN		PWR	5.0V	J1 Pin3	
J1	22	V50-IN		PWR	5.0V	J1 Pin4	
J1	23	VBAT		PWR	3.0V	J1 Pin5	
J1	24	n.c.	-		-	J1 Pin6	
J1	25	GND		PWR	-	J1 Pin7	
J1	26	GND		PWR	-	J1 Pin8	

3.4 J3 RGB Interface

To use the LCD Signals as GPIOs please contact our support team. Not all pin connected directly from the CPU to the connector. Mounting options are possible.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J3	1	GND		PWR	-	
J3	2	R3	LCD_DATA01	O	3.3V	LCD R3
J3	3	R2	LCD_DATA00	O	3.3V	LCD R2(LSB)
J3	4	G7	LCD_DATA11	O	3.3V	LCD G7(MSB)
J3	5	G6	LCD_DATA10	O	3.3V	LCD G6
J3	6	G5	LCD_DATA09	O	3.3V	LCD G5
J3	7	G4	LCD_DATA08	O	3.3V	LCD G4
J3	8	GND		PWR	-	
J3	9	B5	LCD_DATA15	O	3.3V	LCD B5
J3	10	B4	LCD_DATA14	O	3.3V	LCD B4
J3	11	B3	LCD_DATA13	O	3.3V	LCD B3
J3	12	B2	LCD_DATA12	O	3.3V	LCD B2(LSB)
J3	13	G3	LCD_DATA07	O	3.3V	LCD G3
J3	14	G2	LCD_DATA06	O	3.3V	LCD G2(LSB)
J3	15	B7	LCD_DATA17	O	3.3V	LCD B7(MSB)
J3	16	B6	LCD_DATA16	O	3.3V	LCD B6
J3	17	GND		PWR	-	
J3	18	VEEK	GPIO1_IO04	O	3.3V	Backlight dimming Voltage (0..3.3V)
J3	19	CLK	LCD_CLK	O	3.3V	LCD Clock
J3	20	VSNCY	LCD_VSYNC	O	3.3V	LCD VSYNC
J3	21	DE	LCD_ENABLE	O	3.3V	LCD Data Enable
J3	22	HSYNC	LCD_HSYNC	O	3.3V	LCD HSYNC
J3	23	DEN	-	O	3.3V	Display On Signal
J3	24	GND		PWR	-	
J3	25	VLCD	-	PWR	3.3V	Display voltage (3.3/5.0V) set with Jumper J1 and J2
J3	26	n.n.	-	-	-	
J3	27	n.n.	-	-	-	
J3	28	GND		PWR	-	
J3	29	n.n.	-	-	-	
J3	30	VCFL	-	PWR	5.0 – 20.0V	Switched Backlight Voltage from J1
J3	31	R4	LCD_DATA02	O	3.3V	LCD R4

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J3	32	R5	LCD_DATA03	O	3.3V	LCD R5
J3	33	R6	LCD_DATA04	O	3.3V	LCD R6
J3	34	R7	LCD_DATA05	O	3.3V	LCD R7(MSB)

3.5 J4 FS-Bus (8 bit Extension interface)

All I/O's have an onboard 4.7kΩ Pull-Up to VIO.

FS-Bus voltage can be 3.3V or 5.0V depending on configuration.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J4	1	D0	CSI_DATA00	I/O	3.3/5.0V	Data Bit D0
J4	2	D1	CSI_DATA01	I/O	3.3/5.0V	Data Bit D1
J4	3	D2	CSI_DATA02	I/O	3.3/5.0V	Data Bit D2
J4	4	D3	CSI_DATA03	I/O	3.3/5.0V	Data Bit D3
J4	5	D4	CSI_DATA04	I/O	3.3/5.0V	Data Bit D4
J4	6	D5	CSI_DATA05	I/O	3.3/5.0V	Data Bit D5
J4	7	D6	CSI_DATA06	I/O	3.3/5.0V	Data Bit D6
J4	8	D7	CSI_DATA07	I/O	3.3/5.0V	Data Bit D7
J4	9	VIO	-	PWR	3.3/5.0V	IO Voltage Out
J4	10	RD	CSI_VSYNC	O	3.3/5.0V	Read Output, Active High
J4	11	nCS	CSI_MCLK	O	3.3/5.0V	Chip Select, Active Low
J4	12	ADE	NAND_CE1	O	3.3/5.0V	Address Enable, Active High
J4	13	nIRQ	NAND_DQS	I	3.3/5.0V	Interrupt, Active Low
J4	14	nRES	-	I	3.3/5.0V	Reset, Active Low
J4	15	PWM	CSI_HSYNC	O	3.3/5.0V	
J4	16	GND		PWR	-	

3.6 J5 GPIO

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J5	1	GPIO_J5_1	SNVS_TAMPER5	I/O	3.3V	
J5	2	ROW7	GPIO1_IO01 / LCD_DATA23	I/O	3.3V	
J5	3	ROW6	GPIO1_IO00 / LCD_DATA22	I/O	3.3V	
J5	4	ROW5	SNVS_TAMPER9	I/O	3.3V	
J5	5	ROW4	SNVS_TAMPER8	I/O	3.3V	
J5	6	ROW3	SNVS_TAMPER7	I/O	3.3V	
J5	7	ROW2	SNVS_TAMPER6	I/O	3.3V	
J5	8	ROW1	SNVS_TAMPER1	I/O	3.3V	
J5	9	ROW0	SNVS_TAMPER0	I/O	3.3V	
J5	10	COL8 / I2C2-DAT / SPI0-MISO	GPIO1_IO01 / LCD_DATA23	I/O	3.3V	4,7kΩ Pull-Up
J5	11	COL9 / I2C2-CLK / SPI0-MOSI	GPIO1_IO00 / LCD_DATA22	I/O	3.3V	4,7kΩ Pull-Up
J5	12	RXD1	UART5_RX_DATA	I	RS232 / TTL	
J5	13	COL10 / SPI0-CS0	LCD_DATA21	I/O	3.3V	4,7kΩ Pull-Up
J5	14	TXD1	UART5_TX_DATA	O	RS232 / TTL	
J5	15	COL11 /SPI0-CLK	LCD_DATA20	I/O	3.3V	
J5	16	GND		PWR	-	
J5	17	COL7	GPIO1_IO09	I/O	3.3V	4,7kΩ Pull-Up
J5	18	COL6	GPIO1_IO08	I/O	3.3V	4,7kΩ Pull-Up
J5	19	COL5	GPIO1_IO05	I/O	3.3V	4,7kΩ Pull-Up
J5	20	COL4	GPIO1_IO03	I/O	3.3V	4,7kΩ Pull-Up
J5	21	COL3	CSI_PIXCLK	I/O	3.3V	4,7kΩ Pull-Up
J5	22	COL2	LCD_DATA19	I/O	3.3V	4,7kΩ Pull-Up
J5	23	COL1	LCD_DATA18	I/O	3.3V	4,7kΩ Pull-Up
J5	24	COL0	LCD_RESET	I/O	3.3V	4,7kΩ Pull-Up
J5	25	V50-OUT		PWR	5.0V	
J5	26	V33-OUT		PWR	3.3V	

3.7 J7

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J7	1	LINEOUT-L	-	O		
J7	2	LINEOUT-R	-	O		
J7	3	GND		PWR		
J7	4	LINEIN-L	-	I		
J7	5	LINEIN-R	-	I		
J7	6	GND		PWR		
J7	7	MIC	-	I		
J7	8	MICBIAS	-	I		
J7	9	RXD2 / AD2	UART1_RX_DATA / (ADS1015 AIN2)	I		
J7	10	TXD2 / AD3	UART1_TX_DATA / (ADS1015 AIN3)	I/O		
J7	11	AD0	(ADS1015 AIN0)	I		
J7	12	AD1	(ADS1015 AIN1)	I		
J7	13	V50-OUT		PWR	5.0V	
J7	14	GND		PWR		
J7	15	TOUCH X+	(TSC2004 X+)	I		
J7	16	TOUCH Y+	(TSC2004 Y+)	I		
J7	17	TOUCH X-	(TSC2004 X-)	I		
J7	18	TOUCH Y-	(TSC2004 Y-)	I		
J7	19	V33-OUT		PWR O	3.3V	
J7	20	GND		PWR		
J7	21	USBD-	USB_OTG1_DN	I/Od iff		
J7	22	USBD+	USB_OTG1_DP	I/Od iff		
J7	23	USBH-	USB_OTG2_DN	I/Od iff		
J7	24	USBH+	USB_OTG2_DP	I/Od iff		
J7	25	USBD Detect	USB_OTG1_VBUS	I	5.0V	
J7	26	USBH Detect / Power	USB_OTG2_VBUS / -	O	5.0V	

4 SD Card

The NetDCUA7 offers a SD Card Slot.

For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

5 Interfaces

5.1 J7 USB Host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J7	23	USBH-	USB_OTG2_DN	I/O		90 Ohm differential pair; Preferred for host
J7	24	USBH+	USB_OTG2_DP	I/O		
J7	26	USBH Detect / Power	USB_OTG2_VBUS / -	O	5.0V	Power enable

Table 2: USB Host Interface

5.2 USB OTG

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	25	USBD Detect	USB_OTG1_VBUS	I	5.0V	Input
J2	22	USBD+	USB_OTG1_DP	I/O		90 Ohm differential pair
J2	21	USBD-	USB_OTG1_DN	I/O		

Table 3: USB Device Interface

5.3 SPI

The module support HS SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on base-board with other voltage need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*1	MM*1	Voltage	Description
J5	13	SPI0_CS0	LCD_DATA21	I	O	3.3V	
J5	10	SPI0_MISO	LCD_DATA23	O	I	3.3V	Shared with I2C
J5	11	SPI0_MOSI	LCD_DATA22	I	O	3.3V	Shared with I2C
J5	15	SPI0_CLK	LCD_DATA20	I	O	3.3V	

*1: SM: Slave Mode, MM: Master Mode

Table 4: SPI Interface

5.4 I2C

The module supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J5	10	I2C2_SDA	GPIO1_IO01	I/O	3.3V	onboard pull-up 4,7k; shared with SPI
J5	11	I2C2_SCL	GPIO1_IO00	I/O	3.3V	onboard pull-up 4,7k; shared with SPI

Table 5: I2C Interface

5.5 Serial ports

	Pin	Signal	CPU Pad	I/O	Level	Description
J5	12	RXD1	UART5_RX_DATA	I	RS232 / TTL	Reserved for debug
J5	13	TXD1	UART5_TX_DATA	O	RS232 / TTL	Reserved for debug
J1	3	RTS0	UART3_TX_DATA	O	RS232 / TTL	
J1	4	RXD0	UART2_RX_DATA	I	RS232 / TTL	
J1	5	CTS0	UART3_RX_DATA	I	RS232 / TTL	
J1	6	TXD0	UART2_TX_DATA	O	RS232 / TTL	
J7	9	RXD2	UART1_RX_DATA	I	RS232 / TTL	
J7	10	TXD2	UART1_TX_DATA	O	RS232 / TTL	

Table 6: UART A Interface

We recommend to use UART_A for debugging and service only.

F&S standard software uses DCE mode for UART.

5.6 Ethernet

The NetDCU offers two 10/100Mbit Ethernet Ports

	Pin	Signal	KSZ8081 Pad	I/O	Remarks	RJ45 Pin
J1	1	LAN1_RX+	RXP	I/O	Ethernet 1 RX Data+	3
J1	2	LAN1_RX-	RXN	I/O	Ethernet 1 RX Data-	6
J1	7	LAN1_TX+	TXP	I/O	Ethernet 1 TX Data+	1
J1	8	LAN1_TX-	TXN	I/O	Ethernet 1 TX Data-	2
J1	15	LAN2_RX+	RXP	I/O	Ethernet 2 RX Data+	3
J1	16	LAN2_RX-	RXN	I/O	Ethernet 2 RX Data-	6
J1	17	LAN2_TX+	TXP	I/O	Ethernet 2 TX Data+	1
J1	18	LAN2_TX-	TXN	I/O	Ethernet 2 TX Data-	2

Table 7: 2x 10/100Mbit Ethernet Interface

Connect directly to RJ45 connector

The intra pair mismatch of each differential pair should be <50 mil (1.27mm).

Please also refer our "Ethernet Routing Guidelines" on our web download area and refer the comments at our forum.

Ethernet 2 is optional and not mounted in all configurations. Please contact sales to get more information.

5.7 Audio

The audio codec NXP SGTL5000 is mounted on the module.

	Pin	Signal	I/O	Description
J7	1	LINEOUT-L	O	Audio Line Out Left
J7	2	LINEOUT-R	O	Audio Line Out Right
J7	4	LINEIN-L	I	Audio Line In Left
J7	5	LINEIN-R	I	Audio Line In Right
J7	7	MIC	I	Microphone In
J7	8	MICBIAS	I	Microphone Bias Voltage

Table 8: Audio Interface

5.8 Digital RGB

To use the LCD Signals as GPIOs please contact our support team. Not all pin connected directly from the CPU to the connector. Mounting options are possible.

All signals can work with 3.3V or 5.0V logic level.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J3	1	GND		PWR	-	
J3	2	R3	LCD_DATA01	O	3.3/5.0V	LCD R3
J3	3	R2	LCD_DATA00	O	3.3/5.0V	LCD R2(LSB)
J3	4	G7	LCD_DATA11	O	3.3/5.0V	LCD G7(MSB)
J3	5	G6	LCD_DATA10	O	3.3/5.0V	LCD G6
J3	6	G5	LCD_DATA09	O	3.3/5.0V	LCD G5
J3	7	G4	LCD_DATA08	O	3.3/5.0V	LCD G4
J3	8	GND		GND	-	
J3	9	B5	LCD_DATA15	O	3.3/5.0V	LCD B5
J3	10	B4	LCD_DATA14	O	3.3/5.0V	LCD B4
J3	11	B3	LCD_DATA13	O	3.3/5.0V	LCD B3
J3	12	B2	LCD_DATA12	O	3.3/5.0V	LCD B2(LSB)
J3	13	G3	LCD_DATA07	O	3.3/5.0V	LCD G3
J3	14	G2	LCD_DATA06	O	3.3/5.0V	LCD G2(LSB)
J3	15	B7	LCD_DATA17	O	3.3/5.0V	LCD B7(MSB)
J3	16	B6	LCD_DATA16	O	3.3/5.0V	LCD B6
J3	17	GND		PWR	-	
J3	18	VEEK	GPIO1_IO04	O	3.3/5.0V	Backlight dimming Voltage (0..3.3V)
J3	19	CLK	LCD_CLK	O	3.3/5.0V	LCD Clock
J3	20	VSNCY	LCD_VSYNC	O	3.3/5.0V	LCD VSYNC
J3	21	DE	LCD_ENABLE	O	3.3/5.0V	LCD Data Enable
J3	22	HSYNC	LCD_HSYNC	O	3.3/5.0V	LCD HSYNC
J3	23	DEN	-	O	3.3/5.0V	Display On Signal
J3	24	GND		PWR	-	
J3	25	VLCD	-	PWR	3.3/5.0V	Display voltage (3.3/5.0V) set with Jumper J1 and J2
J3	26	n.n.	-	-	-	
J3	27	n.n.	-	-	-	
J3	28	GND		PWR	-	
J3	29	n.n.	-	-	-	
J3	30	VCFL	-	PWR	5.0 – 20.0V	Switched Backlight Voltage from J1

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J3	31	R4	LCD_DATA02	O	3.3/5.0V	LCD R4
J3	32	R5	LCD_DATA03	O	3.3/5.0V	LCD R5
J3	33	R6	LCD_DATA04	O	3.3/5.0V	LCD R6
J3	34	R7	LCD_DATA05	O	3.3/5.0V	LCD R7(MSB)

Table 9: RGB Interface

Note: Most displays support HSYNC/VSYNC or DE mode. Please be sure just connect only useful signals at same time. The 18bit w/o HSYNC/VSYNC mode needs a special configuration made by software. Please refer the SW manual for this configuration.

5.9 CAN Interface

The module can also support two CAN Interfaces with 5.0V Logic Level.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1	12	CAN1_RX	UART3_RTS	I	5.0V	CAN Receive Data
J1	11	CAN1_TX	UART3_CTS	O	5.0V	CAN Transmit Data
J1	14	CAN2_RX	UART2_CTS	I	5.0V	CAN Receive Data
J1	13	CAN2_TX	UART2_RTS	O	5.0V	CAN Transmit Data

Table 10: CAN Pin Layout

5.10 Touch Interface

The module support a 4-wire Resistive Touch.

	Pin	Signal	I/O	Description
J7	15	TOUCH X+	I	
J7	16	TOUCH Y+	I	
J7	17	TOUCH X-	I	
J7	18	TOUCH Y-	I	

Table 11: Touch Interface

NetDCUA7 use touch controller IC Texas Instruments TSC2004. The TSC2004 is connected via I2C to CPU.

5.11 Analog Input

The module support up to 4 Analog Inputs. The chip ADS1015 from TI is connected via I2C to CPU. AD2 and AD3 is shared with COM3.

	Pin	Signal	ADS1015 Pad	I/O	Voltage	Remarks
J7	11	AD0	AIN0	I	0…3.3V	
J7	12	AD1	AIN1	I	0…3.3V	
J7	9	AD2	AIN2	I	0…3.3V	
J7	10	AD3	AIN3	I	0…3.3V	

Table 12: Analog Input

AD2/3 is optional and not mounted in all configurations. Please contact sales to get more information.

5.12 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it’s not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced IO power is not allowed.

6 Status LEDs

The NetDCUA7 has four LED status indicators.

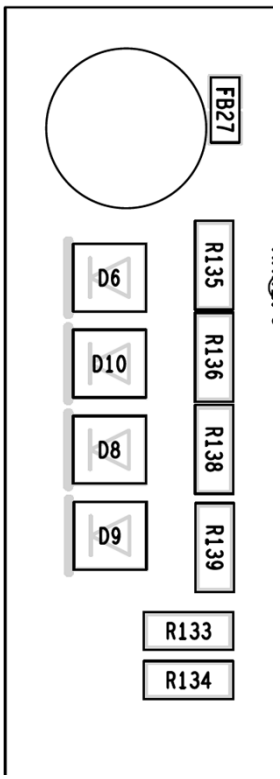

Figure 6.1: Status LED

The following status information's is displayed.

LED	Signal	Description
D9	RUN	CPU in Run-Mode
D8	STA1	Status indication 1 (see Software documentation)
D10	ETH1	Ethernet1 Link and activity status
D6	ETH2	Ethernet2 Link and activity status

Table 13: Status LEDs

7 Configuration

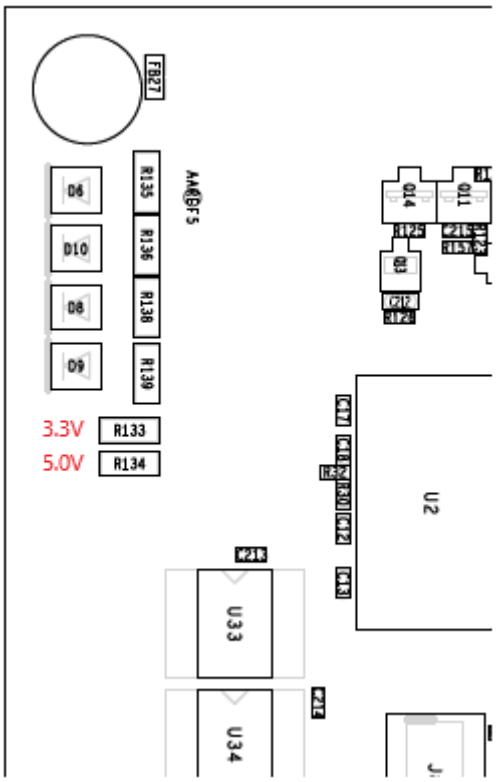

Figure 4: NetDCUA7 Config Resistors

7.1 FS-BUS Interface

The voltage level of the FS-BUS (J4) can be set by jumpers.

Configuration	Resistor
Voltage Level I/O Parallel Interface 3.3V (default)	R133
Voltage Level I/O Parallel Interface 5.0V	R134

Warning: Do not set both resistors at the same time, this will short the power supply and will damage the board.

Jumper: 0 Ohm resistor, size 0805

8 Power and Power Control Pins

	Pin	Signal	I/O	Description
J1	21 22	V50-IN	I	Main Power supply input please refer chapter 11 Electrical characteristic
J1	25 26	GND	I	Main Power supply Ground input
J1	23	VBAT	I	RTC battery input; tie to 3.0V please refer chapter 11 Electrical characteristic
J1	19	VCFL-IN	I	Backlight Input please refer chapter 11 Electrical characteristic
J4	14	RESETIN	I	Power on reset input; 10k PU; 3.3V

Table 14: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

RESETIN is the reset input for the module. RESETIN only resets the CPU. In the event of a power failure, V50-IN must be switched off and on to avoid latch-up effects.

The GND contacts which are given in the table above are the power ground contacts for VDD_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

9 Flash

NetDCUA7 can be shipped with SLC NAND Flash or MLC eMMC. By default fuses of i.MX6ULL CPU are configured so that NetDCUA7 boots from the assembled flash memory.

9.1 NAND Flash

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 16 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system

9.2 eMMC

eMMC can be mounted instead of NAND. An eMMC v4.41 or higher with 4GB or more is mounted from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

10 RTC

There is an external RTC (NXP PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

11 Electrical characteristic

11.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IOs	-0.3	OVDD*+0.3	V
Voltage on any IO with V50-IN off		0.3	V
Maximum power consumption VDD_VBAT at 85°C		0.8	µA
Maximum output current 3.3V*1		100	mA
Maximum output current 5.0V*1		100	mA
Maximum output current VLCD OUT		1	A
Maximum output current VCFL OUT		2	A

Table 15: Absolute Maximum Ratings

*1 Current on all output pins combined

11.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
V50-IN	Module main power		4.5	5.5	V
VBAT	RTC power		0.9	3.6	V
VCFL-IN	Backlight voltage in		3.3	30.0	V
USB_OTG_VBUS	USB supply voltage		4.5	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_SNVS		3.15	3.45	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VBAT			0.22[*1]	µA

Table 16: DC Electrical Characteristics

[*1] Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

12 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top (Ψ_{JT}) – **i.MX6ULL**		0.2		°C /W

Note 1: Maximum junction temperature of the CPU is 95°C /105°C. In this case cooling is necessary and highly recommended for operations near the limits. See also: *Power consumption and cooling*

Please get in contact with F&S for recommended cooling solutions.

Note 2: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN5337 (https://www.nxp.com/docs/en/application-note/AN5337.pdf)

13 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

14 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

15 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

16 Power consumption and cooling

Depend from product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (70°C/85°C).

The maximum power consumption of the board could be **t.b.d**. This value is with 100% working of cores and full working graphic engines.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d** to **t.b.d** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

17 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

18 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59 (1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

19 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

20 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 5: Matrix Code Sticker

21 Appendix

Important Notice

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