Hardware Documentation

FS OSM™-SF-IMX8ULP
for HW Revision 1.00

Preliminary

Version 003
(2024-10-25)

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About This Document

This document describes how to use the FS OSM™-SF-IMX8ULP board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Note:
Please use our schematic review service!

FS OSM-SF-IMX8ULP uses pre series NXP CPU and the module itself is under development.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
18.12.2023	001	All		-	Initial Version	MW
14.02.2024	002	All	M	3, 4.9, 4.10, 4.14, 4.15	Add information about PTF CPU domain voltage	MW
02.04.2024	003	All	M M	2 2.1, 2.3	add information regarding edge overhang mechanical dimensions changed	UK TM
25.10.2024	004	All	M	4.14	Correct table 15	UK TM

V Version
A,M,R Added, Modified, Removed
Au Author

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1 Block Diagram

The picture below shows all interfaces that are compatible with the OSM standard. The maximum number of interfaces varies.

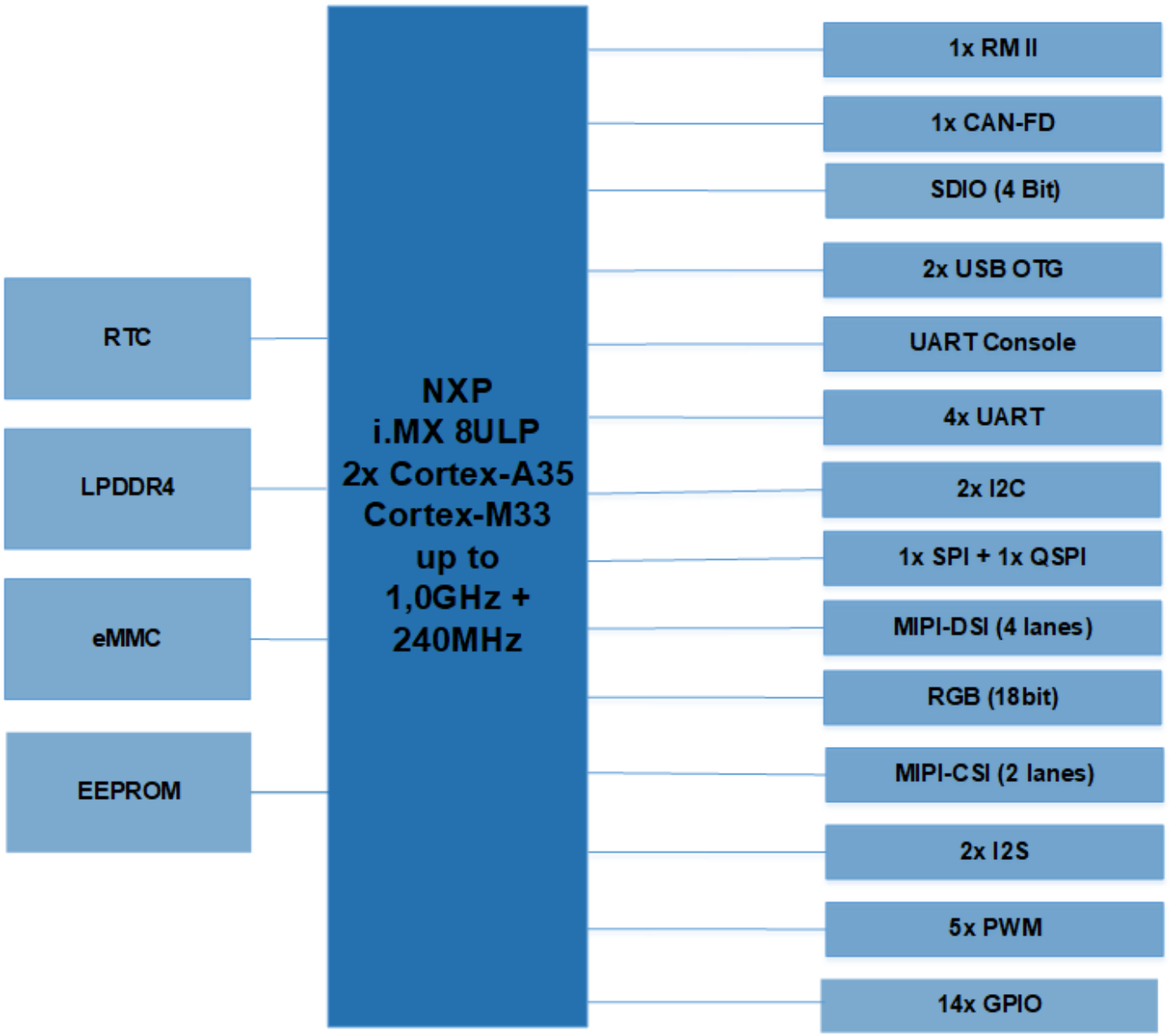
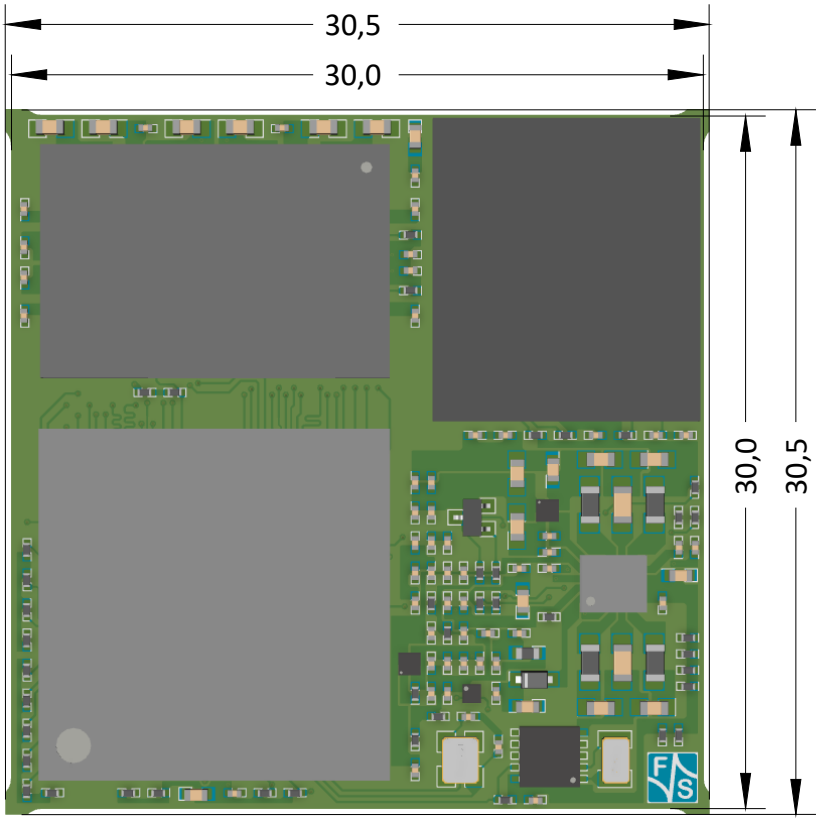


Figure 1: Block diagram

2 Mechanical Dimensions

This OSM module uses single side assembly. So, no cut-out is required on the carrier board. Due to the production process, the modules have an edge overhang which needs to be considered in the design.



all dimensions are in mm

Figure 2: Mechanical Dimensions

Note: Samples may have an overhang, slightly greater than specified above.

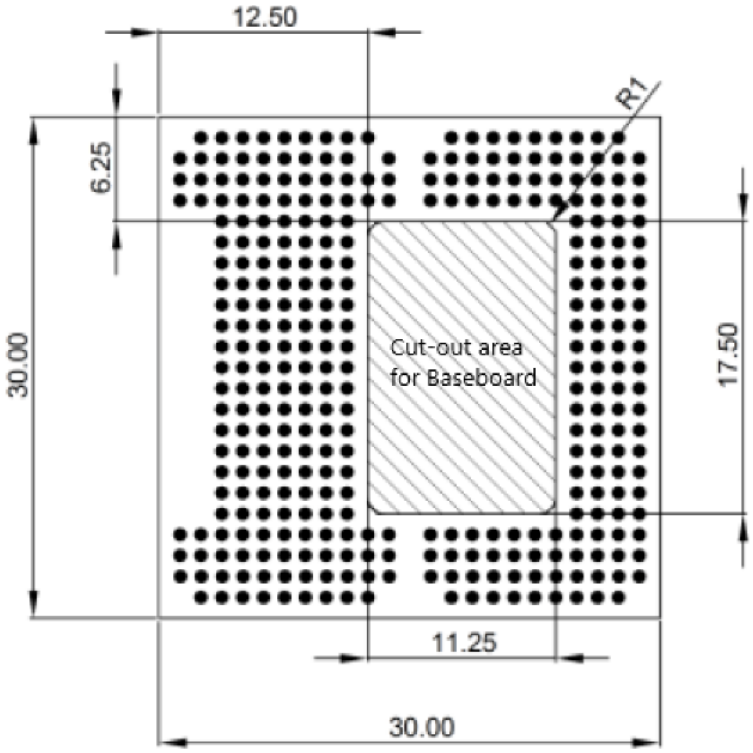


Figure 3: Mechanical Dimensions Bot + cut out area
No Cut-out area is needed for F&S OSM Modules!

Dimensions	Description
Size	30mm x 30mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 1.5mm
Height of the parts on the bottom side	no parts on bottom side
Weight	Max. 14gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

2.1 Heat Spreader

As a base for the cooling concept, F&S offers a heat spreader. Part number of the spreader is **MHS.OSM.1** and can be ordered via F&S web shop. For more information see documentation for MHS.OSM.1.

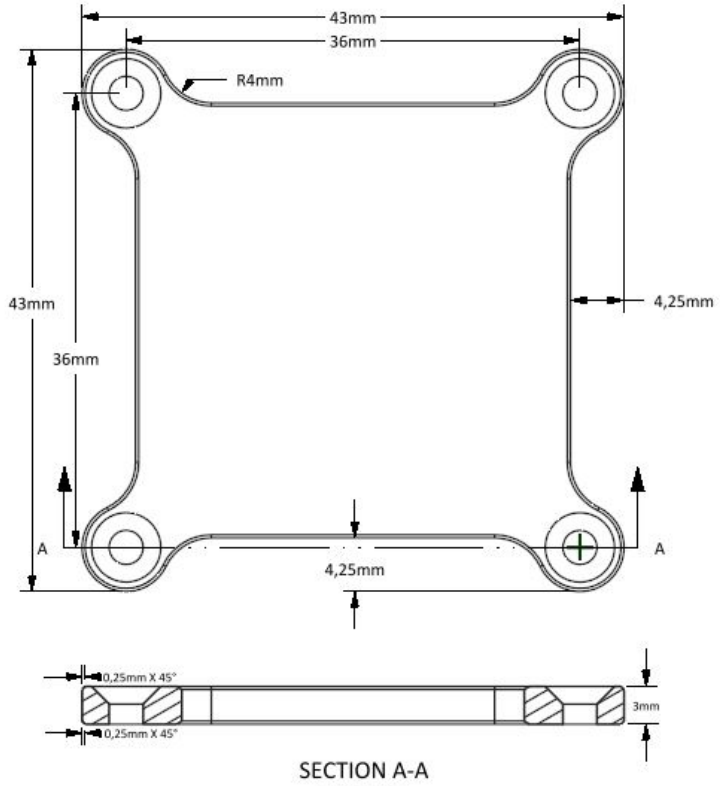


Figure 4: Heat Spreader Mechanical Dimensions

2.2 Recommended Spacer

For mounting we recommend SMT Steel Spacer components, order number **B.MSCHR.34**.
This part is in F&S stock and can be ordered via F&S web shop.
The stack height of the spacer is 3.0mm. If a different stack height is needed, another spacer should be chosen. In this case also the thermal interface material must be adapted.

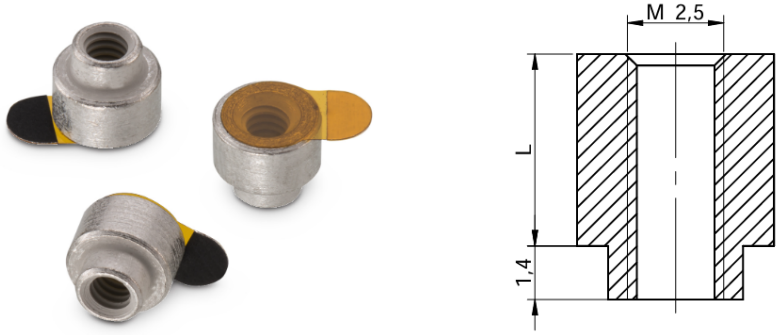


Figure 5: Recommended SMT Steel Spacer

2.3 Recommended Land Pattern

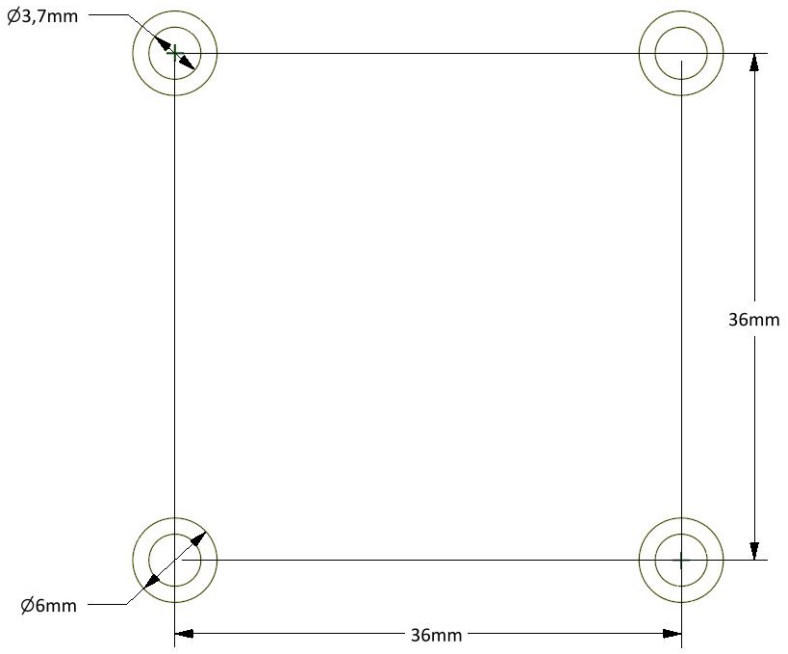


Figure 6: SMT Spacer Recommended Land Pattern

2.4 Stencil Suggestion

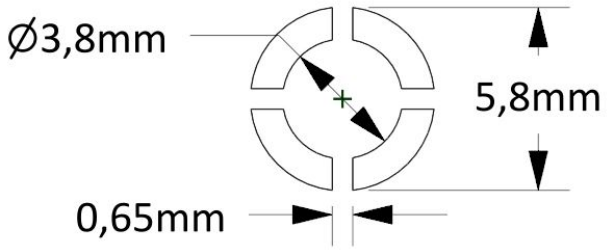


Figure 7: SMT Spacer Stencil Suggestion

3 Interface and Signal Description

3.1 Contact Grid

The FS OSM™-SF-IMX8ULP has to be soldered directly on the carrier board.

The FS OSM™-SF-IMX8ULP is using Fused Tin Grid Array (FTGA) for connecting the module PCB to the baseboard PCB.

All Pins not mentioned below are left unconnected.

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
C2	CAM_MCK	CAM_MCK	PTB12	O	1V8	
G3	CAM_PWR/GPIO_C_	CAM_EN	PTB13	O	1V8	
G4	CAM_RST#/GPIO_C	CAM_RST#	PTB14	O	1V8	
AB17	CAN_A_RX	CAN_A_RX	PTA13	I	1V8	
AC17	CAN_A_TX	CAN_A_TX	PTA12	O	1V8	
V17	CARRIER_PWR_EN	CARRIER_PWR_EN	PTB4	O	1V8	10k pull-down, carrier board circuit should not be powered up until module asserts signal
B3	CSI_CLOCK_N	CSI_CLK_N	CSI_CLK_N	I		
B4	CSI_CLOCK_P	CSI_CLK_P	CSI_CLK_P	I		
C1	CSI_DATA0_N	CSI_D0_N	CSI_DATA0_N	I		
B1	CSI_DATA0_P	CSI_D0_P	CSI_DATA0_P	I		
A2	CSI_DATA1_N	CSI_D1_N	CSI_DATA1_N	I		
A3	CSI_DATA1_P	CSI_D1_P	CSI_DATA1_P	I		
AB8	DSI_CLOCK_N	DSI_CLK_N	DSI_CLK_N	O		
AB7	DSI_CLOCK_P	DSI_CLK_P	DSI_CLK_P	O		
AB11	DSI_DATA0_N	DSI_D0_N	DSI_DATA0_N	O		
AB10	DSI_DATA0_P	DSI_D0_P	DSI_DATA0_P	O		
AC9	DSI_DATA1_N	DSI_D1_N	DSI_DATA1_N	O		
AC8	DSI_DATA1_P	DSI_D1_P	DSI_DATA1_P	O		
AC6	DSI_DATA2_N	DSI_D2_N	DSI_DATA2_N	O		
AC5	DSI_DATA2_P	DSI_D2_P	DSI_DATA2_P	O		
AB5	DSI_DATA3_N	DSI_D3_N	DSI_DATA3_N	O		
AB4	DSI_DATA3_P	DSI_D3_P	DSI_DATA3_P	O		
AA3	DSI_TE	DSI_TE	PTF28	I	1V8 / 3V3[1]	
R15	ETH_A_(R)(G)MII_ RX_CLK	ETH_A_(R)(G)MII_ RX_CLK	PTE19	I	1V8	
M15	ETH_A_(R)(G)MII_ RX_DV(_ER)	ETH_A_(R)(G)MII_ RX_DV(_ER)	PTE18	I	1V8	
L16	ETH_A_(R)(G)MII_ RX_ER	ETH_A_(R)(G)MII_ RX_ER	PTE17	I	1V8	
J15	ETH_A_(R)(G)MII_ TX_CLK	ETH_A_(R)(G)MII_ TX_CLK	PTE3	O	1V8	
K16	ETH_A_(R)(G)MII_ TX_EN(_ER)	ETH_A_(R)(G)MII_ TX_EN(_ER)	PTE16	O	1V8	

Contact	Contact Name	Internal Pad		I/O	Voltage	Remarks
K15	ETH_A_(S)(R)(G)MII_RXD0	ETH_A_(S)(R)(G)MII_RXD0	PTE21	I	1V8	
L15	ETH_A_(S)(R)(G)MII_RXD1	ETH_A_(S)(R)(G)MII_RXD1	PTE20	I	1V8	
H15	ETH_A_(S)(R)(G)MII_TXD0	ETH_A_(S)(R)(G)MII_TXD0	PTE23	O	1V8	
G15	ETH_A_(S)(R)(G)MII_TXD1	ETH_A_(S)(R)(G)MII_TXD1	PTE22	O	1V8	
M17	ETH_IOPWR	V_PTE_F		O	1V8	Output IO voltage for Ethernet on carrier board
T16	ETH_MDC	ETH_MDC	PTE15	O	1V8	
T15	ETH_MDIO	ETH_MDIO	PTE14	I/O	1V8	
T17	FORCE_RECOVERY#	FORCE_RECOVERY#		I	1V8	If LOW, OSM enters recovery mode
A10	GND_A10	GND		PWR	GND	
A4	GND_A4	GND		PWR	GND	
A7	GND_A7	GND		PWR	GND	
AA1	GND_AA1	GND		PWR	GND	
AA10	GND_AA10	GND		PWR	GND	
AA11	GND_AA11	GND		PWR	GND	
AA14	GND_AA14	GND		PWR	GND	
AA17	GND_AA17	GND		PWR	GND	
AA19	GND_AA19	GND		PWR	GND	
AA22	GND_AA22	GND		PWR	GND	
AA4	GND_AA4	GND		PWR	GND	
AA7	GND_AA7	GND		PWR	GND	
AA8	GND_AA8	GND		PWR	GND	
AB15	GND_AB15	GND		PWR	GND	
AB21	GND_AB21	GND		PWR	GND	
AB3	GND_AB3	GND		PWR	GND	
AB6	GND_AB6	GND		PWR	GND	
AB9	GND_AB9	GND		PWR	GND	
AC10	GND_AC10	GND		PWR	GND	
AC4	GND_AC4	GND		PWR	GND	
AC7	GND_AC7	GND		PWR	GND	
B2	GND_B2	GND		PWR	GND	
B5	GND_B5	GND		PWR	GND	
B8	GND_B8	GND		PWR	GND	
B9	GND_B9	GND		PWR	GND	
C11	GND_C11	GND		PWR	GND	
D1	GND_D1	GND		PWR	GND	
D18	GND_D18	GND		PWR	GND	
D5	GND_D5	GND		PWR	GND	
D8	GND_D8	GND		PWR	GND	

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
E15	GND_E15	GND		PWR	GND	
E2	GND_E2	GND		PWR	GND	
E21	GND_E21	GND		PWR	GND	
F16	GND_F16	GND		PWR	GND	
F20	GND_F20	GND		PWR	GND	
H2	GND_H2	GND		PWR	GND	
H4	GND_H4	GND		PWR	GND	
J16	GND_J16	GND		PWR	GND	
J20	GND_J20	GND		PWR	GND	
L18	GND_L18	GND		PWR	GND	
L2	GND_L2	GND		PWR	GND	
L4	GND_L4	GND		PWR	GND	
M16	GND_M16	GND		PWR	GND	
M20	GND_M20	GND		PWR	GND	
P18	GND_P18	GND		PWR	GND	
P2	GND_P2	GND		PWR	GND	
P4	GND_P4	GND		PWR	GND	
R1	GND_R1	GND		PWR	GND	
R16	GND_R16	GND		PWR	GND	
R20	GND_R20	GND		PWR	GND	
U2	GND_U2	GND		PWR	GND	
U4	GND_U4	GND		PWR	GND	
V1	GND_V1	GND		PWR	GND	
V16	GND_V16	GND		PWR	GND	
V20	GND_V20	GND		PWR	GND	
W3	GND_W3	GND		PWR	GND	
Y18	GND_Y18	GND		PWR	GND	
Y2	GND_Y2	GND		PWR	GND	
D17	GPIO_A_0	GPIO_A_0	PTC0	I/O	1V8	
E17	GPIO_A_1	GPIO_A_1	PTC3	I/O	1V8	
F17	GPIO_A_2	GPIO_A_2	PTC11	I/O	1V8	
G17	GPIO_A_3	GPIO_A_3	PTC13	I/O	1V8	
H17	GPIO_A_4	GPIO_A_4	PTC14	I/O	1V8	
J17	GPIO_A_5	GPIO_A_5	PTC15	I/O	1V8	
K17	GPIO_A_6/SPI_A_CS 1#	SPI_A_CS1#	PTC17	I/O	1V8	
L17	GPIO_A_7/SPI_B_CS 1#	SPI_B_CS1#	PTA8	I/O	1V8	
D19	GPIO_B_0	GPIO_B_0	PTC16	I/O	1V8	
E19	GPIO_B_1	GPIO_B_1	PTB5	I/O	1V8	
F19	GPIO_B_2	GPIO_B_2	PTB6	I/O	1V8	
G19	GPIO_B_3	GPIO_B_3	PTA0	I/O	1V8	
H19	GPIO_B_4	GPIO_B_4	PTA24	I/O	1V8	

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
J19	GPIO_B_5	GPIO_B_5	PTF31	I/O	1V8 / 3V3[1]	
K19	GPIO_B_6	GPIO_B_6	PTF30	I/O	1V8 / 3V3[1]	
L19	GPIO_B_7	GPIO_B_7	PTF29	I/O	1V8 / 3V3[1]	
F3	GPIO_C_4/DISP_V	DISP_VDD_EN	PTF5	O	1V8 / 3V3[1]	
F4	GPIO_C_5/DISP_B	DISP_BL_EN	PTF3	O	1V8 / 3V3[1]	
AA15	I2C_A_SCL	I2C_A_SCL	PTE12	O	1V8	2k49 pull-up, OD
AA16	I2C_A_SDA	I2C_A_SDA	PTE13	I/O	1V8	2k49 pull-up, OD
AA20	I2C_B_SCL	I2C_B_SCL	PTA14	O	1V8	2k49 pull-up, OD
AA21	I2C_B_SDA	I2C_B_SDA	PTA15	I/O	1V8	2k49 pull-up, OD
C4	I2C_CAM_SCL/CSI	I2C_CAM_SCL	PTB0	O	1V8	2k49 pull-up, OD
C3	I2C_CAM_SDA/CSI	I2C_CAM_SDA	PTB1	I/O	1V8	2k49 pull-up, OD
V21	I2S_A_DATA_IN	I2S_A_DATA_IN	PTC4	I	1V8	
W21	I2S_A_DATA_OUT	I2S_A_DATA_OUT	PTC7	O	1V8	
V19	I2S_B_DATA_IN	I2S_B_DATA_IN	PTC5	I	1V8	
W19	I2S_B_DATA_OUT	I2S_B_DATA_OUT	PTC6	O	1V8	
W20	I2S_BITCLK	I2S_BITCLK	PTC8	O	1V8	
W18	I2S_LRCLK	I2S_LRCLK	PTC9	O	1V8	
V18	I2S_MCLK	I2S_MCLK	PTC10	O	1V8	
R19	JTAG_nTRST	JTAG_TRST#	PTA19		1V8	
N17	JTAG_TCK(SWCLK)	JTAG_TCK	PTA21		1V8	
P17	JTAG_TDI	JTAG_TDI	PTA23		1V8	
R17	JTAG_TDO(SWO)	JTAG_TDO	PTA22		1V8	
N19	JTAG_TMS(SWDIO)	JTAG_TMS	PTA20		1V8	
E18	PWM_0/DISP_BL_PWM	DISP_BL_PWM	PTF4	O	1V8 / 3V3[1]	
F18	PWM_1	PWM_1	PTA9	O	1V8	
G18	PWM_2	PWM_2	PTA18	O	1V8	
H18	PWM_3	PWM_3	PTC1	O	1V8	
J18	PWM_4	PWM_4	PTC2	O	1V8	
K18	PWM_5	PWM_5	PTC12	O	1V8	
AA9	PWR_BTN#	PWR_BTN#	ONOFF	I	1V8	100k pull-up, active LOW
R4	RGB_B0	RGB_D12	PTF11	O	1V8 / 3V3[1]	
R3	RGB_B1	RGB_D13	PTF10	O	1V8 / 3V3[1]	
P3	RGB_B2	RGB_D14	PTF9	O	1V8 / 3V3[1]	
N3	RGB_B3	RGB_D15	PTF8	O	1V8 / 3V3[1]	

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
N4	RGB_B4	RGB_D16	PTF7	O	1V8 / 3V3[1]	
M3	RGB_B5	RGB_D17	PTF6	O	1V8 / 3V3[1]	
M4	RGB_CLK	RGB_CLK	PTF24	O	1V8 / 3V3[1]	
H3	RGB_CS#	RGB_CS#	PTF2	O	1V8 / 3V3[1]	
J4	RGB_DE	RGB_DE	PTF27	O	1V8 / 3V3[1]	
K4	RGB_DISP	RGB_DISP_EN	PTF1	O	1V8 / 3V3[1]	
W4	RGB_G0	RGB_D06	PTF17	O	1V8 / 3V3[1]	
V3	RGB_G1	RGB_D07	PTF16	O	1V8 / 3V3[1]	
V4	RGB_G2	RGB_D08	PTF15	O	1V8 / 3V3[1]	
U3	RGB_G3	RGB_D09	PTF14	O	1V8 / 3V3[1]	
T3	RGB_G4	RGB_D10	PTF13	O	1V8 / 3V3[1]	
T4	RGB_G5	RGB_D11	PTF12	O	1V8 / 3V3[1]	
K3	RGB_HSYNC	RGB_HSYNC	PTF26	O	1V8 / 3V3[1]	
Y7	RGB_R0	RGB_D00	PTF23	O	1V8 / 3V3[1]	
AA6	RGB_R1	RGB_D01	PTF22	O	1V8 / 3V3[1]	
Y6	RGB_R2	RGB_D02	PTF21	O	1V8 / 3V3[1]	
AA5	RGB_R3	RGB_D03	PTF20	O	1V8 / 3V3[1]	
Y5	RGB_R4	RGB_D04	PTF19	O	1V8 / 3V3[1]	
Y4	RGB_R5	RGB_D05	PTF18	O	1V8 / 3V3[1]	
J3	RGB_RESET#	RGB_RST#	PTF0	O	1V8 / 3V3[1]	
L3	RGB_VSYNC	RGB_VSYNC	PTF25	O	1V8 / 3V3[1]	
W17	RTC_PWR	V_RTC		PWR	3V0	power supply for RTC
J21	SDIO_A_CD#	SDIO_A_CD#	PTD16	I	1V8	10k pull-up
F21	SDIO_A_CLK	SDIO_A_CLK	PTD22	O	1V8	
E20	SDIO_A_CMD	SDIO_A_CMD	PTD23	I/O	1V8	
G20	SDIO_A_D0	SDIO_A_D0	PTD21	I/O	1V8	
G21	SDIO_A_D1	SDIO_A_D1	PTD20	I/O	1V8	
H20	SDIO_A_D2	SDIO_A_D2	PTD19	I/O	1V8	

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
H21	SDIO_A_D3	SDIO_A_D3	PTD18	I/O	1V8	
C20	SDIO_A_IOPWR	V_LDO4_1V8		O	1V8	
D21	SDIO_A_PWR_EN	SDIO_A_PWR_EN	PTD15	O	1V8	
D20	SDIO_A_WP	SDIO_A_WP	PTD17	I	1V8	
W15	SPI_A_/HOLD_(IO3)	SPI_A_HOLD#	PTC19	I/O	1V8	
W16	SPI_A_/WP_(IO2)	SPI_A_WP#	PTC20	I/O	1V8	
Y15	SPI_A_CS0#	SPI_A_CS0#	PTC23	O	1V8	
U16	SPI_A_SCK	SPI_A_SCK	PTC18	O	1V8	
U15	SPI_A_SDI_(IO0)	SPI_A_SDI	PTC22	I/O	1V8	
V15	SPI_A_SDO_(IO1)	SPI_A_SDO	PTC21	I/O	1V8	
AA23	SPI_B_CS0#	SPI_B_CS0#	PTA7	O	1V8	
Y21	SPI_B_SCK	SPI_B_SCK	PTA6	O	1V8	
Y22	SPI_B_SDI	SPI_B_SDI	PTA5	I	1V8	
Y23	SPI_B_SDO	SPI_B_SDO	PTA4	O	1V8	
U17	SYS_RST#	SYS_RST#		I	1V8	100k pull-up, active LOW
C14	UART_A_CTS	UART_A_CTS	PTE8	I	1V8	
C13	UART_A_RTS	UART_A_RTS	PTE9	O	1V8	
A14	UART_A_RX	UART_A_RX	PTE11	I	1V8	
B13	UART_A_TX	UART_A_TX	PTE10	O	1V8	
D16	UART_B_CTS	UART_B_CTS	PTA16	I	1V8	
D15	UART_B_RTS	UART_B_RTS	PTA17	O	1V8	
D14	UART_B_RX	UART_B_RX	PTA3	I	1V8	
D13	UART_B_TX	UART_B_TX	PTA2	O	1V8	
A22	UART_C_RX	UART_C_RX	PTB3	I	1V8	
B23	UART_C_TX	UART_C_TX	PTB2	O	1V8	
D22	UART_CON_RX	UART_CON_RX	PTE7	I	1V8	
D23	UART_CON_TX	UART_CON_TX	PTE6	O	1V8	
C22	UART_D_RX	UART_D_RX	PTA11	I	1V8	
C23	UART_D_TX	UART_D_TX	PTA10	O	1V8	
AB13	USB_A_D_N	USB_A_D_N	USB0_DM			
AC14	USB_A_D_P	USB_A_D_P	USB0_DP			
AC16	USB_A_EN	USB_A_EN	PTD13	O	1V8	
AB14	USB_A_ID	USB_A_ID	PTD12	I	1V8	10k pull-up
AC15	USB_A_OC#	USB_A_OC#	PTD14	I	1V8	10k pull-up
AB16	USB_A_VBUS	USB_A_VBUS	USB0_VBUS_DETEC	I	5V0	
AB23	USB_B_D_N	USB_B_D_N	USB1_DM			
AC22	USB_B_D_P	USB_B_D_P	USB1_DP			
AC20	USB_B_EN	USB_B_EN	PTE2	O	1V8	
AB22	USB_B_ID	USB_B_ID	PTE4	I	1V8	10k pull-up
AC21	USB_B_OC#	USB_B_OC#	PTE5	I	1V8	10k pull-up
AB20	USB_B_VBUS	USB_B_VBUS	USB1_VBUS_DETEC	I	5V0	

Con-tact	Contact Name	Internal Pad		I/O	Vol-tage	Remarks
M19	VCC_2_TEST	V_1V8		PWR	1V8	Test output for 1V8 regulator
Y16	VCC_3_TEST	V_LDO3_3V3		PWR	3V3	Test output for 3V3 regulator
Y20	VCC_4_TEST	V_BUCK2_1V0		PWR	1V0	Test output for 1V0 regulator
Y3	VCC_5_TEST	V_DRAM_VDDQ		PWR	1V1	Test output for 1V1 regulator
C5	VCC_6_TEST	V_DRAM_VDD_1V1		PWR	1V1	Test output for 1V1 regulator
Y10	VCC_IN_5V_Y10	V_5V0		PWR	5V0	
Y11	VCC_IN_5V_Y11	V_5V0		PWR	5V0	
Y8	VCC_IN_5V_Y8	V_5V0		PWR	5V0	
Y9	VCC_IN_5V_Y9	V_5V0		PWR	5V0	
U18	VCC_OUT_IO	V_1V8		PWR	1V8	

Table 2: B2B connector

[1]: The CPU Domain PTF can be 1.8V or 3.3V. Per default its 1.8V. For RGB Option it is 3.3V

4 Interfaces

4.1 USB 2.0 Interfaces

The module supports two USB 2.0 controllers and PHYs. The can be configured as USB host or as USB device.

The 90 Ohm differential pair of USB signals doesn´t need any termination.
For external ports on carrier board ESD and EMV protection is required nearby the USB connectors.
If the USB will be used in Host Mode, contact USB_ID must be connected to GND. Otherwise it must be directly connected to the USB connector.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AB13	USB_A_D_N	USB0_DM			
AC14	USB_A_D_P	USB0_DP			
AC16	USB_A_EN	PTD13	O	1V8	
AB14	USB_A_ID	PTD12	I	1V8	10k pull-up
AC15	USB_A_OC#	PTD14	I	1V8	10k pull-up
AB16	USB_A_VBUS	USB0_VBUS_DETECT	I	5V0	
AB23	USB_B_D_N	USB1_DM			
AC22	USB_B_D_P	USB1_DP			
AC20	USB_B_EN	PTE2	O	1V8	
AB22	USB_B_ID	PTE4	I	1V8	10k pull-up
AC21	USB_B_OC#	PTE5	I	1V8	10k pull-up
AB20	USB_B_VBUS	USB1_VBUS_DETECT	I	5V0	

Table 3: USB A/B Interface Connections

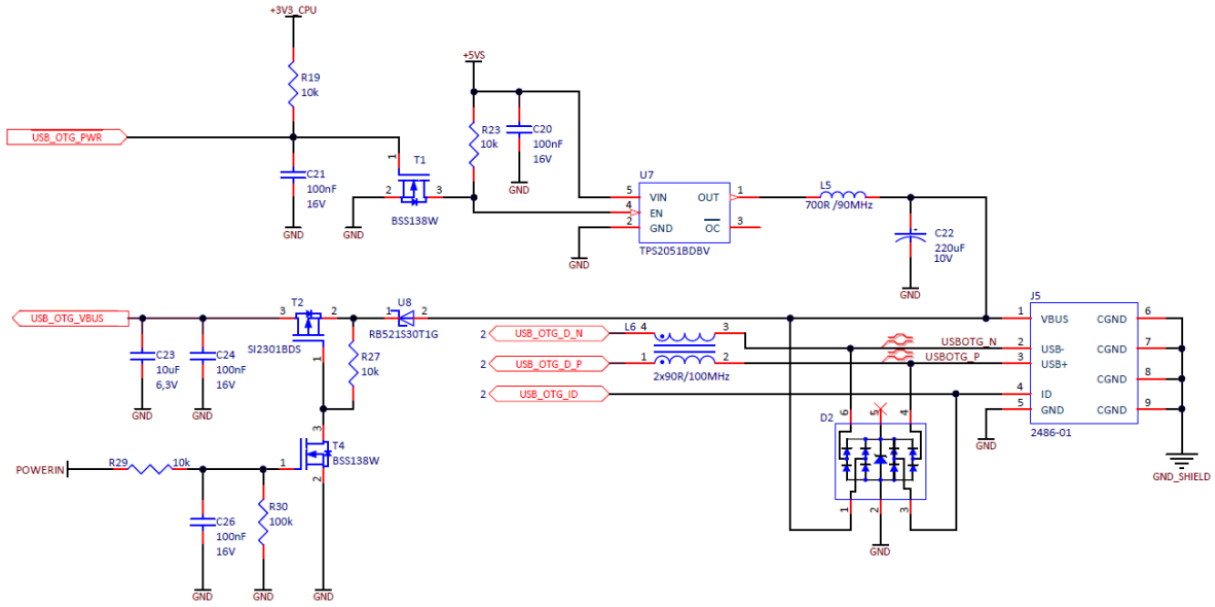


Figure 8: USB OTG example connection on carrier board

4.2 SD/MMC Interface

The module supports one SD/MMC/eMMC/SDHC interface with 4 data bits.

For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The supply voltage of SD_A (SD_A_VCC) is fixed to 1.8V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
C20	SDIO_A_IOPWR		O	1V8	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA
J21	SDIO_A_CD#	PTD16	I	1V8	Active low, card detect, onboard pull-up 10k
F21	SDIO_A_CLK	PTD22	O	1V8	
E20	SDIO_A_CMD	PTD23	I/O	1V8	
G20	SDIO_A_D0	PTD21	I/O	1V8	
G21	SDIO_A_D1	PTD20	I/O	1V8	
H20	SDIO_A_D2	PTD19	I/O	1V8	
H21	SDIO_A_D3	PTD18	I/O	1V8	
D21	SDIO_A_PWR_EN	PTD15	O	1V8	
D20	SDIO_A_WP	PTD17	I	1V8	If not used on carrier board, pull-down pin or disable in software

Table 4: SD Card A Interface

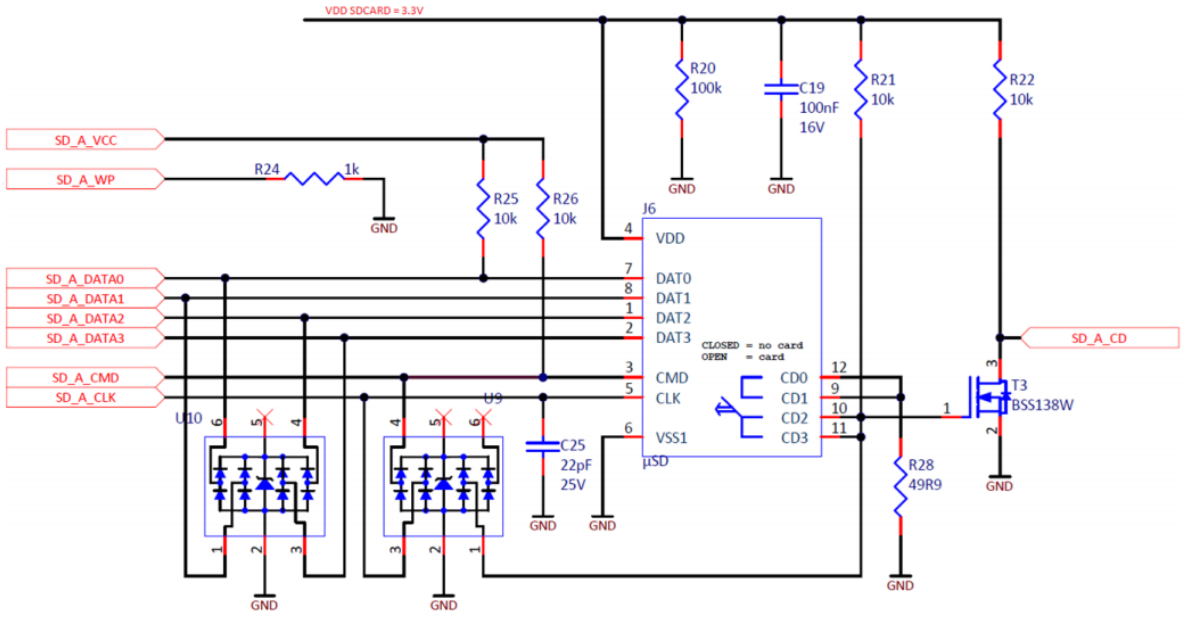


Figure 9: SD Card Connector example connection on carrier board

4.3 QSPI Interface

T.B.D.

4.4 SPI Interface

The module supports two SPIs (Serial Peripheral Interface). All signals are 1.8V compliant. Devices on carrier board with other voltage levels need a level shifter.
Signals don´t have Pull-Ups on module.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
W15	SPI_A_/HOLD_(IO3)	PTC19	I/O	1V8	
W16	SPI_A_/WP_(IO2)	PTC20	I/O	1V8	
Y15	SPI_A_CS0#	PTC23	O	1V8	
U16	SPI_A_SCK	PTC18	O	1V8	
U15	SPI_A_SDI_(IO0)	PTC22	I/O	1V8	
V15	SPI_A_SDO_(IO1)	PTC21	I/O	1V8	
AA23	SPI_B_CS0#	PTA7	O	1V8	
Y21	SPI_B_SCK	PTA6	O	1V8	
Y22	SPI_B_SDI	PTA5	I	1V8	
Y23	SPI_B_SDO	PTA4	O	1V8	

Table 5: SPI Interface

4.5 I2C

The modules supports up to 3 I2C Interfaces. Devices on baseboard with other voltage need a level shifter.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AA15	I2C_A_SCL	PTE12	I/O	1V8	2k49 pull-up, OD
AA16	I2C_A_SDA	PTE13	I/O	1V8	2k49 pull-up, OD
AA20	I2C_B_SCL	PTA14	I/O	1V8	2k49 pull-up, OD
AA21	I2C_B_SDA	PTA15	I/O	1V8	2k49 pull-up, OD
C4	I2C_CAM_SCL/CSI	PTB0	I/O	1V8	2k49 pull-up, OD
C3	I2C_CAM_SDA/CSI	PTB1	I/O	1V8	2k49 pull-up, OD

Table 6: I2C Interface

4.6 Serial Interface (UART)

FS OSM™-SF-IMX8ULP module provides 5 UART channels:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 5 Mbps
- 2x UART with flow control signals RTS and CTS, 3x standard RX and TX.

We recommend to use UART_CON for debugging and service only.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
C14	UART_A_CTS	PTE8	I	1V8	
C13	UART_A_RTS	PTE9	O	1V8	
A14	UART_A_RX	PTE11	I	1V8	
B13	UART_A_TX	PTE10	O	1V8	
D16	UART_B_CTS	PTA16	I	1V8	
D15	UART_B_RTS	PTA17	O	1V8	
D14	UART_B_RX	PTA3	I	1V8	
D13	UART_B_TX	PTA2	O	1V8	
A22	UART_C_RX	PTB3	I	1V8	
B23	UART_C_TX	PTB2	O	1V8	
D22	UART_CON_RX	PTE7	I	1V8	
D23	UART_CON_TX	PTE6	O	1V8	
C22	UART_D_RX	PTA11	I	1V8	
C23	UART_D_TX	PTA10	O	1V8	

Table 7: UART Interface Signals

4.7 Ethernet

The FS OSM™-SF-IMX8ULP supports ONE 10/100Mbit LAN interface via RMII signals.

An external Ethernet-PHY or an external switch is required.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
R15	ETH_A_(R)(G)MII_ RX_CLK	PTE19	I	1V8	
M15	ETH_A_(R)(G)MII_ RX_DV(_ER)	PTE18	I	1V8	
L16	ETH_A_(R)(G)MII_ RX_ER	PTE17	I	1V8	
J15	ETH_A_(R)(G)MII_ TX_CLK	PTE3	O	1V8	
K16	ETH_A_(R)(G)MII_ TX_EN(_ER)	PTE16	O	1V8	
K15	ETH_A_(S)(R)(G)MII_ RXD0	PTE21	I	1V8	
L15	ETH_A_(S)(R)(G)MII_ RXD1	PTE20	I	1V8	
H15	ETH_A_(S)(R)(G)MII_ TXD0	PTE23	O	1V8	
G15	ETH_A_(S)(R)(G)MII_ TXD1	PTE22	O	1V8	
M17	ETH_IOPWR		O	1V8	
T16	ETH_MDC	PTE15	O	1V8	
T15	ETH_MDIO	PTE14	I/O	1V8	

Table 8: RGMII Interface (no Ethernet PHY)

4.8 Audio (I2S)

The module supports only I2S signals. An external audio codec IC (i.e. SGTL500…) on the carrier board is needed for Audio output.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
V21	I2S_A_DATA_IN	PTC4	I	1V8	
W21	I2S_A_DATA_OUT	PTC7	O	1V8	
V19	I2S_B_DATA_IN	PTC5	I	1V8	
W19	I2S_B_DATA_OUT	PTC6	O	1V8	
W20	I2S_BITCLK	PTC8	O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU act in Slave Mode
W18	I2S_LRCLK	PTC9	O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
V18	I2S_MCLK	PTC10	O	1V8	

Table 9: Audio Interface (without Codec)

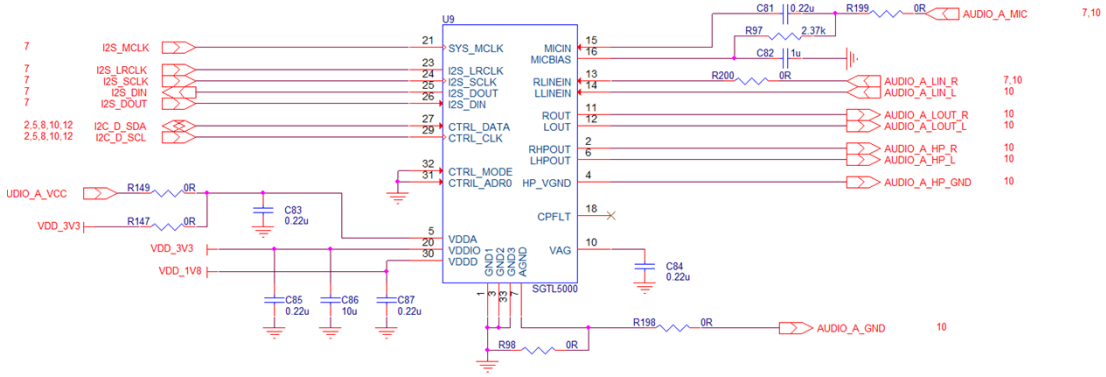


Figure 10 SGTL5000 Codec circuit example for carrier board

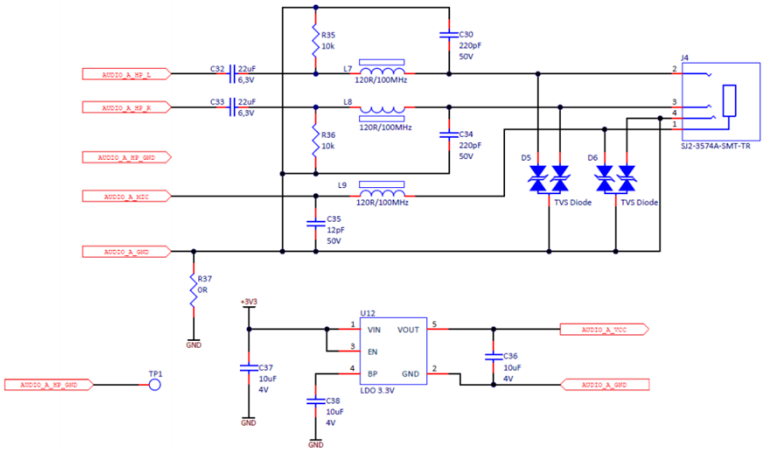


Figure 11 Headphone-Out Mic-In example circuit for carrier board

4.9 MIPI DSI

The module supports one quad lane MIPI DSI interface with following features:

- Support one 4-lane MIPI DSI display with pixels from the LCDIF
- Compliant to MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- The maximum pixel clock is 200 MHz and active pixel rate of 140 Mpixel/s with 24-bit RGB. This includes resolutions such as 1080p60 or 1920x1200p60.
- The maximum data rate per lane is 1.5 Gbps.

The signals can be connected directly to a MIPI compliant display.

The contacts are shared with LVDS interface. **LVDS is a soldering option.**

The CPU Domain PTF can be 1.8V or 3.3V. Per default its 1.8V. For RGB Option it is 3.3V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
AB8	DSI_CLOCK_N	DSI_CLK_N	O	1.2V/200mV*1	
AB7	DSI_CLOCK_P	DSI_CLK_P	O	1.2V/200mV*1	
AB11	DSI_DATA0_N	DSI_DATA0_N	O	1.2V/200mV*1	
AB10	DSI_DATA0_P	DSI_DATA0_P	O	1.2V/200mV*1	
AC9	DSI_DATA1_N	DSI_DATA1_N	O	1.2V/200mV*1	
AC8	DSI_DATA1_P	DSI_DATA1_P	O	1.2V/200mV*1	
AC6	DSI_DATA2_N	DSI_DATA2_N	O	1.2V/200mV*1	
AC5	DSI_DATA2_P	DSI_DATA2_P	O	1.2V/200mV*1	
AB5	DSI_DATA3_N	DSI_DATA3_N	O	1.2V/200mV*1	
AB4	DSI_DATA3_P	DSI_DATA3_P	O	1.2V/200mV*1	
AA3	DSI_TE	PTF28	I	1V8 / 3V3	
F3	DISP_VDD_EN/ GPIO_C_4	PTF5	O	1V8 / 3V3	
F4	DISP_BL_EN / GPIO_C_5	PTF3	O	1V8 / 3V3	
E18	DISP_BL_PWM/ PWM0	PTF4	O	1V8 / 3V3	

Table 10: MIPI-DSI Interface

*1 : 1.2V in single-ended mode, approx. 200mV in differential mode

4.10 RGB

The module supports a 18 bit RGB interface.

The CPU Domain PTF can be 1.8V or 3.3V. Per default its 1.8V. For RGB Option it is 3.3V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
Y7	RGB_R0	PTF23	O	1V8 / 3V3	
AA6	RGB_R1	PTF22	O	1V8 / 3V3	
Y6	RGB_R2	PTF21	O	1V8 / 3V3	
AA5	RGB_R3	PTF20	O	1V8 / 3V3	
Y5	RGB_R4	PTF19	O	1V8 / 3V3	
Y4	RGB_R5	PTF18	O	1V8 / 3V3	
W4	RGB_G0	PTF17	O	1V8 / 3V3	
V3	RGB_G1	PTF16	O	1V8 / 3V3	
V4	RGB_G2	PTF15	O	1V8 / 3V3	
U3	RGB_G3	PTF14	O	1V8 / 3V3	
T3	RGB_G4	PTF13	O	1V8 / 3V3	
T4	RGB_G5	PTF12	O	1V8 / 3V3	
R4	RGB_B0	PTF11	O	1V8 / 3V3	
R3	RGB_B1	PTF10	O	1V8 / 3V3	
P3	RGB_B2	PTF9	O	1V8 / 3V3	
N3	RGB_B3	PTF8	O	1V8 / 3V3	
N4	RGB_B4	PTF7	O	1V8 / 3V3	
M3	RGB_B5	PTF6	O	1V8 / 3V3	
J4	RGB_DE	PTF27	O	1V8 / 3V3	
K4	RGB_DISP	PTF1	O	1V8 / 3V3	
K3	RGB_HSYNC	PTF26	O	1V8 / 3V3	
J3	RGB_RESET#	PTF0	O	1V8 / 3V3	
L3	RGB_VSYNC	PTF25	O	1V8 / 3V3	
M4	RGB_CLK	PTF24	O	1V8 / 3V3	
H3	RGB_CS#	PTF2	O	1V8 / 3V3	

Table 11: RGB Interface

4.11 MIPI CSI Interface

The module supports one dual lance MIPI CSI interface with following features:

- Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2
- Support up to 2 Rx data lanes (plus 1 Rx clock lane)
- MIPI CSI-2 supports: – Pixel clock up to 200 MHz (at both nominal and overdrive voltage) – Up to approximately 150 Mpixel/s supported – 80 Mbps to 1.5 Gbps per lane data rate in high speed operation
- Support 10 Mbps data rate in low power operation

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
B3	CSI_CLOCK_N	CSI_CLK_N	I		
B4	CSI_CLOCK_P	CSI_CLK_P	I		
C1	CSI_DATA0_N	CSI_D0_N	I		
B1	CSI_DATA0_P	CSI_D0_P	I		
A2	CSI_DATA1_N	CSI_D1_N	I		
A3	CSI_DATA1_P	CSI_D1_P	I		
C4	I2C_CAM_SCL	PTB0	I/O	1V8	2k49 pull-up
C3	I2C_CAM_SDA	PTB1	I/O	1V8	2k49 pull-up
C2	CAM_MCK	PTB12	O	1V8	Master clock output
G3	CAM_PWR	PTB13	I/O	1V8	Camera power enable. Active high output.
G4	CAM_RST#	PTB14	I/O	1V8	Camera reset. Active low output

Table 12: MIPI-CSI Interface

4.12 CAN FD Interface

The FS OSM™-SF-IMX8ULP supports one CAN FD interface.

Contact	Contact Name	Internal Pad	I/O	Vendor	Remarks
AB17	CAN_A_RX	PTA13	I	1V8	
AC17	CAN_A_TX	PTA12	O	1V8	

Table 13: CAN Interface

4.13 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it´s not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced I/O power is not allowed.

The CPU Domain PTF can be 1.8V or 3.3V. Per default its 1.8V. For RGB Option it is 3.3V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
D17	GPIO_A_0	PTC0	I/O	1V8	
E17	GPIO_A_1	PTC3	I/O	1V8	
F17	GPIO_A_2	PTC11	I/O	1V8	
G17	GPIO_A_3	PTC13	I/O	1V8	
H17	GPIO_A_4	PTC14	I/O	1V8	
J17	GPIO_A_5	PTC15	/IO	1V8	
K17	GPIO_A_6/ SPI_A_CS1#	PTC17	I/O	1V8	Dual function: SPI_A_CS1#
L17	GPIO_A_7/ SPI_B_CS1#	PTA8	I/O	1V8	Dual function: SPI_A_CS2#
D19	GPIO_B_0	PTC16	I/O	1V8	
E19	GPIO_B_1	PTB5	I/O	1V8	
F19	GPIO_B_2	PTB6	I/O	1V8	
G19	GPIO_B_3	PTA0	I/O	1V8	
H19	GPIO_B_4	PTA24	I/O	1V8	
J19	GPIO_B_5	PTF31	I/O	1V8 / 3V3	
K19	GPIO_B_6	PTF30	I/O	1V8 / 3V3	
L19	GPIO_B_7	PTF29	I/O	1V8 / 3V3	
F3	GPIO_C_4/ DISP_VDD_EN	PTF5	I/O	1V8 / 3V3	Dual function: DISP_VDD_EN
F4	GPIO_C_5/ DISP_BL_EN	PTF3	I/O	1V8 / 3V3	Dual function: DISP_BL_EN
G3	GPIO_C_6 / CAM_PWR	PTB13	I/O	1V8	Dual function: CAM_PWR
G4	GPIO_C_7 / CAM_RST#	PTB14	I/O	1V8	Dual function: CAM_RST#

Table 14: GPIO Interface

4.14 JTAG

JTAG is for debug only.

Leave unconnected, if you don´t use JTAG.

Don´t put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
N17	JTAG_TCK(SWCLK)	PTA21		1V8	
P17	JTAG_TDI	PTA23		1V8	
R17	JTAG_TDO(SWO)	PTA22		1V8	
N19	JTAG_TMS(SWDIO)	PTA20		1V8	
R19	JTAG_nTRST	PTA19		1V8	

Table 15: JTAG Interface

4.15 PWM

PWMs are free programmable. On a non-powered board it´s not allowed to have a voltage on one of the PWM contacts. Also a higher voltage as the announced I/O power is not allowed.

The CPU Domain PTF can be 1.8V or 3.3V. Per default its 1.8V. For RGB Option it is 3.3V.

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
E18	PWM_0/DISP_BL_PWM	PTF4	O	1V8 / 3V3	Dual function: DISP_BL_PWM
F18	PWM_1	PTA9	O	1V8	
G18	PWM_2	PTA18	O	1V8	
H18	PWM_3	PTC1	O	1V8	
J18	PWM_4	PTC2	O	1V8	

Table 16: PWM Interface

4.16 Vendor defined contacts

No vendor defined contacts.

5 eMMC

The module supports eMMC v4.41 or higher from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 RTC

There is an external RTC (PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 Power and Power Control Pins

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
U19	BOOT_SEL0#		I	1V8	If LOW, OSM boots from external QSPI-Flash; Leave open if boot from eMMC
V17	CARRIER_PWR_EN	SAI1_TXFS	O	1V8	10k pull-down, carrier board circuits should not be powered up until module asserts signal
T17	FORCE_RECOVERY#		I	1V8	If LOW, OSM enters recovery mode
A10, A4, A7, AA1, AA10, AA11, AA14, AA17, AA19, AA22, AA4, AA7, AA8, AB15, AB21, AB3, AB6, AB9, AC4, AC7, B2, B5, B8, B9, C11, D1, D18, D5, D8, E15, E2, E21, F16, F20, H2, H4, J16, J20, L18, L2, L4, M16, M20, P18, P2, P4, R1, R16, R20, U2, U4, V1, V16, V20, W3, Y18, Y2, AC10	GND	GND	PWR	GND	Main Power supply Ground input; Connect all GND-Pins on your carrier board.
AA9	PWR_BTN#	ONOFF	I	1V8	Power-button from Carrier board. Carrier to float the line in in-active state. Active low,

Contact	Contact Name	Internal Pad	I/O	Voltage	Remarks
					level sensitive. 100k pull-up, active low
W17	RTC_PWR		I	3V0	RTC battery input; tie to 3.0V. Please refer chapter 8.2DC Electrical Characteristics.
C20	SDIO_A_IOPWR	NVCC_SD2	O	1V8	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA.
U17	SYS_RST#	PMIC_RST_B	I	1V8	Reset input from carrier board. Carrier drives low to force a Module reset, floats the line otherwise. 100k pull-up, active low.
AB16	USB_A_VBUS		I	5V0	
AB20	USB_B_VBUS		I	5V0	
M19	VCC_2_TEST		O	1V8	Module power voltage test point. Leave open (N.C.)
Y16	VCC_3_TEST		O	3V3	Module power voltage test point. Leave open (N.C.)
Y20	VCC_4_TEST		O	1V8	Module power voltage test point. Leave open (N.C.)
Y3	VCC_5_TEST		O	1V1/0V6	Module power voltage test point. Leave open (N.C.)
C5	VCC_6_TEST		O	1V1	Module power voltage test point. Leave open (N.C.)
Y10	VCC_IN_5V	---	I	5V0	Main Power supply input. Please refer chapter 8.2 DC Electrical Characteristics for more information.
Y11	VCC_IN_5V	---	I	5V0	
Y17	VCC_IN_5V	---	I	5V0	
Y8	VCC_IN_5V	---	I	5V0	
Y9	VCC_IN_5V	---	I	5V0	
U18	VCC_OUT_IO		O	1V8	Output IO voltage for peripherals on carrier board. Maximum current 100mA, leave open if not used.
C6, C7, D6, D7, N2, R18, T17, T18, T19, Y13, Y14, AA2, AA13	RESERVED				Leave these pins floating (N.C.)

Table 17: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test Laboratory. It's possible to use a super-capacitor instead.

VCC_OUT_IO is a 1V8 @100mA output. It´s generated from the internal PMIC and powered from VIN. Can be used as "Enable Signal" for the power regulators on baseboard. Please do not use VCC_OUT_IO as power supply for carrier board.

PWR_BTN# is the reset input for the module. PWR_BTN# only resets the CPU. In the event of a power failure, VCC_IN must be switched off and on to avoid latch-up effects.

The GND contacts which are given in the table above are the power ground contacts for VCC_IN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Typ	Max	Unit
Input Voltage range 3.3V IOs	-0.3	3.3	3.6	V
Input Voltage range 1.8V IOs	-0.3	1.8	2.1	V
Voltage on any IO with VDD_VIN off			0.3	V
USB VBUS	-0.3	5	5.6	V
Maximum power consumption VDD_VBAT at 85°C			0.6	µA
Maximum output current VCC_IO			100	mA

Table 18: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
VCC_VIN	Module main power		2.7	5	5.5	V
RTC_PWR	RTC power		0.9	3	5.5	V
USB1/2_VBUS	USB supply voltage		4.4	5	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_VIN		3.15	3.3	3.45	V
VDD_1V8	1.8V output for power enable on carrier board		1.71	1.8	1.89	V
V_{ih}	High Level Input Voltage		0.7*OVDD		OVDD	V
V_{il}	Low Level Input Voltage		0		0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15			V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA			0.15	V
I_o	Output current IOs 1V8	1.8V			10	mA
I_o	Output current IOs 3V3	3.3V			5	mA
I_{VBAT}	Current consumption VBAT				0.22[*1]	µA

Table 19: DC Electrical Characteristics

[*1] Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Grade Operating Temperature	0		+70	°C
Industrial Grade Operating Temperature	-20		+85	°C
Extended Industrial Grade Operating Temperature	-40		t.b.d	°C
Junction Temperature i.MX8ULP (C-Temp)	0		+95	°C
Junction Temperature i.MX8ULP (I-Temp)	-40		+105	°C
Junction to Package TOP (Ψ_{JT}) – i.MX8ULP**Error! Reference source not found.**		t.b.d		°C/W

Table 20: Thermal Specification

Note 1: Maximum junction temperature of the CPU is 105°C.
In this case cooling is necessary and highly recommended.
See also: Power consumption and cooling

Please get in touch with our engineers for F&S recommended cooling solutions.

Note 2: *Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN12468* (https://www.nxp.com/docs/en/application-note/AN12468.pdf)

10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. t.b.d **Watt** to t.b.d **Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity:	6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity:	12 months

For longer storage we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %. Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 12: Matrix Code Sticker

18 Appendix

Important Notice

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