Hardware Documentation

FSSMMX8MP

Preliminary

Version 002
(2023-11-23)

Elektronik Systeme

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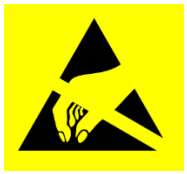
About This Document

This document describes how to use the FSSMMX8MP SMARC compatible SOM with mechanical and electrical information. The latest version of this document can be found at:

https://www.fsembedded.com.

Attention: Please also note the SMARC Design Guide 2.1.1.

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Author
01.04.2023	001	All		-	Initial Version (Preliminary)	HF
14.11.2023	002		M	all	minor adaptions	UK

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block Diagram

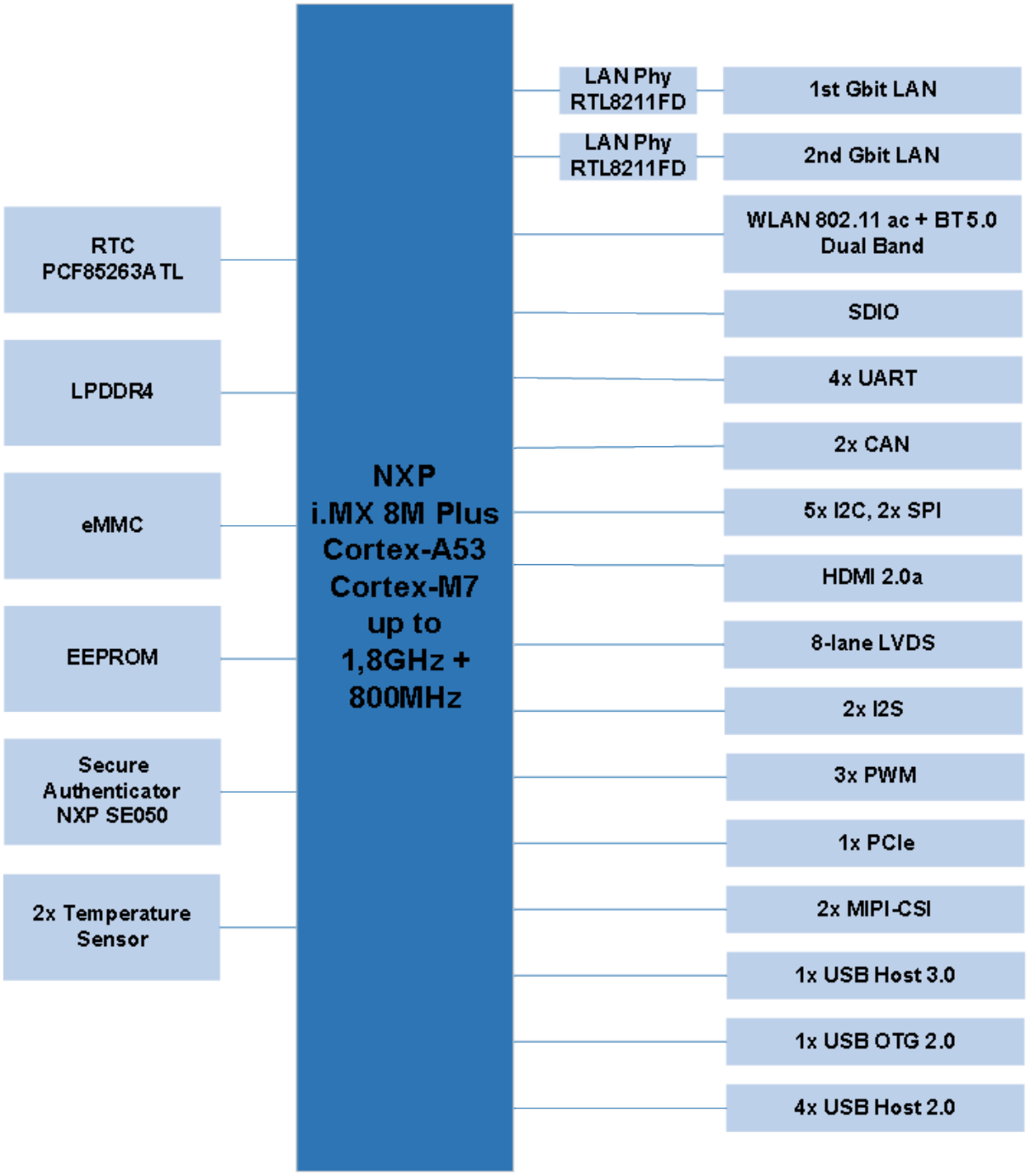

Figure 1: Block Diagram

2 Mechanical Dimensions

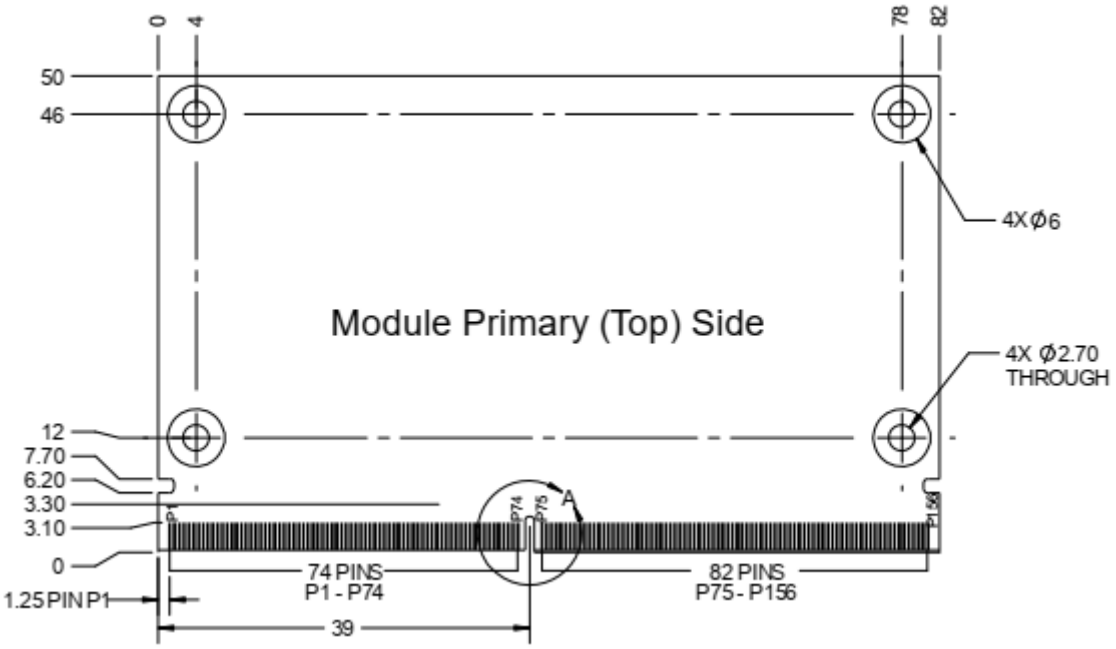

Figure 2: Mechanical Dimensions

Dimensions	Description
Size	82mm x 50mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	max. 3.0mm
Height of the parts on the bottom side	max. 1.3mm

Table 1: Mechanical Dimensions

3D Step model is available, please contact *support@fs-net.de*.

3 Interface and Signal Description

SMARC modules use a gold finger connector that is compatible with the MXM3 graphics card connector. The connector has 314 pins.

See chapter 5.1 of the SMARC 2 specification for a list of connectors suitable for the carrier board.

Pin	Pin Name	CPU Pad / Connection	I/O	Description
P1	SMB_ALERT#	I/O-Expander	I	SM Bus interrupt
P2	GND_1		GND	
P3	CSI1_CK+	MIPI_CSI2_CLK_P	I	CSI1 differential clock+
P4	CSI1_CK-	MIPI_CSI2_CLK_N	I	CSI1 differential clock-
P5	GBE1_SDP		NC	not connected
P6	GBE0_SDP		NC	not connected
P7	CSI1_RX0+	MIPI_CSI2_D0_P	I	CSI1 differential data 0+
P8	CSI1_RX0-	MIPI_CSI2_D0_N	I	CSI1 differential data 0-
P9	GND_2		GND	
P10	CSI1_RX1+	MIPI_CSI2_D1_P	I	CSI1 differential data 1+
P11	CSI1_RX1-	MIPI_CSI2_D1_N	I	CSI1 differential data 1-
P12	GND_3		GND	
P13	CSI1_RX2+	MIPI_CSI2_D2_P	I	CSI1 differential data 2+
P14	CSI1_RX2-	MIPI_CSI2_D2_N	I	CSI1 differential data 2-
P15	GND_4		GND	
P16	CSI1_RX3+	MIPI_CSI2_D3_P	I	CSI1 differential data 3+
P17	CSI1_RX3-	MIPI_CSI2_D3_N	I	CSI1 differential data 3-
P18	GND_5		GND	
P19	GBE0_MDI3-	LAN PHY	I/O	ETH0 MDI differential data 3-
P20	GBE0_MDI3+	LAN PHY	I/O	ETH0 MDI differential data 3+
P21	GBE0_LINK100#	LAN PHY	O	ETH0 link speed indication
P22	GBE0_LINK1000#	LAN PHY	O	ETH0 link speed indication
P23	GBE0_MDI2-	LAN PHY	I/O	ETH0 MDI differential data 2-
P24	GBE0_MDI2+	LAN PHY	I/O	ETH0 MDI differential data 2+
P25	GBE0_LINK_ACT#	LAN PHY	O	ETH0 activity indication
P26	GBE0_MDI1-	LAN PHY	I/O	ETH0 MDI differential data 1-
P27	GBE0_MDI1+	LAN PHY	I/O	ETH0 MDI differential data 1+
P28	GBE0_CTREF		NC	not connected
P29	GBE0_MDI0-	LAN PHY	I/O	ETH0 MDI differential data 0-
P30	GBE0_MDI0+	LAN PHY	I/O	ETH0 MDI differential data 0+
P31	SPI0_CS1#	I2C4_SDA	O	SPI0 Chip Select 1
P32	GND_6		GND	
P33	SDIO_WP	SD2_WP	I	SDIO Write Protect
P34	SDIO_CMD	SD2_CMD	I/O	SDIO Command/Response
P35	SDIO_CD#	SD2_CD_B	I	SDIO Card Detect
P36	SDIO_CK	SD2_CLK	O	SDIO clock
P37	SDIO_PWR_EN	SD2_RESET_B	O	SDIO power enable

P38	GND_7		GND	
P39	SDIO_D0	SD2_DATA0	I/O	SDIO data 0
P40	SDIO_D1	SD2_DATA1	I/O	SDIO data 1
P41	SDIO_D2	SD2_DATA2	I/O	SDIO data 2
P42	SDIO_D3	SD2_DATA3	I/O	SDIO data 3
P43	SPI0_CS0#	ECSPI1_SS0	O	SPI0 Chip Select 0
P44	SPI0_CK	ECSPI1_SCLK	O	SPI0 clock
P45	SPI0_DIN	ECSPI1_MISO	I	SPI0 Master IN / Slave OUT
P46	SPI0_DO	ECSPI1_MOSI	O	SPI0 Master OUT / Slave IN
P47	GND_8		GND	
P48	SATA_TX+		NC	not connected
P49	SATA_TX-		NC	not connected
P50	GND_9		GND	
P51	SATA_RX+		NC	not connected
P52	SATA_RX-		NC	not connected
P53	GND_10		GND	
P54	SPI1_CS0#	ECSPI2_SS0	O	SPI1 Chip Select 0
P55	SPI1_CS1#	GPIO1_IO03	O	SPI1 Chip Select 1
P56	SPI1_CK	ECSPI2_SCLK	O	SPI1 clock
P57	SPI1_DIN	ECSPI2_MISO	I	SPI1 Master IN / Slave OUT
P58	SPI2_DO	ECSPI2_MOSI	O	SPI1 Master OUT / Slave IN
P59	GND_11		GND	
P60	USB0+	USB1_D_P	I/O	USB0 (USB 2.0 OTG) differential data+
P61	USB0-	USB1_D_N	I/O	USB0 (USB 2.0 OTG) differential data-
P62	USB0_EN_OC#	GPIO1_IO13	I/O	USB0 enable/over-current sense
P63	USB0_VBUS_DET	USB1_VBUS	I	USB0 Host Power Detection
P64	USB0_OTG_ID	GPIO1_IO10	I	USB0 ID
P65	USB1+	USB Hub	I/O	USB1 (USB 2.0 Host) differential data+
P66	USB1-	USB Hub	I/O	USB1 (USB 2.0 Host) differential data-
P67	USB1_EN_OC#	USB Hub	I/O	USB1 enable/over-current sense
P68	GND_12		GND	
P69	USB2+	USB2_D_P / USB Hub	I/O	USB2 (USB 2.0/3.0 Host) differential data+
P70	USB2-	USB2_D_N / USB Hub	I/O	USB2 (USB 2.0/3.0 Host) differential data-
P71	USB2_EN_OC#	USB Hub	I/O	USB2 (USB 2.0) enable/over-current sense
P72	RSVD_2		NC	not connected
P73	RSVD_3		NC	not connected
P74	USB3_EN_OC#	USB Hub	I/O	USB3 enable/over-current sense
P75	PCIE_A_RST#	I/O-Expander	O	PCIe0 reset
P76	USB4_EN_OC#	USB Hub	I/O	USB4

				enable/over-current sense
P77	PCIE_B_CKREQ#		NC	not connected
P78	PCIE_A_CKREQ#	I2C4_SCL	I	PCIe clock request
P79	GND_13		GND	
P80	PCIE_C_REFCK+		NC	not connected
P81	PCIE_C_REFCK-		NC	not connected
P82	GND_14		GND	
P83	PCIE_A_REFCK+	PCIE_REF_PAD_CL	O	PCIe diff. reference clock+
P84	PCIE_A_REFCK-	PCIE_REF_PAD_CL	O	PCIe diff. reference clock-
P85	GND_15		GND	
P86	PCIE_A_RX+	PCIE_RXN_P	I	PCIe diff. receive data+
P87	PCIE_A_RX-	PCIE_RXN_N	I	PCIe diff. receive data-
P88	GND_16		GND	
P89	PCIE_A_TX+	PCIE_TXN_P	O	PCIe diff. transmit data+
P90	PCIE_A_TX-	PCIE_TXN_N	O	PCIe diff. transmit data-
P91	GND_17		GND	
P92	HDMI_D2+	HDMI_TX2_P	O	HDMI differential data 2+
P93	HDMI_D2-	HDMI_TX2_N	O	HDMI differential data 2-
P94	GND_18		GND	
P95	HDMI_D1+	HDMI_TX1_P	O	HDMI differential data 1+
P96	HDMI_D1-	HDMI_TX1_N	O	HDMI differential data 1-
P97	GND_19		GND	
P98	HDMI_D0+	HDMI_TX0_P	O	HDMI differential data 0+
P99	HDMI_D0-	HDMI_TX0_N	O	HDMI differential data 0-
P100	GND_20		GND	
P101	HDMI_CK+	HDMI_TXC_P	O	HDMI differential clock+
P102	HDMI_CK-	HDMI_TXC_N	O	HDMI differential clock-
P103	GND_21		GND	
P104	HDMI_HPD	HDMI_HPD	I	HDMI hot plug detection
P105	HDMI_CTRL_CK	HDMI_DDC_SCL	O	HDMI dedicated I^2C clock
P106	HDMI_CTRL_DAT	HDMI_DDC_SDA	I/O	HDMI dedicated I^2C data
P107	DP1_AUX_SEL		NC	not connected
P108	CAM0_PWR#	GPIO1_IO09	O	Camera0 power enable (may be used as GPIO)
P109	CAM1_PWR#	GPIO1_IO07	O	Camera1 power enable (may be used as GPIO)
P110	CAM0_RST#	GPIO1_IO05	O	Camera0 reset (may be used as GPIO)
P111	CAM1_RST#	GPIO1_IO15	O	Camera1 reset (may be used as GPIO)
P112	HDA_RST#	SAI3_RXFS	O	HD Audio reset (may be used as GPIO)
P113	GPIO5	SPDIF_EXT_CLK	I/O	
P114	GPIO6	SAI3_TXC	I/O	
P115	GPIO7	GPIO1_IO11	I/O	
P116	GPIO8	NAND_CE3_B	I/O	
P117	GPIO9	NAND_CLE	I/O	

P118	GPIO10	NAND_RE_B	I/O	
P119	GPIO11	NAND_READY_B	I/O	
P120	GND_22		GND	
P121	I2C_PM_CK	NAND_CE1_B	I/O	PM dedicated I²C clock
P122	I2C_PM_DAT	NAND_CE2_B	I/O	PM dedicated I²C data
P123	BOOT_SEL0#	I/O-Expander	I	determine module boot dev.
P124	BOOT_SEL1#	I/O-Expander	I	determine module boot dev.
P125	BOOT_SEL2#	I/O-Expander	I	determine module boot dev.
P126	RESET_OUT#	SAI1_RXFS	O	GP reset output
P127	RESET_IN#	PMIC	I	reset (carrier board)
P128	POWER_BTN#	ONOFF	I	PWR button (carrier board)
P129	SER0_TX	UART2_TXD	O	UART0 transmit data
P130	SER0_RX	UART2_RXD	I	UART0 receive data
P131	SER0_RTS#	SAI3_RXC	O	UART0 Request to Send
P132	SER0_CTS#	SAI3_RXD	I	UART0 Clear to Send
P133	GND_23		GND	
P134	SER1_TX	UART1_TXD	O	UART1 transmit data
P135	SER1_RX	UART1_RXD	I	UART1 receive data
P136	SER2_TX	UART4_TXD	O	UART2 transmit data
P137	SER2_RX	UART4_RXD	I	UART2 receive data
P138	SER2_RTS#	NAND_DATA02	O	UART2 Request to Send
P139	SER2_CTS#	NAND_DATA03	I	UART2 Clear to Send
P140	SER3_TX	UART3_TXD	O	UART3 transmit data
P141	SER3_RX	UART3_RXD	I	UART3 receive data
P142	GND_24		GND	
P143	CAN0_TX	SAI5_RXD1	O	CAN0 transmit data
P144	CAN0_RX	SAI5_RXD2	I	CAN0 receive data
P145	CAN1_TX	SAI5_RXD3	O	CAN1 transmit data
P146	CAN1_RX	SAI5_MCLK	I	CAN1 receive data
P147	VDD_IN_1		PWR	
P148	VDD_IN_2		PWR	
P149	VDD_IN_3		PWR	
P150	VDD_IN_4		PWR	
P151	VDD_IN_5		PWR	
P152	VDD_IN_6		PWR	
P153	VDD_IN_7		PWR	
P154	VDD_IN_8		PWR	
P155	VDD_IN_9		PWR	
P156	VDD_IN_10		PWR	

Table 2: Primary Side Connector

Pin	Pin Name	CPU Pad / Connection	I/O	Description
S1	I2C_CAM1_CK	I2C2_SCL	I/O	CAM1 dedicated I²C clock
S2	I2C_CAM1_DAT	I2C2_SDA	I/O	CAM1 dedicated I²C data
S3	GND_25		GND	
S4	RSVD_1		NC	not connected
S5	I2C_CAM0_CK	I2C1_SCL	I/O	CAM0 dedicated I²C clock
S6	CAM_MCK	CLKOUT2	O	master clock
S7	I2C_CAM0_DAT	I2C1_SDA	I/O	CAM0 dedicated I²C data
S8	CSI0_CK+	MIPI_CSI1_CLK_P	I	CSI0 differential clock+
S9	CSI0_CK-	MIPI_CSI1_CLK_N	I	CSI0 differential clock-
S10	GND_26	USB1_RX_P		
S11	CSI0_RX0+	MIPI_CSI1_D0_P	I	CSI0 differential data 0+
S12	CSI0_RX0-	MIPI_CSI1_D0_N	I	CSI0 differential data 0-
S13	GND_27		GND	
S14	CSI0_RX1+	MIPI_CSI1_D1_P	I	CSI0 differential data 1+
S15	CSI0_RX1-	MIPI_CSI1_D1_N	I	CSI0 differential data 1-
S16	GND_28		GND	
S17	GBE1_MDI0+	LAN PHY	I/O	ETH1 MDI differential data 0+
S18	GBE1_MDI0-	LAN PHY	I/O	ETH1 MDI differential data 0-
S19	GBE1_LINK100#	LAN PHY	O	ETH1 link speed indication
S20	GBE1_MDI1+	LAN PHY	I/O	ETH1 MDI differential data 1+
S21	GBE1_MDI1-	LAN PHY	I/O	ETH1 MDI differential data 1-
S22	GBE1_LINK1000#	LAN PHY	O	ETH1 link speed indication
S23	GBE1_MDI2+	LAN PHY	I/O	ETH1 MDI differential data 2+
S24	GBE1_MDI2-	LAN PHY	I/O	ETH1 MDI differential data 2-
S25	GND_29		GND	
S26	GBE1_MDI3+	LAN PHY	I/O	ETH1 MDI differential data 3+
S27	GBE1_MDI3-	LAN PHY	I/O	ETH1 MDI differential data 3-
S28	GBE1_CTREF		NC	not connected
S29	PCIE_D_TX+		NC	not connected
S30	PCIE_D_TX-		NC	not connected
S31	GBE1_LINK_ACT#	LAN PHY	O	ETH1 activity indication
S32	PCIE_D_RX+		NC	not connected
S33	PCIE_D_RX-		NC	not connected
S34	GND_30		GND	
S35	USB4+	USB Hub	I/O	USB4 (USB 2.0 Host) differential data+
S36	USB4-	USB Hub	I/O	USB4 (USB 2.0 Host) differential data-
S37	USB3_VBUS_DET		NC	not connected
S38	AUDIO_MCK	CLKOUT1	O	I²S master clock
S39	I2S0_LRCK	SAI2_TXFS	I/O	I²S0 left & right SYNC clock
S40	I2S0_SDOUT	SAI2_TXD0	O	I²S0 digital audio OUT
S41	I2S0_SDIN	SAI2_RXD0	I	I²S0 digital audio IN
S42	I2S0_CK	SAI2_TXC	I/O	I²S0 digital audio clock

S43	ESPI_ALERT0#		NC	not connected
S44	ESPI_ALERT1#		NC	not connected
S45	MDIO_CLK		NC	not connected
S46	MDIO_DAT		NC	not connected
S47	GND_31		GND	
S48	I2C_GP_CK	I2C3_SCL	I/O	GP dedicated I²C clock
S49	I2C_GP_DAT	I2C3_SDA	I/O	GP dedicated I²C data
S50	I2S2_LRCK	NAND_DATA01	I/O	I²S1 left & right SYNC clock
S51	I2S2_SDOUT	NAND_CE0_B	O	I²S1 digital audio OUT
S52	I2S2_SDIN	NAND_DATA00	I	I²S1 digital audio IN
S53	I2S2_CK	NAND_ALE	I/O	I²S1 digital audio clock
S54	SATA_ACT#		NC	not connected
S55	USB5_EN_OC#		NC	not connected
S56	ESPI_IO_2		NC	not connected
S57	ESPI_IO_3		NC	not connected
S58	ESPI_RESET#		NC	not connected
S59	USB5+		NC	not connected
S60	USB5-		NC	not connected
S61	GND_32		GND	
S62	USB3_SSTX+		NC	not connected
S63	USB3_SSTX-		NC	not connected
S64	GND_33		GND	
S65	USB3_SSRX+		NC	not connected
S66	USB3_SSRX-		NC	not connected
S67	GND_34		GND	
S68	USB3+	USB Hub	I/O	USB3 (USB 2.0 Host) differential data+
S69	USB3-	USB Hub	I/O	USB3 (USB 2.0 Host) differential data-
S70	GND_35		GND	
S71	USB2_SSTX+	USB2_TX_P	O	USB2 (USB 3.0 Host) SS differential transmit data+
S72	USB2_SSTX-	USB2_TX_N	O	USB2 (USB 3.0 Host) SS differential transmit data-
S73	GND_36		GND	
S74	USB2_SSRX+	USB2_RX_P	I	USB2 (USB 3.0 Host) SS differential receive data+
S75	USB2_SSRX-	USB2_RX_N	I	USB2 (USB 3.0 Host) SS differential receive data-
S76	PCIE_B_RST#		NC	not connected
S77	PCIE_B_CLKREQ#		NC	not connected
S78	PCIE_C_RX+		NC	not connected
S79	PCIE_C_RX-		NC	not connected
S80	GND_37		GND	
S81	PCIE_C_TX+		NC	not connected
S82	PCIE_C_TX-		NC	not connected
S83	GND_38		GND	

S84	PCIE_B_REFCK+		NC	not connected
S85	PCIE_B_REFCK-		NC	not connected
S86	GND_39		GND	
S87	PCIE_B_RX+		NC	not connected
S88	PCIE_B_RX-		NC	not connected
S89	GND_40		GND	
S90	PCIE_B_TX+		NC	not connected
S91	PCIE_B_TX-		NC	not connected
S92	GND_41		GND	
S93	DP0_LANE0+		NC	not connected
S94	DP0_LANE0-		NC	not connected
S95	DP0_AUX_SEL		NC	not connected
S96	DP0_LANE1+		NC	not connected
S97	DP0_LANE1-		NC	not connected
S98	DP0_HPD		NC	not connected
S99	DP0_LANE2+		NC	not connected
S100	DP0_LANE2-		NC	not connected
S101	GND_42		GND	
S102	DP0_LANE3+		NC	not connected
S103	DP0_LANE3-		NC	not connected
S104	USB3_OTG_ID		NC	not connected
S105	DP0_AUX+		NC	not connected
S106	DP0_AUX-		NC	not connected
S107	LCD1_BKLT_EN	SAI1_RXD1	O	DISP1 backlight enable
S108	LVDS1_CK+	LVDS1_CLK_P	O	LVDS1 differential clock+
S109	LVDS1_CK-	LVDS1_CLK_N	O	LVDS1 differential clock-
S110	GND_43		GND	
S111	LVDS1_0+	LVDS1_D0_P	O	LVDS1 differential data 0+
S112	LVDS1_0-	LVDS1_D0_N	O	LVDS1 differential data 0-
S113	eDP1_HPD		NC	
S114	LVDS1_1+	LVDS1_D1_P	O	LVDS1 differential data 1+
S115	LVDS1_1-	LVDS1_D1_N	O	LVDS1 differential data 1-
S116	LCD1_VDD_EN	SAI1_RXD0	O	DSIP1 panel PWR enable
S117	LVDS1_2+	LVDS1_D2_P	O	LVDS1 differential data 2+
S118	LVDS1_2-	LVDS1_D2_N	O	LVDS1 differential data 2-
S119	GND_44		GND	
S120	LVDS1_3+	LVDS1_D3_P	O	LVDS1 differential data 3+
S121	LVDS1_3-	LVDS1_D3_N	O	LVDS1 differential data 3-
S122	LCD1_BKLT_PWM	SAI5_RXD0	O	DISP1 brightness control
S123	GPIO13	HDMI_CEC	I/O	
S124	GND_45		GND	
S125	LVDS0_0+	LVDS0_D0_P MIPI_DSI1_D0_P	O	mounting option: LVDS0/DSI differential data 0+
S126	LVDS0_0-	LVDS0_D0_N MIPI_DSI1_D0_N	O	mounting option: LVDS0/DSI differential data 0-

S127	LCD0_BKLT_EN	SAI1_RXC	O	DISP0 backlight enable
S128	LVDS0_1+	LVDS0_D1_P MIPI_DSI1_D1_P	O	mounting option: LVDS0/DSI differential data 1+
S129	LVDS0_1-	LVDS0_D1_N MIPI_DSI1_D1_N	O	mounting option: LVDS0/DSI differential data 1-
S130	GND_46		GND	
S131	LVDS0_2+	LVDS0_D2_P MIPI_DSI1_D2_P	O	mounting option: LVDS0/DSI differential data 2+
S132	LVDS0_2-	LVDS0_D2_N MIPI_DSI1_D2_N	O	mounting option: LVDS0/DSI differential data 2-
S133	LCD0_VDD_EN	SAI1_MCLK	O	DSIP0 panel PWR enable
S134	LVDS0_CK+	LVDS0_CLK_P MIPI_DSI1_CLK_P	O	mounting option: LVDS0/DSI differential clock+
S135	LVDS0_CK-	LVDS0_CLK_N MIPI_DSI1_CLK_N	O	mounting option: LVDS0/DSI differential clock-
S136	GND_47		GND	
S137	LVDS0_3+	LVDS0_D3_P MIPI_DSI1_D3_P	O	mounting option: LVDS0/DSI differential data 3+
S138	LVDS0_3-	LVDS0_D3_N MIPI_DSI1_D3_N	O	mounting option: LVDS0/DSI differential data 3-
S139	I2C_LCD_CK	SPDIF_TX	I/O	DISP dedicated I^2C clock
S140	I2C_LCD_DAT	SPDIF_RX	I/O	DISP dedicated I^2C data
S141	LCD0_BKLT_PWM	SAI3_MCLK	O	DISP0 brightness control
S142	GPIO12	NAND_DQS	I/O	
S143	GND_48		GND	
S144	eDP0_HPD		NC	not connected
S145	WDT_TIME_OUT#	GPIO1_IO01 GPIO1_IO02 (optional)	O	watch-dog-timer
S146	PCIE_WAKE#	SAI3_TXFS	I	PCIe wake up interrupt
S147	VDD_RTC	RTC	PWR	RTC battery PWR
S148	LID#	I/O-Expander	I	Lid open/close indication
S149	SLEEP#	I/O-Expander	I	sleep indicator (carrier)
S150	VIN_PWR_BAD#		I	PWR bad indicator (carrier)
S151	CHARGING#	I/O-Expander	I	Held LOW by carrier during battery charging.
S152	CHARGER_PRSNT#	I/O-Expander	I	Held LOW by carrier if DC input for battery charger is present.
S153	CARRIER_STBY#	OMIC_STBY_REQ	O	module standby indication
S154	CARRIER_PWR_ON	tied to 1V8	O	Carrier circuits should not be powered up until the module asserts this signal.
S155	FORCE_RECOV#	BOOT_MODE3	I	LOW starts USB loader
S156	BATLOW#	I/O-Expander	I	battery low indication
S157	TEST#	I/O-Expander	I	RSVD for testing. Leave floating for normal operation.
S158	GND_49		GND	

Table 3: Secondary Side Connector

4 Interfaces

4.1 USB OTG & Host

The FSSMMX8MP module provides 1x USB 2.0 OTG, 4x USB 2.0 Host & 1x USB 3.0 Host[1].

Pin	Signal	I/O	Voltage	Remarks
USB0				
P60	USB0+	I/O	3.3V	
P61	USB0-	I/O	3.3V	
P62	USB0_EN_OC#	I/O	3.3V	10k PU on module module LOW: disables USB0 PWR carrier LOW: over-current indication
P63	USB0_VBUS_DET	I	5V	
P64	USB0_OTG_ID	I		Host mode: Connect to GND via resistor or directly connect to USB connector.
USB1				
P65	USB1+	I/O	3.3V	
P66	USB1-	I/O	3.3V	
P67	USB1_EN_OC#	I/O	3.3V	10k PU on module module LOW: disables USB1 PWR carrier LOW: over-current indication
USB2				
P69	USB2+	I/O	3.3V	
P70	USB2-	I/O	3.3V	
P71	USB2_EN_OC#	I/O	3.3V	10k PU on module module LOW: disables USB2 PWR carrier LOW: over-current indication
S71	USB2_SSTX+	O	± 500mV	AC-coupling (100nF) on module
S72	USB2_SSTX-	O	± 500mV	
S74	USB2_SSRX+	I	± 500mV	AC-coupling (100nF) on carrier
S75	USB2_SSRX-	I	± 500mV	
USB3				
S68	USB3+	I/O	3.3V	
S69	USB3-	I/O	3.3V	
P74	USB3_EN_OC#	I/O	3.3V	10k PU on module module LOW: disables USB3 PWR carrier LOW: over-current indication
USB4				
S35	USB4+	I/O	3.3V	
S36	USB4-	I/O	3.3V	
P76	USB4_EN_OC#	I/O	3.3V	10k PU on module module LOW: disables USB4 PWR carrier LOW: over-current indication

Table 4: USB Interfaces

[1] The module implements the USB 2.0 Hub USB2514B to increase the number of USB ports. Please contact *sales* to get more information.

4.2 SDIO

The FSSMMX8MP module provides one 4 bit SDIO interface with all necessary signals, needed for a SD card channel.

For specification and licensing please refer to the website of the SD Association *http://www.sdcard.org*.

Pin	Signal	I/O	Voltage	Remarks
P33	SDIO_WP	I	1.8V/3.3V[2]	10k PU on module
P34	SDIO_CMD	I/O	1.8V/3.3V[2]	
P35	SDIO_CD#	I	1.8V/3.3V[2]	10k PU on module
P36	SDIO_CK	O	1.8V/3.3V[2]	
P37	SDIO_PWR_EN	O	3.3V	10k PU on module
P39	SDIO_D0	I/O	1.8V/3.3V[2]	
P40	SDIO_D1	I/O	1.8V/3.3V[2]	
P41	SDIO_D2	I/O	1.8V/3.3V[2]	
P42	SDIO_D3	I/O	1.8V/3.3V[2]	

Table 5: SDIO Interface

[2] 3.3V in standard mode, 1.8V in HS mode

4.3 SPI

The FSSMMX8MP module provides two HS SPI (Serial Peripheral Interface).

Pin	Signal	I/O	Voltage	Remarks
SPI0				
P31	SPI0_CS1#	O	1.8V	
P43	SPI0_CS0#	O	1.8V	
P44	SPI0_CK	O	1.8V	
P45	SPI0_DIN	I	1.8V	
P46	SPI0_DO	O	1.8V	
SPI1				
P54	SPI1_CS0#	O	1.8V	
P55	SPI1_CS1#	O	1.8V	
P56	SPI1_CK	O	1.8V	
P57	SPI1_DIN	I	1.8V	
P58	SPI2_DO	O	1.8V	

Table 6: SPI Interfaces

4.4 I2C

The FSSMMX8MP module provides five useable I²C interfaces[3].

Pin	Signal	I/O	Voltage	Remarks
I2C_GP (General Purpose I²C)				
S48	I2C_GP_CK	I/O	1.8V	2k2 PU on module multi-master capable
S49	I2C_GP_DAT	I/O	1.8V	2k2 PU on module
I2C_LCD (I²C primary dedicated to Flat Panel detection & control)				
S139	I2C_LCD_CK	I/O	1.8V	2k2 PU on module
S140	I2C_LCD_DAT	I/O	1.8V	2k2 PU on module
I2C_HDMI (HDMI control)				
P105	HDMI_CTRL_CK	I/O	1.8V	100k PU on module Level shifter and PUs (5V) shall be placed between module and HDMI connector.
P106	HDMI_CTRL_DAT	I/O	1.8V	100k PU on module Level shifter and PUs (5V) shall be placed between module and HDMI connector.
I2C_CAM0 (I²C primary dedicated to a camera)				
S5	I2C_CAM0_CK	I/O	1.8V	2k2 PU on module multi-master capable
S7	I2C_CAM0_DAT	I/O	1.8V	2k2 PU on module
I2C_CAM1 (I²C primary dedicated to a camera)				
S1	I2C_CAM1_CK	I/O	1.8V	2k2 PU on module multi-master capable
S2	I2C_CAM1_DAT	I/O	1.8V	2k2 PU on module
I2C_PM (I²C primary dedicated to the Power Management)				
P121	I2C_PM_CK	I/O	1.8V	2k2 PU on module multi-master capable
P122	I2C_PM_DAT	I/O	1.8V	2k2 PU on module

Table 7: I²C Interfaces

[3] Most of the I²C interfaces have a dedicated primary function. Internal devices, like RTC, PMIC or Trust Secure Element are connected to a separate I²C interface.

I2C-Bus	Device	Address
I2C_INT	PMIC	0x25
	I/O-Expander	0x40
	SE050	0x48
	Temp. Sensor 1	0x49
	Temp. Sensor 2	0x2C
	RTC	0x51
I2C_GP	EEPROM (module, 24C64)	0x50
	EEPROM (carrier)	0x57

Table 8: I²C Addresses

4.5 UART

The FSSMMX8MP module provides four UART interfaces. The F&S standard software uses DCE mode for UART.

Pin	Signal	I/O	Voltage	Remarks
UART0				
P129	SER0_TX	O	1.8V	
P130	SER0_RX	I	1.8V	100k PU on module
P131	SER0_RTS#	O	1.8V	
P132	SER0_CTS#	I	1.8V	100k PU on module
UART1				
P134	SER1_TX	O	1.8V	
P135	SER1_RX	I	1.8V	100k PU on module
UART2				
P136	SER2_TX	O	1.8V	
P137	SER2_RX	I	1.8V	100k PU on module
P138	SER2_RTS#	O	1.8V	
P139	SER2_CTS#	I	1.8V	100k PU on module
UART3				
P140	SER3_TX	O	1.8V	
P141	SER3_RX	I	1.8V	100k PU on module

Table 9: UART Interfaces

4.6 Ethernet

The FSSMMX8MP module implements up to two Gigabit LAN PHYs (RTL8211FD)[4].

Pin	Signal	I/O	Voltage	Remarks
ETH0				
P29	GBE0_MDI0-	I/O	±1V	
P30	GBE0_MDI0+	I/O	±1V	
P26	GBE0_MDI1-	I/O	±1V	
P27	GBE0_MDI1+	I/O	±1V	
P23	GBE0_MDI2-	I/O	±1V	
P24	GBE0_MDI2+	I/O	±1V	
P19	GBE0_MDI3-	I/O	±1V	
P20	GBE0_MDI3+	I/O	±1V	
P21	GBE0_LINK100#	O	3.3V	
P22	GBE0_LINK1000#	O	3.3V	
P25	GBE0_LINK_ACT#	O	3.3V	
ETH1				
S17	GBE1_MDI0+	I/O	±1V	
S18	GBE1_MDI0-	I/O	±1V	
S20	GBE1_MDI1+	I/O	±1V	
S21	GBE1_MDI1-	I/O	±1V	
S23	GBE1_MDI2+	I/O	±1V	
S24	GBE1_MDI2-	I/O	±1V	
S26	GBE1_MDI3+	I/O	±1V	
S27	GBE1_MDI3-	I/O	±1V	
S19	GBE1_LINK100#	O	3.3V	
S22	GBE1_LINK1000#	O	3.3V	
S31	GBE1_LINK_ACT#	O	3.3V	

Table 10: Ethernet Interfaces

[4] Please contact *sales* to get more information.

4.7 Audio

The FSSMMX8MP module provides two I²S interfaces with a common master clock.

Pin	Signal	I/O	Voltage	Remarks
S38	AUDIO_MCK	O	1.8V	
I2S0				
S39	I2S0_LRCK	I/O	1.8V	
S40	I2S0_SDOUT	O	1.8V	
S41	I2S0_SDIN	I	1.8V	
S42	I2S0_CK	I/O	1.8V	
I2S2[5]				
S50	I2S2_LRCK	I/O	1.8V	
S51	I2S2_SDOUT	O	1.8V	
S52	I2S2_SDIN	I	1.8V	
S53	I2S2_CK	I/O	1.8V	

Table 11: Audio Interfaces

[5] I2S1 from SMARC V1.1 is no part of SMARC V2 anymore.

Use I2C_GP to connect the I²C-interface of the audio codec on the carrier board.

4.8 PCIe

The FSSMMX8MP module supports single lane PCI Express Gen 2. The interface can operate as root complex or endpoint (dual mode operation).

Pin	Signal	I/O	Voltage	Remarks
P86	PCIE_A_RX+	I		AC-coupling (100nF) on carrier
P87	PCIE_A_RX-	I		
P89	PCIE_A_TX+	O		AC-coupling (100nF) on module
P90	PCIE_A_TX-	O		
P83	PCIE_A_REFCK+	O		AC-coupling (100nF) on module
P84	PCIE_A_REFCK-	O		
P75	PCIE_A_RST#	O	3.3V	10k PU on module
P78	PCIE_A_CKREQ#	I	3.3V	10k PU on module
S146	PCIE_WAKE#	I	3.3V	10k PU on module

Table 12: PCIe Interface

4.9 Display Interfaces

4.9.1 LVDS

The FSSMMX8MP module supports dual channel LVDS with up to (1920x1200)pixel & 24 bit[6].

Pin	Signal	I/O	Voltage	Remarks
LVDS0				
S125	LVDS0_0+	O	±200mV	
S126	LVDS0_0-	O	±200mV	
S128	LVDS0_1+	O	±200mV	
S129	LVDS0_1-	O	±200mV	
S131	LVDS0_2+	O	±200mV	
S132	LVDS0_2-	O	±200mV	
S134	LVDS0_CK+	O	±200mV	
S135	LVDS0_CK-	O	±200mV	
S137	LVDS0_3+	O	±200mV	
S138	LVDS0_3-	O	±200mV	
S127	LCD0_BKLT_EN	O	1.8V	
S133	LCD0_VDD_EN	O	1.8V	
S141	LCD0_BKLT_PWM	O	1.8V	
LVDS1				
S111	LVDS1_0+	O	±200mV	
S112	LVDS1_0-	O	±200mV	
S114	LVDS1_1+	O	±200mV	
S115	LVDS1_1-	O	±200mV	
S117	LVDS1_2+	O	±200mV	
S118	LVDS1_2-	O	±200mV	
S108	LVDS1_CK+	O	±200mV	
S109	LVDS1_CK-	O	±200mV	
S120	LVDS1_3+	O	±200mV	
S121	LVDS1_3-	O	±200mV	
S107	LCD1_BKLT_EN	O	1.8V	
S116	LCD1_VDD_EN	O	1.8V	
S122	LCD1_BKLT_PWM	O	1.8V	

Table 13: LVDS Interfaces

4.9.2 MIPI-DSI

The FSSMMX8MP module supports one quad lane MIPI DSI interface with up to 800 Mbps[6]

Pin	Signal	I/O	Voltage	Remarks
LVDS0				
S125	DSI_A_D0+	O	±200mV	
S126	DSI_A_D0-	O	±200mV	
S128	DSI_A_D1+	O	±200mV	
S129	DSI_A_D1-	O	±200mV	
S131	DSI_A_D2+	O	±200mV	
S132	DSI_A_D2-	O	±200mV	
S134	DSI_A_CLK+	O	±200mV	
S135	DSI_A_CLK-	O	±200mV	
S137	DSI_A_D3+	O	±200mV	
S138	DSI_A_D3-	O	±200mV	
S127	LCD0_BKLT_EN	O	1.8V	
S133	LCD0_VDD_EN	O	1.8V	
S141	LCD0_BKLT_PWM	O	1.8V	

Table 14: DSI Interface

MIPI-DSI is a mounting option. Standard configuration is dual channel LVDS.

4.9.3 HDMI

The FSSMMX8MP module supports one HDMI interface[6].

Pin	Signal	I/O	Voltage	Remarks
P98	HDMI_D0+	O		
P99	HDMI_D0-	O		
P95	HDMI_D1+	O		
P96	HDMI_D1-	O		
P92	HDMI_D2+	O		
P93	HDMI_D2-	O		
P101	HDMI_CK+	O		
P102	HDMI_CK-	O		
P104	HDMI_HPD	I	1.8V	1M PD on module

Table 15: DSI Interface

[6] Please contact *sales* to get more information.

4.10 MIPI-CSI

The FSSMMX8MP module supports two MIPI-CSI 2.0 interfaces (1x quad-lane & 1x dual-lane).

See chapter 4.4 I2C for the definition of the serial camera support signals.

Pin	Signal	I/O	Voltage	Remarks
S6	CAM_MCK	O		
CSI0				
S8	CSI0_CK+	I		D-PHY
S9	CSI0_CK-	I		
S11	CSI0_RX0+	I		D-PHY
S12	CSI0_RX0-	I		
S14	CSI0_RX1+	I		D-PHY
S15	CSI0_RX1-	I		
P108	CAM0_PWR#		1.8V	470k PU on module shared with GPIO0
P110	CAM0_RST#		1.8V	470k PU on module shared with GPIO2
CSI1				
P3	CSI1_CK+	I		D-PHY
P4	CSI1_CK-	I		
P7	CSI1_RX0+	I		D-PHY
P8	CSI1_RX0-	I		
P10	CSI1_RX1+	I		D-PHY
P11	CSI1_RX1-	I		
P13	CSI1_RX2+	I		D-PHY
P14	CSI1_RX2-	I		
P16	CSI1_RX3+	I		D-PHY
P17	CSI1_RX3-	I		
P109	CAM1_PWR#		1.8V	470k PU on module shared with GPIO1
P111	CAM1_RST#		1.8V	470k PU on module shared with GPIO3

Table 16: CSI Interfaces

4.11 WLAN and Bluetooth

The FSSMMX8MP module contains a certified high-performance WLAN and Bluetooth module.

The module is based on the NXP W8997 chip, having CE, FCC, IC, NCC, AU/NZ, India, Japan (pre) certificates. Please contact support@fs-net.de for additional information about the process of certification.

The module provides:

- IEEE802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, Bluetooth 3.0 and Bluetooth 5.0 (supports low Energy)

Information about Bluetooth (QDID):

Please refer to the following BT QDID info for 88W8997 (AW-CM276NF).

QDID : D046929

https://launchstudio.bluetooth.com/ListingDetails/91724

If Bluez-5.37 is be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

> **Note:**
> This component is optional and not mounted in all configurations. Please contact *sales* to get more information.

4.12 CAN

The FSSMMX8MP module supports two CAN FD Interfaces.

Pin	Signal	I/O	Voltage	Remarks
P143	CAN0_TX	O	1.8V	
P144	CAN0_RX	I	1.8V	
P145	CAN1_TX	O	1.8V	
P146	CAN1_RX	I	1.8V	

Table 17: CAN FD Interfaces

4.13 GPIOs

All GPIOs are free programmable and can trigger an interrupt.

Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on one of the GPIO contacts.

A higher voltage as the specified IO voltage is not allowed.

Some of the GPIOs have optional functions[7].

Pin	Signal	I/O	Voltage	Remarks
P108	GPIO0	I/O	1.8V	shared with CAM0_PWR#
P109	GPIO1	I/O	1.8V	shared with CAM1_PWR#
P110	GPIO2	I/O	1.8V	shared with CAM0_RST#
P111	GPIO3	I/O	1.8V	shared with CAM1_RST#
P112	GPIO4	I/O	1.8V	
P113	GPIO5	I/O	1.8V	PWM capable
P114	GPIO6	I/O	1.8V	
P115	GPIO7	I/O	1.8V	
P116	GPIO8	I/O	1.8V	
P117	GPIO9	I/O	1.8V	
P118	GPIO10	I/O	1.8V	
P119	GPIO11	I/O	1.8V	
S142	GPIO12	I/O	1.8V	
S123	GPIO13	I/O	1.8V	

Table 18: GPIOs

[7] Please contact *sales* to get more information.

4.14 JTAG

A JTAG connector can be optionally mounted directly on the SOM for debugging purposes.

Pin	Signal	I/O	Voltage	Remarks
J2 #2	JTAG_TMS	I	1.8V	Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU.
J2 #4	LTAG_TCK	I	1.8V	
J2 #6	JTAG_TDO	O	1.8V	
J2 #8	JTAG_TDI	I	1.8V	

Table 19: JTAG

5 Power and Control Pins

Pin	Signal	I/O	Voltage	Remarks
P147 … P156	VDD_IN	PWR	5V	please refer to chapter 9 Electrical Characteristic
S147	VDD_RTC[8]	PWR	3V	please refer to chapter 9 Electrical Characteristic
P128	POWER_BTN#	I	1.8V	10k PU on module
S150	VIN_PWR_BAD#	I	VDD_IN	10k PU on module
P127	RESET_IN#	I	1.8V	10k PU on module Only resets the CPU. In the event of a power failure, VDD_VIN must be switched off and on to avoid latch-up effects.
P126	RESET_OUT#	O	1.8V	10k PD on module
S154	CARRIER_PWR_ON	O	1.8V	
S153	CARRIER_STBY#	O	1.8V	10k PU on module Set LOW when the CPU is in standby mode. This allows to switch off peripheral functions and save more power. Wakeup from standby mode needs support by the driver.
S155	FORCE_RECOV#	I	1.8V	10k PU on module
S145	WDT_TIME_OUT#	O	1.8V	
S148	LID#	I	1.8V	10k PU on module
S149	SLEEP#	I	1.8V	10k PU on module
S156	BATLOW#	I	1.8V	10k PU on module
P1	SMB_ALERT#	I	1.8V	2k2 PU on module
S157	TEST#	I	1.8V	10k PU on module
S151	CHARGING#	I	1.8V	10k PU on module
S152	CHARGER_PRSNT#	I	1.8V	10k PU on module
P123	BOOT_SEL0#	I	1.8V	10k PU on module
P124	BOOT_SEL1#	I	1.8V	10k PU on module
P125	BOOT_SEL2#	I	1.8V	10k PU on module

Table 20: Power & Control Pins

[7] By using a battery for VDD_RTC, you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

6 eMMC

On the FSSMMX8MP module, the fuses of i.MX8MP are configured to boot from eMMC by default. Please contact support for other boot options.

An eMMC v4.41 or higher with 4GB or more from various manufacturers is mounted.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles, and data retention depends on temperature. It is important to know, that high temperature affect the data retention of SLC or MLC flash regardless of whether the device is powered or not. Please contact us if your device is constantly operated in an environment with temperatures above 50°C.

7 RTC

A NXP PCF85263ATL RTC or compatible is used on board. The accuracy is limited because the temperature of the board is not constant. A drift of several seconds per day may be possible at high and low temperatures.

8 Secure Authenticator IC

The secure tamper-resistant authentication IC NXP SE05x offers a strong cryptographic solution intended to be used by device manufacturers to prove the authenticity of their genuine products. It can be used for brand protection, revenue protection, and or customer safety.

For more information visit NXPs web side.

Note:

This component is optional and not mounted in all configurations. Please contact *sales* to get more information.

9 Electrical Characteristic

9.1 Absolute Maximum Ratings

Description	min	max	unit
Input Voltage range 3.3V IOs	-0.3	OVDD+0.3	V
Voltage on any IO with VDD_VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 21: Absolute Maximum Ratings

9.2 DC Electrical Characteristics

Parameter	Description	Condition	min	max	unit
VDD_VIN	Module main power		4.5	5.5	V
VDD_VBAT	RTC power		0.9	5.5	V
USB_VBUS	USB supply voltage		4.4	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_SNVS		3.15	3.45	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	$I_{oh} = 0.1mA$	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	$I_{ol} = 0.1mA$		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VDD_VBAT			0.22[9]	µA

Table 22: DC Electrical Characteristics

[9] Low current: Typical 0.22µA @ VDD_{BAT} = 3.3V & T_{AMB} = 25 °C.

10 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	min	typ	max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	0		+95	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+105	°C
Extended Industrial Range Environmental Temperature (XI)	-40		+85	°C
Extended Industrial Range CPU Junction Temperature (XI)	-40		+105	°C
Junction to Package Top (Ψ_{JT})		0.98		°C /W

Note 1: Maximum junction temperature of the CPU is 95°C / 105°C. In this case cooling is necessary and highly recommended for operations near the limits. See also: Power Consumption and Cooling

Please get in contact with F&S for recommended cooling solutions.

Note 2: WLAN/BT is -30°C to +85°C only. These components are not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

11 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

12 ESD and EMI

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and decrease your shielding requirements. We highly recommend having your baseboard with controlled impedance and wires as short as possible.

13 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

14 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d. Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d. Watt** to **t.b.d. Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14.1 Power Consumption in Suspend to RAM

FSSMMX8MP-V1:
i.MX8M Plus@1.8GHz, 16GB eMMC, 2GB LPDDR4, 2x GBit LAN, WLAN/BT

Power consumption: t.b.d. mW for the full board.

The purpose of the above value is only to give you an idea about the power consumption in "suspend to ram" mode. The value is for the whole board.

15 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months

For longer storage we recommend vacuum dry packs.

16 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

17 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

18 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

19 Appendix

Important Notice

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