Hardware Documentation

FS 8MX OSM™-SF
for HW Revision 1.00

Preliminary

Version 002
(2021-12-20)

Elektronik Systeme

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About This Document

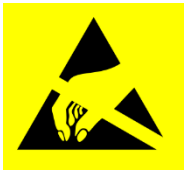
This document describes how to use the FS 8MX OSM™-SF board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

The related standard boards are given in the table below.

Related Modules
FS 8MX OSM™-SF-V1-LIN

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
08.09.2021	001	All		-	Initial Version	GI
07.12.2021	002	All	M	9	Updated	GI

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

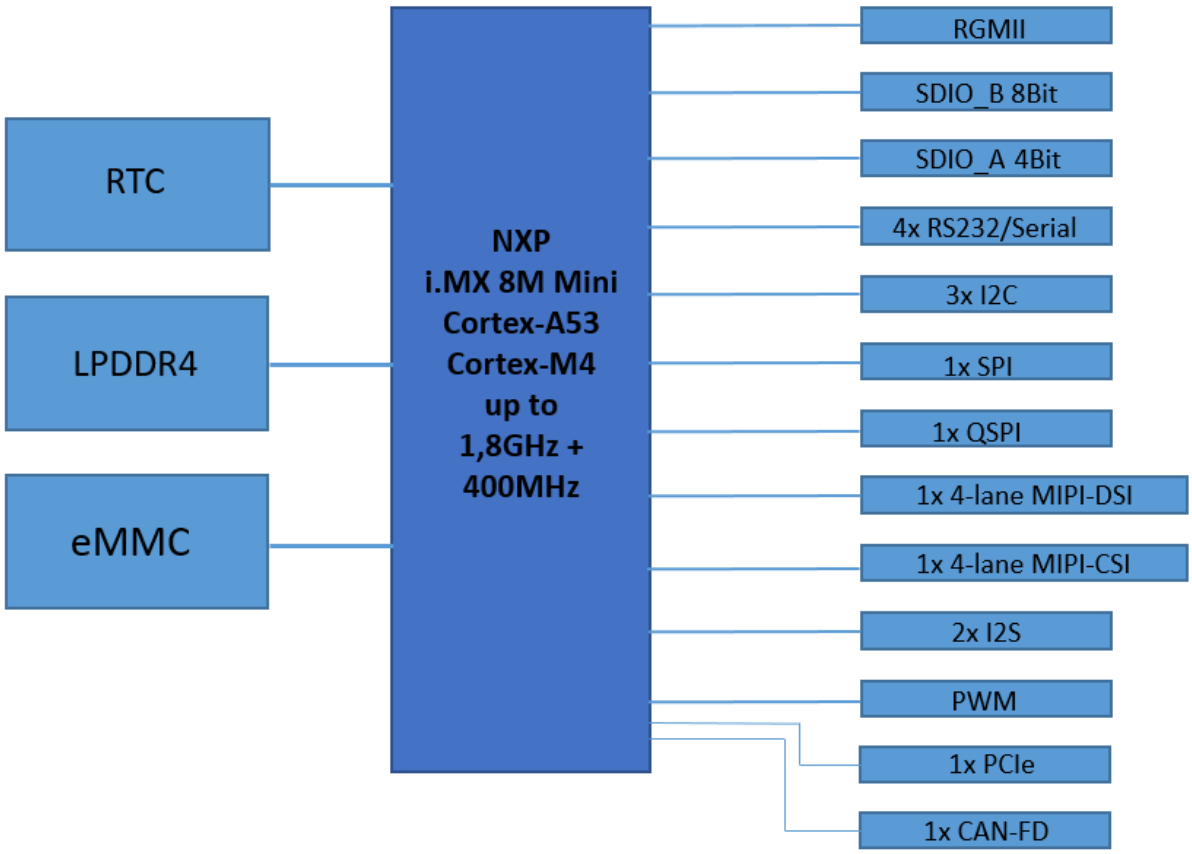

Figure 1 Block diagram

2 Mechanical Dimension

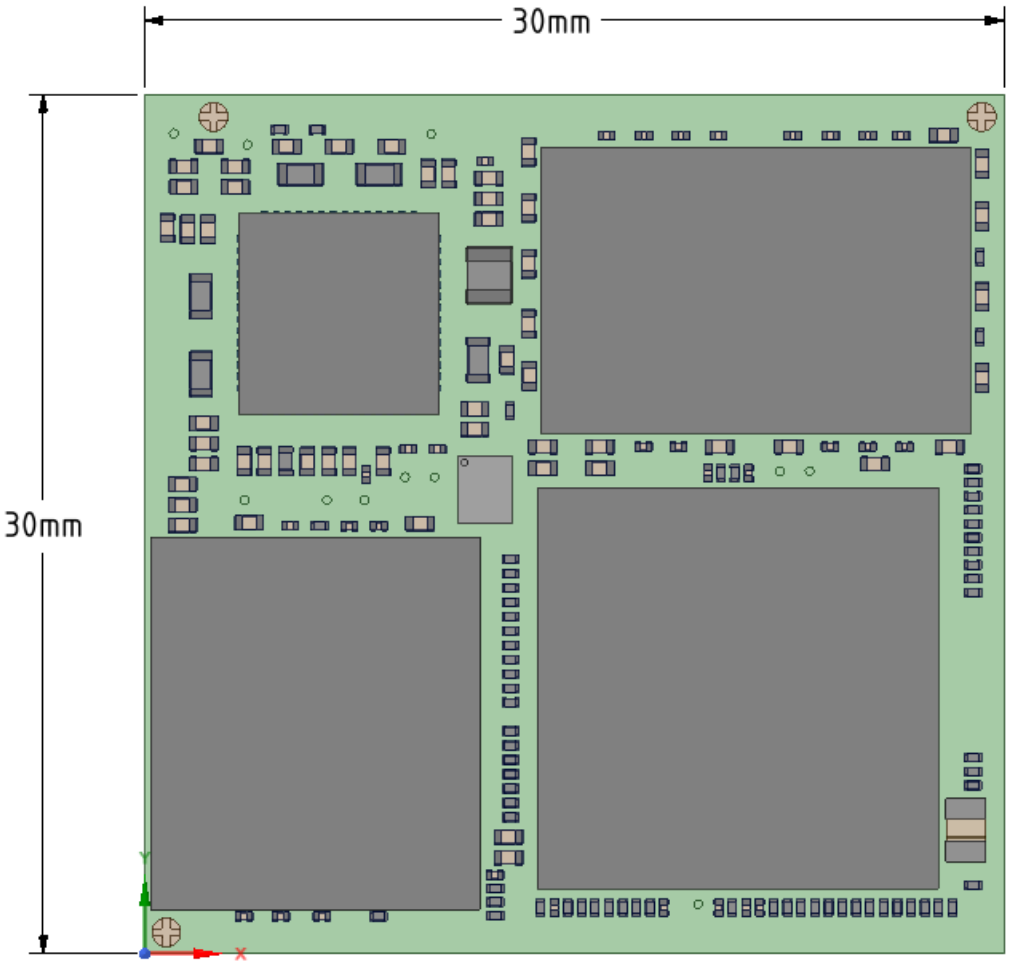

Figure 2 Mechanical Dimensions Top

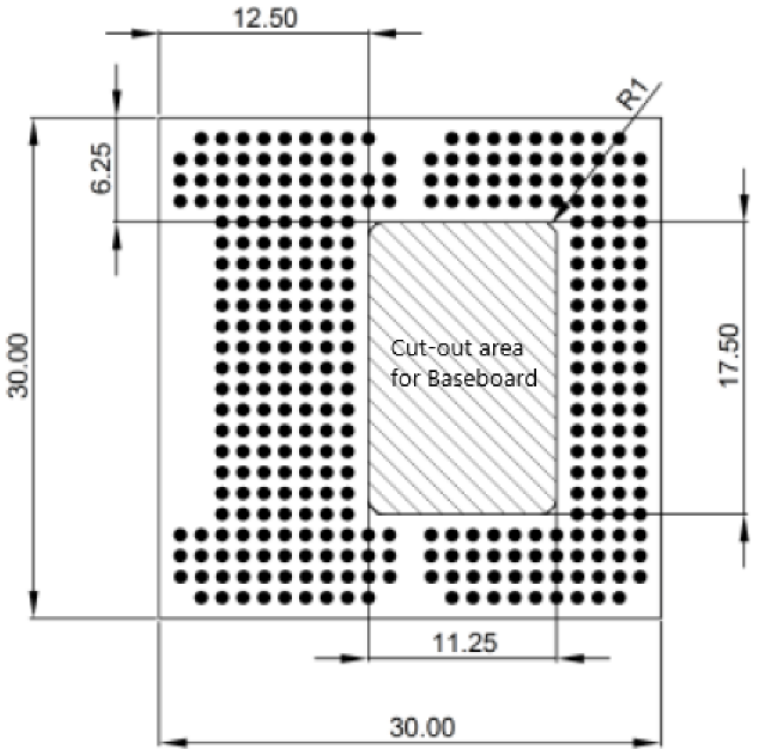

Figure 3 Mechanical Dimensions Bot + cut out area

Dimensions	Description
Size	30mm x 30mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	Max. 1.5mm
Height of the parts on the bottom side	Max. 1.4mm
Weight	Max. 12gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 Contact Grid

The FS 8MX OSM™-SF has to be soldered directly on the carrier board.

The FS 8MX OSM™-SF is using Fused Tin Grid Array (FTGA) for connecting the module PCB to the baseboard PCB.

The baseboard needs to have a cut out area so the components placed on bottom can fit, see marked area in Figure 3 11.25mm x 17.50mm

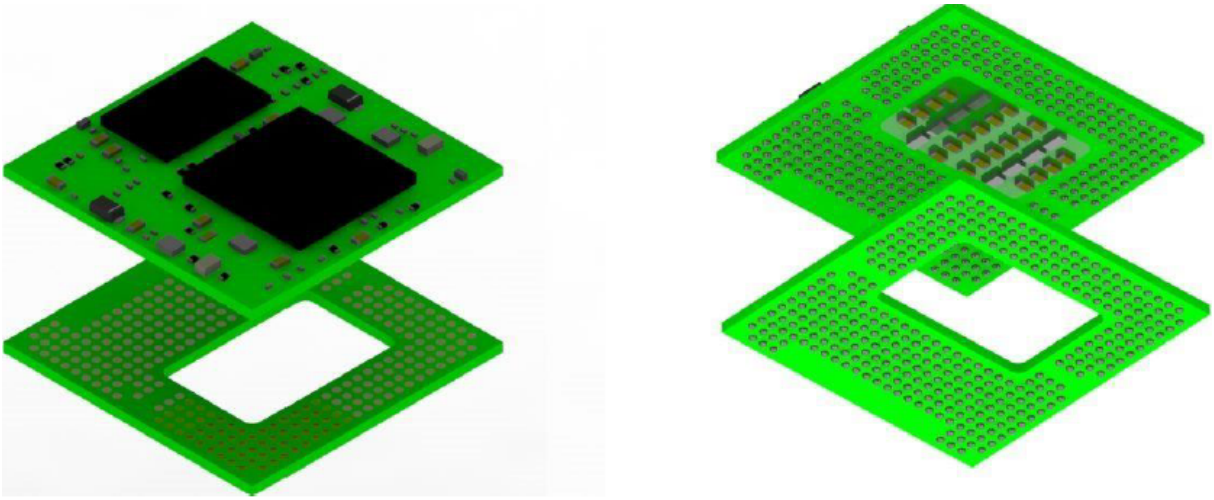

Figure 4 Illustration of cut out area for carrier board

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1E	A2	CSI_DATA1_N	MIPI_CSI_D1_N	I		
J1E	A3	CSI_DATA1_P	MIPI_CSI_D1_P	I		
J1L	A4	GND_A4		PWR	GND	
J1E	A5	CSI_DATA2_N	MIPI_CSI_D2_N	I		
J1E	A6	CSI_DATA2_P	MIPI_CSI_D2_P	I		
J1L	A7	GND_A7		PWR	GND	
J1G	A8	USB_C_SSTX_P	N.C.	X		USB_C not supported
J1G	A9	USB_C_SSTX_N	N.C.	X		USB_C not supported
J1L	A10	GND_A10		PWR	GND	
J1B	A14	UART_A_RX	ECSPI1_SCLK	I	1V8	
J1K	A15	COM_AREA_01	N.C.	X		No antenna supported
J1K	A16	COM_AREA_02	N.C.	X		No antenna supported
J1K	A17	COM_AREA_03	N.C.	X		No antenna supported
J1K	A18	COM_AREA_04	N.C.	X		No antenna supported

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1K	A19	COM_AREA_05	N.C.	X		No antenna supported
J1K	A20	COM_AREA_06	N.C.	X		No antenna supported
J1K	A21	COM_AREA_07	N.C.	X		No antenna supported
J1B	A22	UART_C_RX	UART4_RXD	X	1V8	
J1E	B1	CSI_DATA0_P	MIPI_CSI_D0_P	I		
J1L	B2	GND_B2		PWR	GND	
J1E	B3	CSI_CLK_N	MIPI_CSI_CLK_N	I		
J1E	B4	CSI_CLK_P	MIPI_CSI_CLK_P	I		
J1L	B5	GND_B5		PWR	GND	
J1E	B6	CSI_DATA3_N	MIPI_CSI_D3_N	I		
J1E	B7	CSI_DATA3_P	MIPI_CSI_D3_P	I		
J1L	B8	GND_B8		PWR	GND	
J1L	B9	GND_B9		PWR	GND	
J1G	B10	USB_C_SSRX_P	N.C.	X		Not supported
J1G	B11	USB_C_SSRX_N	N.C.	X		Not supported
J1B	B13	UART_A_TX	ECSPI1_MOSI	O	1V8	
J1K	B15	COM_AREA_08	N.C.	X		No antenna supported
J1K	B16	COM_AREA_09	N.C.	X		No antenna supported
J1K	B17	COM_AREA_10	N.C.	X		No antenna supported
J1K	B18	COM_AREA_11	N.C.	X		No antenna supported
J1K	B19	COM_AREA_12	N.C.	X		No antenna supported
J1K	B20	COM_AREA_13	N.C.	X		No antenna supported
J1K	B21	COM_AREA_14	N.C.	X		No antenna supported
J1J	B22	CLKOUT2	CLKOUT2	O	1V8	F&S defined extra Output
J1B	B23	UART_C_TX	UART4_TXD	O	1V8	
J1E	C1	CSI_DATA0_N	MIPI_CSI_D0_N	I		
J1E	C2	CAM_MCK	CLKOUT1	O	1V8	
J1E	C3	I2C_CAM_SDA	SAI2_TXC	I/O	1V8	Onboard Pull-Up 2k2
J1E	C4	I2C_CAM_SCL	SAI2_TXFS	I/O	1V8	Onboard Pull-Up 2k2
J1L	C5	VCC_6_TEST		O	1V1	Test pin, leave open
J1J	C6	N.C.				Reserved Pin, leave open
J1J	C7	N.C.				Reserved Pin, leave open
J1G	C8	USB_C_OC#	N.C.	X		USB_C not supported
J1G	C9	USB_C_VBUS	N.C.	X		USB_C not supported
J1G	C10	USB_C_EN	N.C.	X		USB_C not supported
J1L	C11	GND_C11		PWR		

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1B	C13	UART_A_RTS	ECSPI1_MISO	O	1V8	
J1B	C14	UART_A_CTS	ECSPI1_SS0	I	1V8	
J1K	C15	COM_AREA_15	N.C.	X		No antenna supported
J1J	C16	SD_B_VCC	N.C.	O	3V3/1V8	Selectable voltage*2
J1K	C17	COM_AREA_16	N.C.	X		No antenna supported
J1J	C18	TEST_GENERIC	N.C.	X		Not connected
J1K	C19	COM_AREA_17	N.C.	X		No antenna supported
J1C	C20	SD_A_VCC	N.C.	O	3V3/1V8	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA *2
J1K	C21	COM_AREA_18	N.C.	X		No antenna supported
J1B	C22	UART_D_RX	N.C.	X		Not connected
J1B	C23	UART_D_TX	N.C.	X		Not connected
J1L	D1	GND_D1		PWR	GND	
J1A	D2	ETH_B_MII_CRS	N.C.	X		ETH_B not supported
J1I	D3	GPIO_C_0	SAI1_TXD4	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	D4	GPIO_C_1	SAI1_TXD0	I/O	1V8	Standard GPIO, only with Mini CPU
J1L	D5	GND_D5		PWR	GND	
J1J	D6	N.C.				Reserved Pin, leave open
J1J	D7	N.C.				Reserved Pin, leave open
J1L	D8	GND_D8		PWR	GND	
J1G	D9	USB_C_ID	N.C.	X		USB_C not supported
J1G	D10	USB_C_D_P	N.C.	X		USB_C not supported
J1G	D11	USB_C_D_N	N.C.	X		USB_C not supported
J1B	D13	UART_B_TX	SAI2_RXFS	O	1V8	
J1B	D14	UART_B_RX	SAI2_RXC	I	1V8	
J1B	D15	UART_B_RTS	UART3_RXD	O	1V8	
J1B	D16	UART_B_CTS	UART3_TXD	I	1V8	
J1I	D17	GPIO_A_0	SAI3_MCLK	I/O	1V8	Standard GPIO
J1L	D18	GND_D18		PWR	GND	
J1I	D19	GPIO_B_0	SAI1_RXD6	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	D20	SDIO_A_WP	SD2_WP	I	SD_A_VCC	Tie to GND on carrier, if not used
J1C	D21	SDIO_A_PWR_EN	SD2_RESET_B	O	SD_A_VCC	Power enable for SD card
J1B	D22	UART_CON_RX	SAI3_TXFS	I	1V8	UART Debug

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1B	D23	UART_CON_TX	SAI3_TXC	O	1V8	UART Debug
J1A	E1	ETH_B_MII_COL	N.C.	X		ETH_B not supported
J1L	E2	GND_E2		PWR	GND	
J1I	E3	GPIO_C_2	SAI1_TXC	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	E4	GPIO_C_3	SAI1_TXFS	I/O	1V8	Standard GPIO, only with Mini CPU
J1L	E15	GND_E15		PWR	GND	
J1A	E16	ETH_A_MII_CRS	N.C.	X		CRS not supported
J1I	E17	GPIO_A_1	SAI3_TXD	I/O	1V8	Standard GPIO
J1J	E18	PWM_1	SPDIF_EXT_CLK	O	1V8	Standard PWM
J1I	E19	GPIO_B_1	SAI1_RXD5	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	E20	SDIO_A_CMD	SD2_CMD	I/O	SD_A_VCC	Command/Response, onboard 100k pull-up
J1L	E21	GND_E21		PWR	GND	
J1A	F1	ETH_B_MII_TXD1	N.C.	X		ETH_B not supported
J1A	F2	ETH_B_MII_TXD3	N.C.	X		ETH_B not supported
J1I	F3	GPIO_C_4	SAI1_MCLK	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	F4	GPIO_C_5	SAI1_RXD3	I/O	1V8	Standard GPIO, only with Mini CPU
J1A	F15	ETH_A_MII_COL	N.C.	X		COL not supported
J1L	F16	GND_F16		PWR	GND	
J1I	F17	GPIO_A_2	SAI3_RXFS	I/O	1V8	Standard GPIO
J1J	F18	PWM_2	SPDIF_RX	O	1V8	Standard PWM
J1I	F19	GPIO_B_2	SAI1_RXD4	I/O	1V8	Standard GPIO, only with Mini CPU
J1L	F20	GND_F20		PWR	GND	
J1C	F21	SDIO_A_CLK	SD2_CLK	O	SD_A_VCC	
J1A	G1	ETH_B_MII_TXD0	N.C.	X		ETH_B not supported
J1A	G2	ETH_B_MII_TXD2	N.C.	X		ETH_B not supported
J1E	G3	CAM_PWR	SAI5_RXD1	O	1V8	
J1E	G4	CAM_RST#	SAI5_RXD2	O	1V8	
J1A	G15	ETH_A_MII_TXD1	ENET_TD1	O	NVCC_RGMII	Optional 1V8, _N when used as differential
J1A	G16	ETH_A_MII_TXD3	ENET_TD3	O	NVCC_RGMII	Optional 1V8
J1I	G17	GPIO_A_3	SAI3_RXC	I/O	1V8	Standard GPIO
J1J	G18	PWM_3	SPDIF_TX	O	1V8	Standard PWM
J1I	G19	GPIO_B_3	SAI1_RXD0	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	G20	SDIO_A_D0	SD2_DATA0	I/O	SD_A_VCC	Onboard pull-up 100k

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1C	G21	SDIO_A_D1	SD2_DATA1	I/O	SD_A_VCC	
J1A	H1	ETH_B_MII_TX_CLK	N.C.	X		ETH_B not supported
J1L	H2	GND_H2		PWR	GND	
J1F	H3	RGB_CS#	N.C.	X		RGB not supported
J1L	H4	GND_H4		PWR	GND	
J1A	H15	ETH_A_MII_TXD0	ENET_TD0	O	NVCC_RGMII	Optional 1V8, _P when used as differential
J1A	H16	ETH_A_MII_TXD2	ENET_TD2	O	NVCC_RGMII	Optional 1V8
J1I	H17	GPIO_A_4	SAI3_RXD	I/O	1V8	Standard GPIO
J1J	H18	PWM_3	N.C.	X		PWM_3 not supported
J1I	H19	GPIO_B_4	SAI1_RXC	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	H20	SDIO_A_D2	SD2_DATA2	I/O	SD_A_VCC	
J1C	H21	SDIO_A_D3	SD2_DATA3	I/O	SD_A_VCC	
J1A	J1	ETH_B_MII_RXD0	N.C.	X		ETH_B not supported
J1A	J2	ETH_B_MII_TX_EN	N.C.	X		ETH_B not supported
J1F	J3	RGB_RESET#	N.C.	X		RGB not supported
J1F	J4	RGB_DE	N.C.	X		RGB not supported
J1A	J15	ETH_A_MII_TX_CLK	ENET_TXC	I/O	NVCC_RGMII	Optional 1V8
J1L	J16	GND_J16		PWR	GND	
J1I	J17	GPIO_A_5	SAI2_RXD0	I/O	1V8	Standard GPIO
J1J	J18	PWM_4	N.C.	X		PWM_4 not supported
J1J	J19	GPIO_B_5	SAI1_RXFS	I/O	1V8	Standard GPIO, only with Mini CPU
J1L	J20	GND_J20		PWR	GND	
J1C	J21	SDIO_A_CD#	SD2_CD_B	I	SD_A_VCC	
J1A	K1	ETH_B_MII_RXD1	N.C.	X		ETH_B not supported
J1A	K2	ETH_B_MII_RX_ER	N.C.	X		ETH_B not supported
J1F	K3	RGB_HSYNC	N.C.	X		RGB not supported
J1F	K4	RGB_DISP	N.C.	X		RGB not supported
J1A	K15	ETH_A_MII_RXD0	ENET_RD0	I	NVCC_RGMII	Optional 1V8
J1A	K16	ETH_A_MII_TX_EN	ENET_TX_CTL	O	NVCC_RGMII	Optional 1V8
J1I	K17	GPIO_A_6	SAI2_TXD0	I/O	1V8	Standard GPIO
J1J	K18	PWM_5	N.C.	X		PWM_5 not supported
J1I	K19	GPIO_B_6	SAI1_TXD6	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	K20	SDIO_B_CLK	SD1_CLK	O	SD_B_VCC	
J1C	K21	SDIO_B_CMD	SD1_CMD	I/O	SD_B_VCC	Onboard Pull-Up 100k
J1A	L1	ETH_B_MII_RX_DV	N.C.	X		ETH_B not supported
J1L	L2	GND_L2		PWR	GND	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1F	L3	RGB_VSYNC	N.C.	X		RGB not supported
J1L	L4	GND_L4		PWR	GND	
J1A	L15	ETH_A_MII_RXD1	ENET_RD1	I	NVCC_RGMII	Optional 1V8
J1A	L16	ETH_A_MII_RX_ER	N.C.	X		Error Receive not supported
J1I	L17	GPIO_A_7	SAI1_RXD7	I/O	1V8	Standard GPIO, only with Mini CPU
J1L	L18	GND_L18		PWR	GND	
J1I	L19	GPIO_B_7	SAI1_TXD5	I/O	1V8	Standard GPIO, only with Mini CPU
J1C	L20	SDIO_B_D0	SD1_DATA0	I/O	SD_B_VCC	Onboard Pull-Up 100k
J1C	L21	SDIO_B_D1	SD1_DATA1	I/O	SD_B_VCC	
J1A	M1	ETH_B_MII_RXD2	N.C.	X		ETH_B not supported
J1A	M2	ETH_B_SDP	N.C.	X		ETH_B not supported
J1F	M3	RGB_B5	N.C.	X		RGB not supported
J1F	M4	RGB_CLK	N.C.	X		RGB not supported
J1A	M15	ETH_A_MII_RX_DV (ER)	ENET_RX_CTL	I	NVCC_RGMII	Data Valid Signal, optional 1V8
J1L	M16	GND_M16		PWR	GND	
J1L	M17	VCC_1_TEST	N.C.	O	0V8	Test pin, leave open
J1J	M18	ADC_0	N.C.	X		ADC not supported
J1J	M19	VCC_2_TEST	N.C.	O	0V9	Test pin, leave open
J1J	M20	GND_M20		PWR	GND	
J1C	M21	SDIO_B_D2	SD1_DATA2	I/O	SD_B_VCC	
J1A	N1	ETH_B_MII_RXD3	N.C.	X		ETH_B not supported
J1J	N2	RESERVED_N2	N.C.	X		Reserved Pin, leave open
J1F	N3	RGB_B3	N.C.	X		RGB not supported
J1F	N4	RGB_B4	N.C.	X		RGB not supported
J1A	N15	ETH_A_MII_RXD2	ENET_RD2	I	NVCC_RGMII	Optional 1V8
J1A	N16	ETH_A_SDP	N.C.	X		SDP not supported
J1J	N17	JTAG_TCK	JTAG_TCK	I	1V8	
J1J	N18	ADC_1	N.C.	X		ADC not supported
J1J	N19	JTAG_TMS	JTAG_TMS	I	1V8	
J1C	N20	SDIO_B_D3	SD1_DATA3	I/O	SD_B_VCC	
J1C	N21	SDIO_B_D4	SD1_DATA4	I/O	SD_B_VCC	
J1A	P1	ETH_B_MII_RX_CLK	N.C.	X		ETH_B not supported
J1L	P2	GND_P2		PWR	GND	
J1F	P3	RGB_B2	N.C	X		RGB not supported
J1L	P4	GND_P4		PWR	GND	

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1A	P15	ETH_A_MII_RXD3	ENET_RD3	I	NVCC_RGMII	Optional 1V8
J1J	P16	NVCC_RGMII		PWR	1V8	connect with ETH Phy on carrier board, or power NVCC_RGMII via mounting option
J1J	P17	JTAG_TDI	JTAG_TDI	I	1V8	
J1L	P18	GND_P18		PWR	GND	
J1J	P19	JTAG_RTCK	N.C.	X		RTCK not supported
J1C	P20	SDIO_B_D5	SD1_DATA5	I/O	SD_B_VCC	
J1C	P21	SDIO_B_D6	SD1_DATA6	I/O	SD_B_VCC	
J1L	R1	GND_R1		PWR	GND	
J1D	R2	PCIe_SM_ALERT#	SAI1_RXD2	I	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2
J1F	R3	RGB_B1	N.C.	X		RGB not supported
J1F	R4	RGB_B0	N.C.	X		RGB not supported
J1A	R15	ETH_A_MII_RX_CLK	ENET_RXC	I/O	NVCC_RGMII	Optional 1V8
J1L	R16	GND_R16		PWR	GND	
J1J	R17	JTAG_TDO	JTAG_TDO	O	1V8	
J1J	R18	RESERVED_R18	N.C.	X		Reserved Pin, leave open
J1J	R19	JTAG_nTRST	JTAG_TRST_B	I	1V8	
J1L	R20	GND_R20		PWR	GND	
J1C	R21	SDIO_B_D7	SD1_DATA7	I/O	SD_B_VCC	
J1D	T1	PCIe_SMCLK	SAI1_TXD3	O	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2
J1D	T2	PCIE_WAKE#	GPIO1_IO00	I	3V3	PCIe only with Mini CPU, onboard Pull-Up 10k
J1F	T3	RGB_G4	N.C.	X		RGB not supported
J1F	T4	RGB_G5	N.C.	X		RGB not supported
J1A	T15	ETH_MDIO	ENET_MDIO	I/O	NVCC_RGMII	Optional 1V8
J1A	T16	ETH_MDC	ENET_MDC	O	NVCC_RGMII	Optional 1V8
J1J	T17	RESERVED_T17	N.C.	X		Reserved Pin, leave open
J1J	T18	RESERVED_T18	N.C.	X		Reserved Pin, leave open
J1J	T19	RESERVED_T19	N.C.	X		Reserved Pin, leave open
J1C	T20	SD_B_VCC	N.C.	PWR, O	3V3/1V8	SDIO B Voltage. It is used to provide the IO Voltage Level ,100mA max current*2

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1C	T21	SDIO_B_CD#	GPIO1_IO06	I	SD_B_VCC	Active low card detect
J1D	U1	PCIe_SMDAT	SAI1_TXD2	I/O	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2
J1L	U2	GND_U2		PWR	GND	
J1F	U3	RGB_G3	N.C.	X		RGB not supported
J1L	U4	GND_U4		PWR	GND	
J1I	U15	QSPI_A_SDI_IO0	NAND_DATA00	I/O	1V8	QSPI
J1I	U16	QSPI_A_SCK	NAND_ALE	I/O	1V8	QSPI
J1L	U17	SYS_RST#	N.C.	I	1V8	Reset input from carrier board*2
J1L	U18	VCC_OUT_IO	N.C.	O	1V8/3V3	Selectable voltage via jumper*2
J1J	U19	BOOT_SEL#	BOOT_MODE0	I	1V8	If low on carrier board, OSM boots from carrier boot medium, onboard Pull-Up 10k
J1C	U20	SDIO_B_WP	GPIO1_IO07	I	3V3	Tie to GND on carrier, if not used, onboard Pull-Up 10k
J1C	U21	SDIO_B_PWR_EN	SD1_RESET_B	O	SD_B_VCC	
J1L	V1	GND_V1		PWR	GND	
J1D	V2	PCIe_A_PERST#	GPIO1_IO01	O	3V3	PCIe only with Mini
J1F	V3	I2C_C_SCL /RGB_G1	I2C3_SCL	I/O	1V8	I2C_C led out to RGB_G1, RGB not supported, onboard Pull-Up 2,2k*1
J1F	V4	RGB_G2	N.C.	X		RGB not supported
J1I	V15	QSPI_A_SDO_IO1	NAND_DATA01	I/O	1V8	QSPI
J1L	V16	GND_V16		PWR	GND	
J1L	V17	CPU_POR_B	POR_B	O	1V8	Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN Signal, Optional 1V8 fix*2
J1H	V18	I2S_MCLK	SAI5_MCLK	I/O	1V8	
J1H	V19	I2S_B_DATA_IN	SAI1_RXD1	I/O	1V8	I2S_B only with Mini CPU
J1L	V20	GND_V20		PWR	GND	
J1H	V21	I2S_A_DATA_IN	SAI5_RXD0	I/O	1V8	
J1D	W1	PCIe_REF_CLK_P	PCIE_CLK_P	O		PCIe only with Mini
J1D	W2	PCIe_A_PRSNT#	GPIO1_IO04	I	3V3	PCIe only with Mini, onboard Pull-Up 10k

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1L	W3	GND_W3		PWR	GND	
J1F	W4	I2C_C_SDA/RGB_G0	I2C3_SDA	I/O	1V8	I2C_C led out to RGB_G0, RGB not supported, onboard Pull-Up 2,2k*1
J1I	W15	QSPI_A_/HOLD_IO3	NAND_DATA03	I/O	1V8	QSPI
J1I	W16	QSPI_A_/WP_IO2	NAND_DATA02	I/O	1V8	QSPI
J1L	W17	RTC_PWR	N.C.	PWR	3V	Low current RTC circuit backup power. May be sourced from a Carrier based Lithium cell or Super Cap.*2
J1H	W18	I2S_LRCLK	SAI5_RXFS	I/O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
J1H	W19	I2S_B_DATA_OUT	SAI1_TXD1	I/O	1V8	I2S_B only with Mini CPU
J1H	W20	I2S_BITCLK	SAI5_RXC	I/O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU act in Slave Mode
J1H	W21	I2S_A_DATA_OUT	SAI5_RXD3	I/O	1V8	
J1D	Y1	PCIe_REF_CLK_N	PCIE_CLK_N	O		PCIe only with Mini
J1L	Y2	GND_Y2		PWR	GND	
J1L	Y3	VCC_5_TEST	N.C.	O	1V8	Test pin, leave open
J1F	Y4	GPIO1_IO03/RGB_R5	GPIO1_IO03	I/O	3V3	Standard GPIO1_IO03 led out to RGB_R5, RGB not supported*1
J1F	Y5	GPIO1_IO09/RGB_R4	GPIO1_IO09	I/O	3V3	Standard GPIO1_IO09 led out to RGB_R4, RGB not supported*1
J1F	Y6	GPIO1_IO10/RGB_R2	GPIO1_IO10	I/O	3V3	Standard GPIO1_IO10 led out to RGB_R2, RGB not supported*1
J1F	Y7	GPIO1_IO11/RGB_R0	GPIO1_IO11	I/O	3V3	Standard GPIO1_IO11 led out to RGB_R0, RGB not supported*1
J1L	Y8	VCC_IN_5V_Y8	N.C.	PWR	5V	Power Input OSM*2
J1L	Y9	VCC_IN_5V_Y9	N.C.	PWR	5V	Power Input OSM*2
J1L	Y10	VCC_IN_5V_Y10	N.C.	PWR	5V	Power Input OSM*2
J1L	Y11	VCC_IN_5V_Y11	N.C.	PWR	5V	Power Input OSM*2
J1J	Y13	RESERVED_Y13	N.C.			Reserved Pin, leave open
J1J	Y14	RESERVED_Y14	N.C.			Reserved Pin, leave open

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1I	Y15	QSPI_A_CS#	NAND_CE0_B	O	1V8	QSPI
J1L	Y16	VCC_3_TEST	N.C.	O	0V9	Test pin, leave open
J1L	Y17	VCC_IN_5V_Y17	N.C.	PWR	5V	Power Input OSM*2
J1L	Y18	GND_Y18		PWR	GND	
J1L	Y19	VCC_IN_3V3	N.C.	X		Not connected*2
J1L	Y20	VCC_4_TEST	N.C.	O	3V3	Test pin, leave open
J1I	Y21	SPI_B_SCK	ECSPI2_SCLK	O	1V8	
J1I	Y22	SPI_B_SDI	ECSPI2_MOSI	I	1V8	
J1I	Y23	SPI_B_SDO	ECSPI2_MISO	O	1V8	
J1L	AA1	GND_AA1		PWR	GND	
J1J	AA2	RESERVED_AA2	N.C.	X		Reserved Pin, leave open
J1E	AA3	DSI_TE	N.C.	X		DSI-TE not supported
J1L	AA4	GND_AA4		PWR	GND	
J1F	AA5	RGB_R3	N.C.	X		RGB not supported
J1F	AA6	RGB_R1	N.C.	X		RGB not supported
J1L	AA7	GND_AA7		PWR	GND	
J1L	AA8	GND_AA8		PWR	GND	
J1L	AA9	PWR_BTN#	ONOFF	I	1V8	Power-button from Carrier board.
J1L	AA10	GND_AA10		PWR	GND	
J1L	AA11	GND_AA11		PWR	GND	
J1J	AA13	RESERVED_AA13	N.C.	X		Reserved Pin, leave open
J1L	AA14	GND_AA14		PWR	GND	
J1I	AA15	I2C_A_SCL	I2C1_SCL	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1I	AA16	I2C_A_SDA	I2C1_SDA	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1L	AA17	GND_AA17		PWR	GND	
J1L	AA18	V_BAT_AA18	N.C.	X		Not connected, leave open*2
J1L	AA19	GND_AA19		PWR	GND	
J1I	AA20	I2C_B_SCL	I2C2_SCL	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1I	AA21	I2C_B_SDA	I2C2_SDA	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1L	AA22	GND_AA22		PWR	GND	
J1I	AA23	SPI_B_CS#	ECSPI2_SS0	O	1V8	
J1D	AB1	PCIe_A_HSI0_P	PCIE_RXN_P	I		PCIe only with Mini, AC coupled off module

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1D	AB2	PCIe_A_HSI0_N	PCIE_RXN_N	I		PCIe only with Mini, AC coupled off module
J1L	AB3	GND_AB3		PWR	GND	
J1E	AB4	DSI_DATA3_P	MIPI_DSI_D3_P	O		
J1E	AB5	DSI_DATA3_N	MIPI_DSI_D3_N	O		
J1L	AB6	GND_AB6		PWR	GND	
J1E	AB7	DSI_CLOCK_P	MIPI_DSI_CLK_P	O		
J1E	AB8	DSI_CLOCK_N	MIPI_DSI_CLK_N	O		
J1L	AB9	GND_AB9		PWR	GND	
J1E	AB10	DSI_DATA0_P	MIPI_DSI_D0_P	O		
J1E	AB11	DSI_DATA0_N	MIPI_DSI_D0_N	O		
J1G	AB13	USB_A_D_N	USB1_DN	I/O	USB	
J1G	AB14	USB_A_ID	USB1_ID	I	3V3	
J1L	AB15	GND_AB15		PWR	GND	
J1G	AB16	USB_A_VBUS	USB1_VBUS	I	VBUS 5V	*2
J1B	AB17	CAN_A_RX	N.C.	I	1V8	CAN-FD
J1L	AB18	V_BAT_AB18	N.C.	X		Not connected
J1B	AB19	CAN_B_RX	N.C.	X		Not connected
J1G	AB20	USB_B_VBUS	USB2_VBUS	I	VBUS 5V	Only with Mini CPU*2
J1L	AB21	GND_AB21		PWR	GND	
J1G	AB22	USB_B_ID	USB2_ID	I	3V3	Only with Mini CPU
J1G	AB23	USB_B_D_N	USB2_DN	I/O	USB	
J1D	AC2	PCIe_A_HSO0_P	PCIE_TXN_P	O		PCIe only with Mini, AC coupled off module
J1D	AC3	PCIe_A_HSO0_N	PCIE_TXN_N	O		PCIe only with Mini, AC coupled off module
J1L	AC4	GND_AC4		PWR	GND	
J1E	AC5	DSI_DATA2_P	MIPI_DSI_D2_P	O	1V8	
J1E	AC6	DSI_DATA2_N	MIPI_DSI_D2_N	O	1V8	
J1L	AC7	GND_AC7		PWR	GND	
J1E	AC8	DSI_DATA1_P	MIPI_DSI_D1_P	O	1V8	
J1E	AC9	DSI_DATA1_N	MIPI_DSI_D1_N	O	1V8	
J1L	AC10	GND_AC10		PWR	GND	
J1G	AC14	USB_A_D_P	USB1_DP	I/O	USB	
J1G	AC15	USB_A_OC#	GPIO1_IO13	I	3V3	
J1G	AC16	USB_A_EN	GPIO1_IO12	O	3V3	
J1B	AC17	CAN_A_TX	N.C.	O	1V8	CAN-FD
J1J	AC18	DEBUG_EN	N.C.	X		Not connected
J1B	AC19	CAN_B_TX	N.C.	X		Not connected

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1G	AC20	USB_B_EN	GPIO1_IO14	O	3V3	
J1G	AC21	USB_B_OC#	GPIO1_IO15	I	3V3	
J1G	AC22	USB_B_D_P	USB2_DP	I/O	USB	Only with Mini CPU

Table 2: B2B connector

*1: The module does not support the RGB-Interface. These contacts are connected with GPIOs or I2C_C.

*2: Please see Chapter 7 for further information about these power & control contacts.

4 Interfaces

4.1 USB 2.0

FS 8MX OSM-SF board with Mini CPU can support 1x USB HOST Mode and 1x USB OTG. FS 8MX OSM-SF board with Nano can only support 1x USB OTG (USB_A). The 90 Ohm differential pair of USB signals doesn´t need any termination. For external ports on carrier board ESD and EMV protection is required nearby the USB connectors.
If the USB will be used in Host Mode, contact USB_ID must be connected to GND via a pull down resistor. Otherwise it must be directly connected to the USB connector.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1G	AB16	USB_A_VBUS	USB1_VBUS	I	VBUS 5V	
J1G	AB13	USB_A_D_N	USB1_DN	I/O	USB	
J1G	AC14	USB_A_D_P	USB1_DP	I/O	USB	
J1G	AB14	USB_A_ID	USB1_ID	I	3V3	
J1G	AC15	USB_A_OC#	GPIO1_IO13	I	3V3	
J1G	AC16	USB_A_EN	GPIO1_IO12	O	3V3	
J1G	AB20	USB_B_VBUS	USB2_VBUS	I	VBUS 5V	Only with Mini CPU
J1G	AB23	USB_B_D_N	USB2_DN	I/O	USB	Only with Mini CPU
J1G	AC22	USB_B_D_P	USB2_DP	I/O	USB	Only with Mini CPU
J1G	AB22	USB_B_ID	USB2_ID	I	3V3	Only with Mini CPU
J1G	AC21	USB_B_OC#	GPIO1_IO15	I	3V3	
J1G	AC20	USB_B_EN	GPIO1_IO14	O	3V3	

Table 3 USB A/B Interface Connections

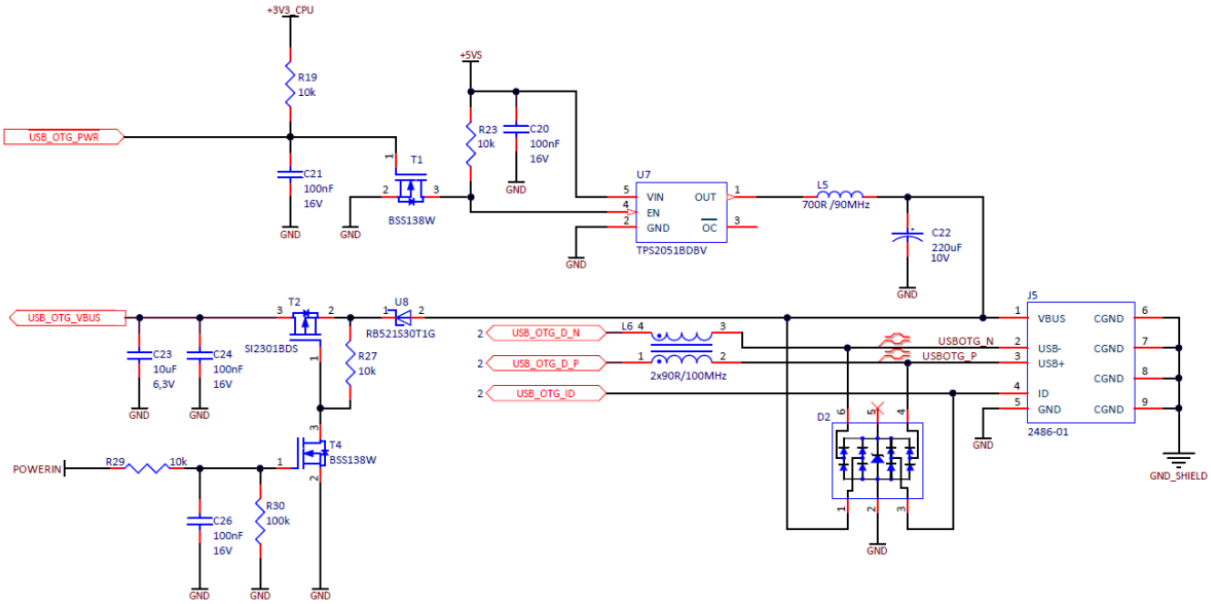

Figure 5 USB OTG example connection on carrier board

4.2 SD Card Interface A

This interface is supporting a 4Bit SD card channel.

For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The Supply voltage of SD_A (SD_A_VCC) can be set to 1.8V or 3.3V via mounting option

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1C	C20	SD_A_VCC	NVCC_SD2	PWR, O	3V3/1V8	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA
J1C	D21	SDIO_A_PWR_EN	SD2_RESET_B	O	SD_A_VCC	Power enable for SD card, onboard pull-up 10k
J1C	G20	SDIO_A_D0	SD2_DATA0	I/O	SD_A_VCC	Onboard pull-up 100k
J1C	G21	SDIO_A_D1	SD2_DATA1	I/O	SD_A_VCC	
J1C	H20	SDIO_A_D2	SD2_DATA2	I/O	SD_A_VCC	
J1C	H21	SDIO_A_D3	SD2_DATA3	I/O	SD_A_VCC	
J1C	E20	SDIO_A_CMD	SD2_CMD	I/O	SD_A_VCC	Command/Response, onboard 100k pull-up
J1C	J21	SDIO_A_CD#	SD2_CD_B	I	SD_A_VCC	Active low, card detect, onboard pull-up 10k
J1C	D20	SDIO_A_WP	SD2_WP	I	SD_A_VCC	Tie to GND on carrier, if not used, onboard pull-up 10k
J1C	F21	SDIO_A_CLK	SD2_CLK	O	SD_A_VCC	

Table 4 SD Card A Interface

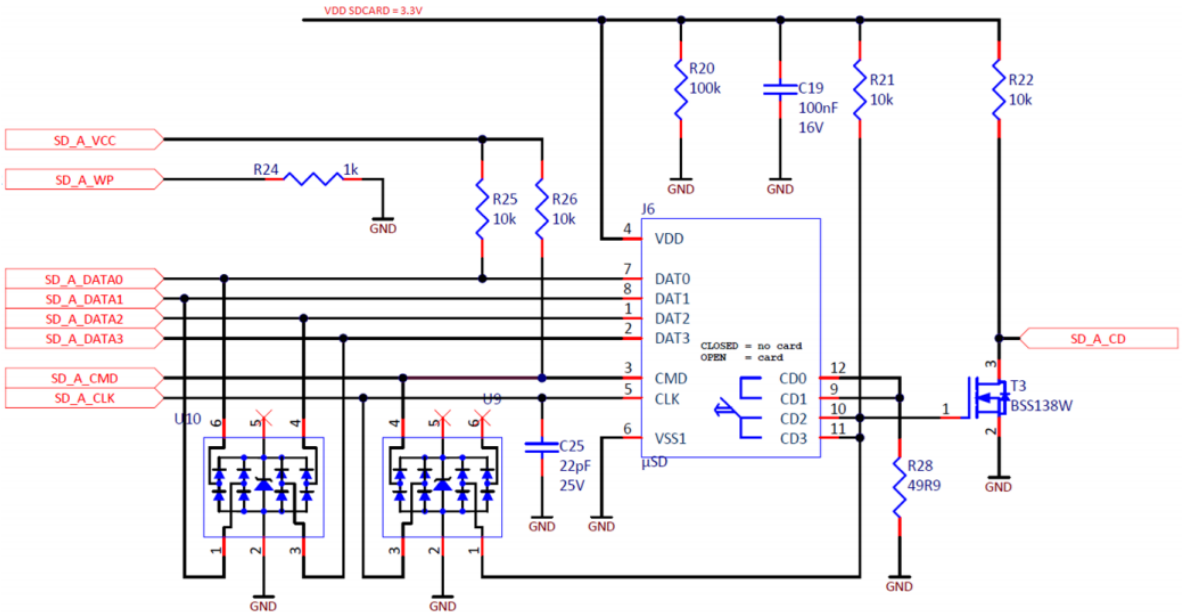

Figure 6 SD Card Connector example connection on carrier board

4.3 SD Card Interface B

This interface is supporting a 8Bit SD/MMC interface.

For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

The Supply voltage of SD_B (SD_B_VCC) is configured by the driver (1.8V or 3.3V)

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1C	T20	SD_B_VCC	NVCC_SD1	PWR, O	3V3/1V8	SDIO B Voltage. It is used to provide the IO Voltage Level ,100mA max current
J1C	U21	SDIO_B_PWR_EN	SD1_RESET_B	O	SD_B_VCC	
J1C	L20	SDIO_B_D0	SD1_DATA0	I/O	SD_B_VCC	Onboard pull-up 100k
J1C	L21	SDIO_B_D1	SD1_DATA1	I/O	SD_B_VCC	
J1C	M21	SDIO_B_D2	SD1_DATA2	I/O	SD_B_VCC	
J1C	N20	SDIO_B_D3	SD1_DATA3	I/O	SD_B_VCC	
J1C	N21	SDIO_B_D4	SD1_DATA4	I/O	SD_B_VCC	
J1C	P20	SDIO_B_D5	SD1_DATA5	I/O	SD_B_VCC	
J1C	P21	SDIO_B_D6	SD1_DATA6	I/O	SD_B_VCC	
J1C	R21	SDIO_B_D7	SD1_DATA7	I/O	SD_B_VCC	
J1C	K21	SDIO_B_CMD	SD1_CMD	I/O	SD_B_VCC	Onboard Pull-Up 100k
J1C	T21	SDIO_B_CD#	GPIO1_IO06	I	SD_B_VCC	Active low card detect, onboard pull-up 10k
J1C	U20	SDIO_B_WP	GPIO1_IO07	I	3V3	Tie to GND on carrier, if not used, onboard Pull-Up 10k
J1C	K20	SDIO_B_CLK	SD1_CLK	O	SD_B_VCC	

Table 5 SD Card B Interface

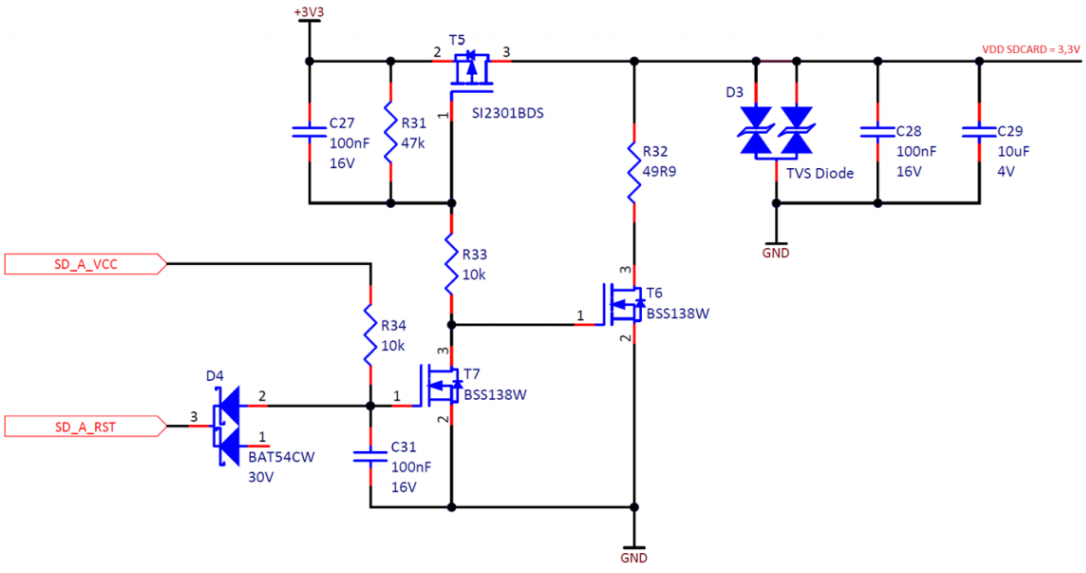

Figure 7 SD Card B supply voltage switching circuit example on carrier board

4.4 QSPI Interface

The module supports one QSPI Interface with 1.8V voltage level.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1I	U15	QSPI_A_SDI_IO0	NAND_DATA00	I/O	1V8	QSPI
J1I	V15	QSPI_A_SDO_IO1	NAND_DATA01	I/O	1V8	QSPI
J1I	W16	QSPI_A_/WP_IO2	NAND_DATA02	I/O	1V8	QSPI
J1I	W15	QSPI_A_/HOLD_IO3	NAND_DATA03	I/O	1V8	QSPI
J1I	U16	QSPI_A_SCK	NAND_ALE	I/O	1V8	QSPI
J1I	Y15	QSPI_A_CS#	NAND_CE0_B	O	1V8	QSPI

Table 6 QSPI Interface

4.5 SPI Interface

The module supports SPI (Serial Peripheral Interface). All signals are 1.8V compliant. Devices on carrier board with other voltage levels need a level shifter.
Signals don´t have Pull-Ups on module.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1I	Y21	SPI_B_SCK	ECSPI2_SCLK	O	1V8	
J1I	Y22	SPI_B_SDI	ECSPI2_MOSI	I	1V8	
J1I	Y23	SPI_B_SDO	ECSPI2_MISO	O	1V8	
J1I	AA23	SPI_B_CS#	ECSPI2_SS0	O	1V8	

Table 7 SPI Interface

4.6 I2C

The modules supports up to 3 I2C Interfaces. Devices on baseboard with other voltage need a level shifter.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1F	V3	I2C_C_SCL /RGB_G1	I2C3_SCL	I/O	1V8	I2C_C led out to RGB_G1, RGB not supported, onboard Pull-Up 2,2k
J1F	W4	I2C_C_SDA/RGB_G0	I2C3_SDA	I/O	1V8	I2C_C led out to RGB_G0, RGB not supported, onboard Pull-Up 2,2k
J1I	AA15	I2C_A_SCL	I2C1_SCL	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1I	AA16	I2C_A_SDA	I2C1_SDA	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1I	AA20	I2C_B_SCL	I2C2_SCL	I/O	1V8	Not shared, onboard Pull-Up 2,2k
J1I	AA21	I2C_B_SDA	I2C2_SDA	I/O	1V8	Not shared, onboard Pull-Up 2,2k

Table 8 I2C Interface

Note:

If PCIe I2C and MIPI CSI I2C is used as software solution then I2C_C is not shared and led out to RGB_G1/G0 (only possible with i.MX8M Mini processor since PCIe is only supported by Mini CPU).

I2C_C is led out to the RGB connector with 1.8V voltage level.

4.7 Serial Interface (UART)

FS 8MX OSM-SF module provides 4 UART channels
(2x UART with flow control signals RTS and CTS, 2x standard RX and TX).
We recommend to use UART_CON for debugging and service only.
F&S standard software uses DCE mode for UART

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1B	C13	UART_A_RTS	ECSPI1_MISO	O	1V8	
J1B	C14	UART_A_CTS	ECSPI1_SS0	I	1V8	Onboard pull-up 100k
J1B	A14	UART_A_RX	ECSPI1_SCLK	I	1V8	Onboard pull-up 100k
J1B	B13	UART_A_TX	ECSPI1_MOSI	O	1V8	
J1B	D15	UART_B_RTS	UART3_RXD	O	1V8	
J1B	D16	UART_B_CTS	UART3_TXD	I	1V8	Onboard pull-up 100k
J1B	D14	UART_B_RX	SAI2_RXC	I	1V8	Onboard pull-up 100k
J1B	D13	UART_B_TX	SAI2_RXFS	O	1V8	
J1B	A22	UART_C_RX	UART4_RXD	X	1V8	Onboard pull-up 100k
J1B	B23	UART_C_TX	UART4_TXD	O	1V8	
J1B	D22	UART_CON_RX	SAI3_TXFS	I	1V8	UART Debug, onboard pull-up 100k
J1B	D23	UART_CON_TX	SAI3_TXC	O	1V8	UART Debug

Table 9 UART Interface Signals

4.8 Ethernet

The FS 8MX OSM-SF supports one 10/100/1000Mbit LAN interface via RGMII signals.

An external Ethernet-PHY (i.e. AR8035-AL1A…) or an external switch (i.e. KSZ9893R…) is required.

The Ethernet data signals need to be connected to the Ethernet-PHY as 100-Ohm differential pairs.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1A	E16	ETH_A_MII_CRS	N.C.	X		CRS not supported
J1A	F15	ETH_A_MII_COL	N.C.	X		COL not supported
J1A	H15	ETH_A_MII_TXD0	ENET_TD0	O	NVCC_RGMII	Optional 1V8, _P when used as differential
J1A	G15	ETH_A_MII_TXD1	ENET_TD1	O	NVCC_RGMII	Optional 1V8, _P when used as differential
J1A	H16	ETH_A_MII_TXD2	ENET_TD2	O	NVCC_RGMII	Optional 1V8
J1A	G16	ETH_A_MII_TXD3	ENET_TD3	O	NVCC_RGMII	Optional 1V8
J1A	K16	ETH_A_MII_TX_EN	ENET_TX_CTL	O	NVCC_RGMII	Optional 1V8
J1A	J15	ETH_A_MII_TX_CLK	ENET_TXC	I/O	NVCC_RGMII	Optional 1V8
J1A	K15	ETH_A_MII_RXD0	ENET_RD0	I	NVCC_RGMII	Optional 1V8, _P when used as differential
J1A	L15	ETH_A_MII_RXD1	ENET_RD1	I	NVCC_RGMII	Optional 1V8, _N when used as differential
J1A	N15	ETH_A_MII_RXD2	ENET_RD2	I	NVCC_RGMII	Optional 1V8
J1A	P15	ETH_A_MII_RXD3	ENET_RD3	I	NVCC_RGMII	Optional 1V8
J1A	L16	ETH_A_MII_RX_ER	N.C.	X		Error Receive not supported
J1A	M15	ETH_A_MII_RX_DV (ER)	ENET_RX_CTL	I	NVCC_RGMII	Data Valid Signal, optional 1V8
J1A	R15	ETH_A_MII_RX_CLK	ENET_RXC	I/O	NVCC_RGMII	Optional 1V8
J1A	N16	ETH_A_SDP	N.C.	X		SDP not supported
J1A	T15	ETH_MDIO	ENET_MDIO	I/O	NVCC_RGMII	Optional 1V8
J1A	T16	ETH_MDC	ENET_MDC	O	NVCC_RGMII	Optional 1V8

Table 10 RGMII Interface (no Ethernet PHY)

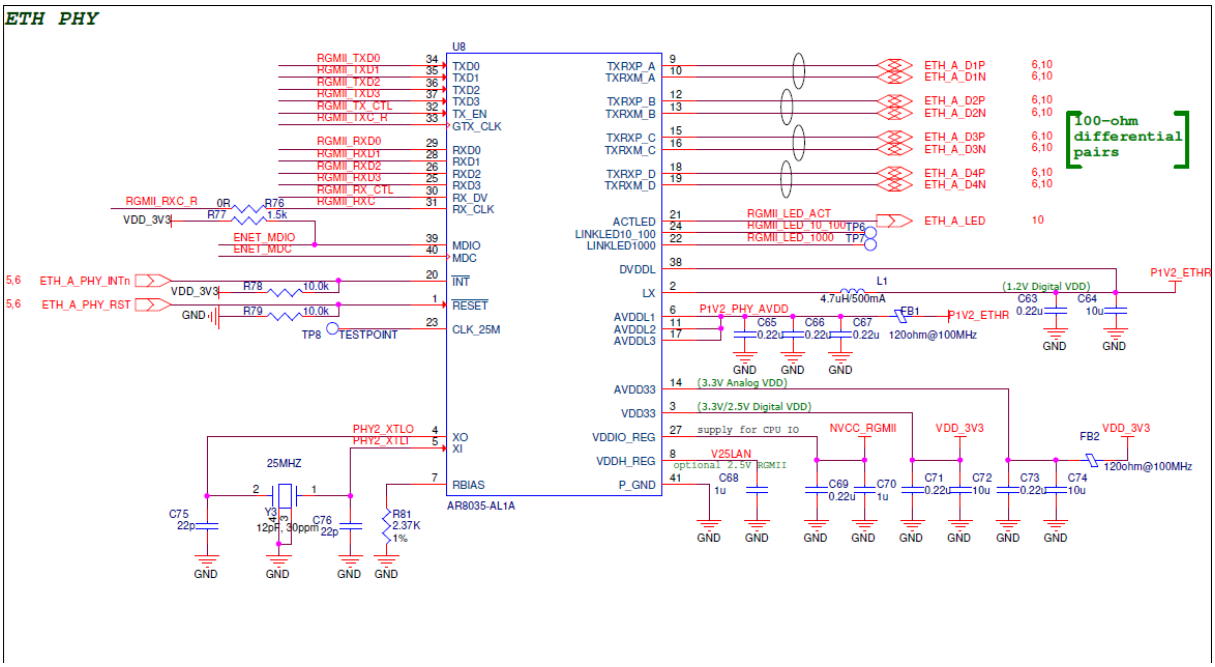

Figure 8 RGMII to Ethernet PHY example

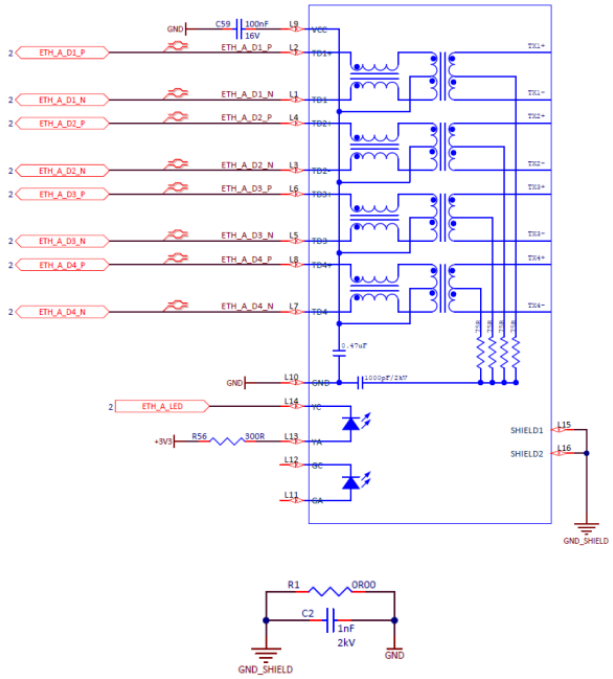

Figure 9 Ethernet PHY to LAN connector example

4.9 Audio (I2S)

The module supports only I2S signals. An external audio codec IC (i.e. SGTL500…) on the carrier board is needed for Audio output.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1H	V21	I2S_A_DATA_IN	SAI5_RXD0	I/O	1V8	
J1H	W21	I2S_A_DATA_OUT	SAI5_RXD3	I/O	1V8	
J1H	V19	I2S_B_DATA_IN	SAI1_RXD1	I/O	1V8	I2S_B only with Mini CPU
J1H	W19	I2S_B_DATA_OUT	SAI1_TXD1	I/O	1V8	I2S_B only with Mini CPU
J1H	V18	I2S_MCLK	SAI5_MCLK	I/O	1V8	
J1H	W18	I2S_LRCLK	SAI5_RXFS	I/O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
J1H	W20	I2S_BITCLK	SAI5_RXC	I/O	1V8	Module Output if CPU acts in Master Mode Module Input if CPU act in Slave Mode

Table 11 Audio Interface (without Codec)

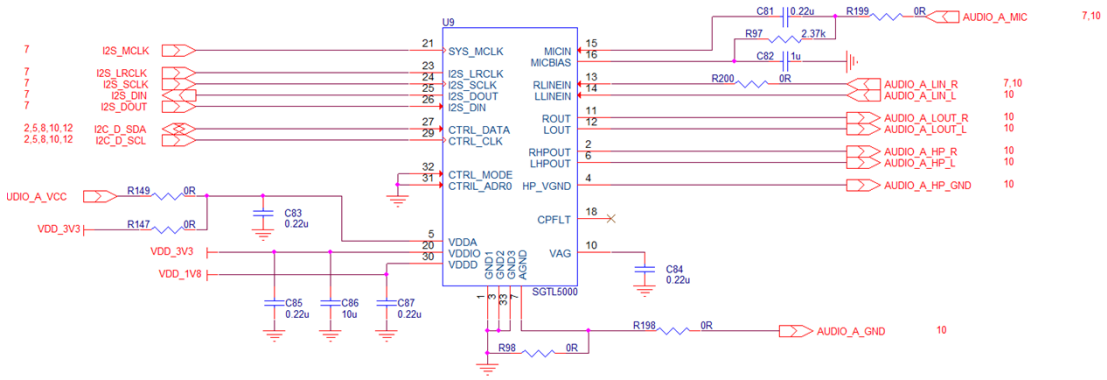

Figure 10 SGTL5000 Codec circuit example for carrier board

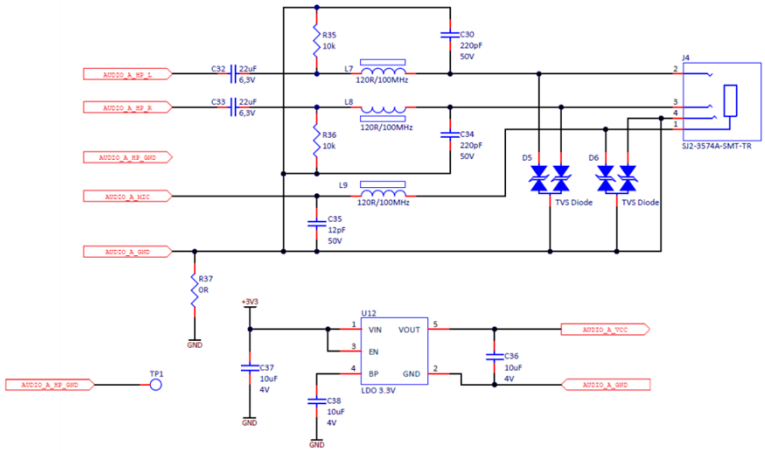

Figure 11 Headphone-Out Mic-In example circuit for carrier board

4.10 PCIE Interface

FS 8MX OSM-SF supports single lane PCI Express Gen 2. The interface can work as root complex or endpoint (Dual mode operation).

mPCIe Interface is only supported with i.MX8M Mini Processor based modules.

Modules with i.MX8M Nano Processor do not have mPCIe option and the related pins on the contact grid are N.C!

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1D	AB1	PCIe_A_HSI0_P	PCIE_RXN_P	I		PCIe only with Mini, AC coupled off module
J1D	AB2	PCIe_A_HSI0_N	PCIE_RXN_N	I		PCIe only with Mini, AC coupled off module
J1D	AC2	PCIe_A_HSO0_P	PCIE_TXN_P	O		PCIe only with Mini, AC coupled off module
J1D	AC3	PCIe_A_HSO0_N	PCIE_TXN_N	O		PCIe only with Mini, AC coupled off module
J1D	W2	PCIe_A_PRSNT#	GPIO1_IO04	I	3V3	PCIe only with Mini, onboard Pull-Up 10k
J1D	V2	PCIe_A_PERST#	GPIO1_IO01	O	3V3	PCIe only with Mini
J1D	W1	PCIe_REF_CLK_P	PCIE_CLK_P	O		PCIe only with Mini
J1D	Y1	PCIe_REF_CLK_N	PCIE_CLK_N	O		PCIe only with Mini
J1D	T2	PCIE_WAKE#	GPIO1_IO00	I	3V3	PCIe only with Mini CPU, onboard Pull-Up 10k
J1D	U1	PCIe_SMDAT	SAI1_TXD2	I/O	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2
J1D	T1	PCIe_SMCLK	SAI1_TXD3	O	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2
J1D	R2	PCIe_SM_ALERT#	SAI1_RXD2	I	1V8	PCIe only with Mini CPU, onboard Pull-Up 2k2

PCIe_SM-DAT/CLK (I2C_C) is available as Software or Hardware solution

If PCIe I2C and MIPI CSI I2C is used as software solution then I2C_C is not shared and led out to RGB_G1/G0 (only possible with i.MX8M Mini processor since PCIe is only supported by Mini CPU).

4.11 MIPI DSI

The module supports one quad lane MIPI DSI interface (up to 800 Mbps).

The signals can be connected directly to a MIPI compliant display.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1E	AB10	DSI_DATA0_P	MIPI_DSI_D0_P	O	1.2V/200mV*1	
J1E	AB11	DSI_DATA0_N	MIPI_DSI_D0_N	O	1.2V/200mV*1	
J1E	AC8	DSI_DATA1_P	MIPI_DSI_D1_P	O	1.2V/200mV*1	
J1E	AC9	DSI_DATA1_N	MIPI_DSI_D1_N	O	1.2V/200mV*1	
J1E	AC5	DSI_DATA2_P	MIPI_DSI_D2_P	O	1.2V/200mV*1	
J1E	AC6	DSI_DATA2_N	MIPI_DSI_D2_N	O	1.2V/200mV*1	
J1E	AB4	DSI_DATA3_P	MIPI_DSI_D3_P	O	1.2V/200mV*1	
J1E	AB5	DSI_DATA3_N	MIPI_DSI_D3_N	O	1.2V/200mV*1	
J1E	AB8	DSI_CLOCK_N	MIPI_DSI_CLK_N	O	1.2V/200mV*1	
J1E	AB7	DSI_CLOCK_P	MIPI_DSI_CLK_P	O	1.2V/200mV*1	
J1E	AA3	DSI_TE	N.C.	X		DSI-TE not supported

*1 : 1.2V in single-ended mode, approx. 200mV in differential mode

4.12 MIPI CSI Interface

The module supports one quad lance MIPI CSI interface

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1E	C1	CSI_DATA0_N	MIPI_CSI_D0_N	I		
J1E	B1	CSI_DATA0_P	MIPI_CSI_D0_P	I		
J1E	A2	CSI_DATA1_N	MIPI_CSI_D1_N	I		
J1E	A3	CSI_DATA1_P	MIPI_CSI_D1_P	I		
J1E	A5	CSI_DATA2_N	MIPI_CSI_D2_N	I		
J1E	A6	CSI_DATA2_P	MIPI_CSI_D2_P	I		
J1E	B6	CSI_DATA3_N	MIPI_CSI_D3_N	I		
J1E	B7	CSI_DATA3_P	MIPI_CSI_D3_P	I		
J1E	B3	CSI_CLK_N	MIPI_CSI_CLK_N	I		
J1E	B4	CSI_CLK_P	MIPI_CSI_CLK_P	I		
J1E	C2	CAM_MCK	CLKOUT1	O	1V8	
J1E	C3	I2C_CAM_SDA	SAI2_TXC	I/O	1V8	Onboard Pull-Up 2k2
J1E	C4	I2C_CAM_SCL	SAI2_TXFS	I/O	1V8	Onboard Pull-Up 2k2
J1E	G3	CAM_PWR	SAI5_RXD1	O	1V8	
J1E	G4	CAM_RST#	SAI5_RXD2	O	1V8	

I2C_CAM(I2C_C) is available as Software or Hardware solution

If PCIe I2C and MIPI CSI I2C is used as software solution then I2C_C is not shared and led out to RGB_G1/G0 (only possible with i.MX8M Mini processor since PCIe is only supported by Mini CPU).

4.13 CAN FD Interface

The FS 8MX OSM-SF supports the CAN FD Interface with an external controller onboard.

The module comes with MCP2518FD CAN controller IC which uses one of SPI channel (SPI_CAN).

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1B	AC17	CAN_A_TX		O	1V8	CAN-FD
J1B	AB17	CAN_A_RX		I	1V8	CAN-FD

4.14 GPIOs

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it´s not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced I/O power is not allowed.

GPIO_A0 - _A6 is available with i.MX8M Mini and Nano CPU

GPIO_A7 - _C5 is only available with i.MX8M Mini CPU

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1I	D17	GPIO_A_0	SAI3_MCLK	I/O	1V8	Standard GPIO
J1I	E17	GPIO_A_1	SAI3_TXD	I/O	1V8	Standard GPIO
J1I	F17	GPIO_A_2	SAI3_RXFS	I/O	1V8	Standard GPIO
J1I	G17	GPIO_A_3	SAI3_RXC	I/O	1V8	Standard GPIO
J1I	H17	GPIO_A_4	SAI3_RXD	I/O	1V8	Standard GPIO
J1I	J17	GPIO_A_5	SAI2_RXD0	I/O	1V8	Standard GPIO
J1I	K17	GPIO_A_6	SAI2_TXD0	I/O	1V8	Standard GPIO
J1I	L17	GPIO_A_7	SAI1_RXD7	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	D19	GPIO_B_0	SAI1_RXD6	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	E19	GPIO_B_1	SAI1_RXD5	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	F19	GPIO_B_2	SAI1_RXD4	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	G19	GPIO_B_3	SAI1_RXD0	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	H19	GPIO_B_4	SAI1_RXC	I/O	1V8	Standard GPIO, only with Mini CPU
J1J	J19	GPIO_B_5	SAI1_RXFS	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	K19	GPIO_B_6	SAI1_TXD6	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	L19	GPIO_B_7	SAI1_TXD5	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	D3	GPIO_C_0	SAI1_TXD4	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	D4	GPIO_C_1	SAI1_TXD0	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	E3	GPIO_C_2	SAI1_TXC	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	E4	GPIO_C_3	SAI1_TXFS	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	F3	GPIO_C_4	SAI1_MCLK	I/O	1V8	Standard GPIO, only with Mini CPU
J1I	F4	GPIO_C_5	SAI1_RXD3	I/O	1V8	Standard GPIO, only with Mini CPU

4.15 JTAG

JTAG is for debug only.

Leave unconnected, if you don´t use JTAG

Don´t put them in a JTAG chain, because different power sequence and power level could kill the CPU

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1J	N17	JTAG_TCK	JTAG_TCK	I	1V8	
J1J	N19	JTAG_TMS	JTAG_TMS	I	1V8	
J1J	P17	JTAG_TDI	JTAG_TDI	I	1V8	
J1J	P19	JTAG_RTCK	N.C.	X		RTCK not supported
J1J	R17	JTAG_TDO	JTAG_TDO	O	1V8	
J1J	R19	JTAG_nTRST	JTAG_TRST_B	I	1V8	
J1J	AC18	DEBUG_EN	N.C.	X		Not connected
J1J	C18	TEST_GENERIC	N.C.	X		Not connected

Table 12 JTAG Interface

4.16 PWM

PWMs are free programmable. On a non-powered board it´s not allowed to have a voltage on one of the PWM contacts. Also a higher voltage as the announced I/O power is not allowed.

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1J	E18	PWM_1	SPDIF_EXT_CLK	O	1V8	Standard PWM
J1J	F18	PWM_2	SPDIF_RX	O	1V8	Standard PWM
J1J	G18	PWM_3	SPDIF_TX	O	1V8	Standard PWM

4.17 Vendor defined contacts

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1J	B22	CLKOUT2	CLKOUT2	O	1V8	F&S defined extra Output
J1J	P16	NVCC_RGMII		PWR	1V8	connect with ETH Phy on carrier board, or power NVCC_RGMII via mounting option

CLKOUT2 is an extra clock output from the i.MX8M CPU, for more info lookup i.MX8M CPU datasheet

NVCC_RGMII is a PWR Input. NVCC_RGMII is generated from the external Ethernet PHY.

NVCC_RGMII can also be powered via mounting option on FS 8MX OSM-SF.

5 eMMC

The module supports eMMC v4.41 or higher from several manufacturers.

The eMMC Flash is based on multi-level cell (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6 RTC

There is an external RTC (PCF85263ATL) mounted on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

7 Power and Power Control Pins

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
J1L	Y8	VCC_IN_5V_Y8	N.C.	PWR	5V	Main Power supply input. Please refer chapter 8.2 DC Electrical Characteristics for more information
	Y9	VCC_IN_5V_Y9				
	Y10	VCC_IN_5V_Y10				
	Y11	VCC_IN_5V_Y11				
	Y17	VCC_IN_5V_Y17				
J1L	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, D18, E2, E15, E21, F16, F20, H2, H4, J16, J20, L2, L4, L18, M16, M20, P2, P4, P18, R1, R16, R20, U2, U4, V1, V16, V20, W3, Y2, Y18, AA1, AA4, AA7, AA8, AA10, AA11. AA14, AA17, AA19, AA22, AB3, AB6, AB9, AB15, AB21, AC4, AC7, AC10	GND_XX	N.C.	PWR	GND	Main Power supply Ground input
J1L	W17	RTC_PWR	N.C.	PWR	3V	RTC battery input; tie to 3.0V. Please refer chapter 8.2DC Electrical Characteristics
J1J	C6 C7 D6 D7 N2 R18 T17 T18 T19 Y13 Y14 AA2 AA13	RESERVED				Leave these pins floating (N.C.)
J1L	AA9	PWR_BTN#	ONOFF	I	1V8	Power-button from Carrier board. Carrier to float the line in in-

	Pin	Signal	CPU Pad	I/O	Voltage	Remarks
						active state. Active low, level sensitive
J1L	M17 M19 Y16 Y20 Y3 C5	VCC_X_Test				Module power voltage test point. Leave open (N.C.)
J1L	U17	SYS_RST#	N.C.	I	1V8	Reset input from carrier board. Carrier drives low to force a Module reset, floats the line otherwise
J1L	V17	CPU_POR_B	POR_B	O	1V8	Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN Signal, Optional via mounting option 1V8 fix
J1L	U18	VCC_OUT_IO	N.C.	O	1V8/3V3	Selectable voltage via jumper. Maximum current 100mA, leave open if not used
J1J	U19	BOOT_SEL#	BOOT_MODE0	I	1V8	If low on carrier board, OSM boots from carrier boot medium, onboard Pull-Up 10k
J1C	C20	SD_A_VCC	N.C.	O	3V3/1V8	SDIO A Voltage. It is used to provide the IO Voltage Level, max 100mA
J1J	C16	SD_B_VCC	N.C.	O	3V3/1V8	Selectable voltage

Table 13 Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test Laboratory. It's possible to use a supercapacitor instead.

VCC_OUT_IO is a 1V8 or 3V3 @100mA output. It´s generated from the internal PMIC and powered from VIN. Can be used as "Enable Signal" for the power regulators on baseboard. Please do not use VCC_OUT_IO as power supply for carrier board.

PWR_BTN# is the reset input for the module. PWR_BTN# only resets the CPU. In the event of a power failure, VCC_IN must be switched off and on to avoid latch-up effects.

The GND contacts which are given in the table above are the power ground contacts for VCC_IN. For a better EMC performance it is highly recommended to connect all GND Contacts to GND on the carrier board (not just the power ground contacts).

SD_A_VCC can be 3V3 and 1V8 via mounting option so it´s fixed voltage.

SD_B_VCC can be 3V3 and 1V8 via driver settings.

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Typ	Max	Unit
Input Voltage range 3.3V IOs	-0.3	3.3	3.6	V
Input Voltage range 1.8V IOs	-0.3	1.8	2.1	V
Voltage on any IO with VDD_VIN off			0.3	V
USB VBUS	-0.3	5	5.6	V
Maximum power consumption VDD_VBAT at 85°C			0.6	µA
Maximum output current VCC_IO			100	mA

Table 14: Absolute Maximum Ratings

8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
VCC_VIN	Module main power		2.7	5	5.5	V
RTC_PWR	RTC power		0.9	3	5.5	V
USB1/2_VBUS	USB supply voltage		4.4	5	5.5	V
OVDD	On module 3.3V from on module PMIC, delayed after VDD_VIN		3.15	3.3	3.45	V
VDD_1V8	1.8V output for power enable on carrier board		1.71	1.8	1.89	V
V_{ih}	High Level Input Voltage		0.7*OVDD		OVDD	V
V_{il}	Low Level Input Voltage		0		0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15			V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA			0.15	V
I_o	Output current IOs 1V8	1.8V			10	mA
I_o	Output current IOs 3V3	3.3V			5	mA
I_{VBAT}	Current consumption VBAT				0.22[*1]	µA

Table 15: DC Electrical Characteristics

[*1] Low current: typical 0.22 µA at VDD = 3.3 V and Tamb = 25 °C

9 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!

The following table shows nominal thermal specification of the module:

Operating Ranges	Min	Typ.	Max	Unit
Consumer Grade Operating Temperature	0		+70	°C
Industrial Grade Operating Temperature	-20		+85	°C
Extended Industrial Grade Operating Temperature	-40		+85	°C
Junction Temperature i.MX8M Mini & i.MX8M Nano (C-Temp)	0		+95	°C
Junction Temperature i.MX8M Mini & i.MX8M Nano (I-Temp)	-40		+105	°C
Junction to Package TOP (Ψ_{JT}) – i.MX8M Mini & Nano*[2]		0.2		°C/W

Table 16: Thermal Specification

Note 1: Maximum junction temperature of the CPU is 105°C.
In this case cooling is necessary and highly recommended.
See also: Power consumption and cooling

Please get in touch with our engineers for F&S recommended cooling solutions.

Note 2: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN12468 (https://www.nxp.com/docs/en/application-note/AN12468.pdf)

10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

11 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

13 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **8.5Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **2Watt** to **4Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 12: Matrix Code Sticker

18 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

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