Hardware Documentation

FS 8MM OSM-SF

for HW Revision 1.20

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Elektronik Systeme

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About This Document

This document describes how to use the FS 8MM OSM-SF (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com/en/osm.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/09.2021	All		All	Initial Version	GI
002/12.2021	All	M	9	Updated	GI
003/05.2024	All	A, M, R	All	New HW revision	SM
004/11.2024	All	M	5.2	Voltage ranges corrected	UK
005/04.2025	-	A, M, R	All	New design template, major adaptions	UK

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1 Overview

1.1 Additional Documentation

The “OSM Implementation Guide” contains information which are the same for all F&S OSM products, e.g. the

- mechanical description,
- general OSM contact grid signal description,
- handling information.

The latest version can be downloaded from www.fsembedded.com/en/osm.

1.2 General Parameter

Parameter	Description
Dimensions (L x W x H)	(30.0 x 30.0 x 2.0) mm
Weight	≈ 5 g
Pin Count	332 (224 used)

Table 1: General Parameter

1.3 Block Diagram

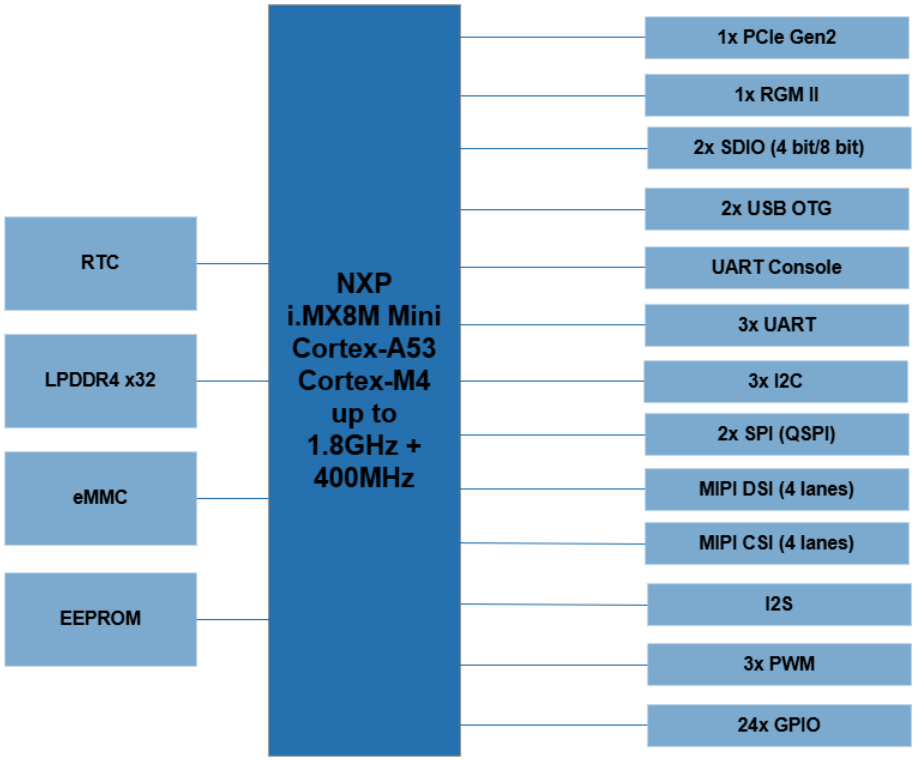

Figure 1: Block Diagram

Note: This diagram shows the maximum available features. The availability depends on the configuration.

1.4 Design Data

To ease the implementation, F&S provides the “OSM Carrier Board Design Library” which contains

- a schematic symbol (Altium & Cadence) including module-specific implementation information,
- the footprint (Altium & Cadence, baseboard side),
- a 3D model.

The latest version can be downloaded from www.fsembedded.com/en/osm.

2 Detailed Description

To increase clarity, the GND[1] pins and all pins which are not connected on the module are not listed in the following sections.

[1] All GND pins are connected on the module. F&S highly recommends to connect all of them on the carrier.

2.1 Power and Management

2.1.1 Power Supply

The following table shows the intended use of the power (PWR) pins on the module.

Contact #	Contact Name	I/O	Voltage	Comments
M19	VCC_2_TEST	PO	1.8 V	1.8 V intended for testing purposes max. current: 50 mA
Y20	VCC_4_TEST	PO	3.3 V	3.3 V intended to supply carrier peripherals max. current: 200 mA
Y8, Y9, Y10, Y11, Y17,	VCC_IN_5V	P	5.0 V	main power supply input
U18	VCC_OUT_IO	PO	1.8 V	general I/O reference voltage max. current: 100 mA
M17	ETH_IOPWR	PO	1.8 V	Ethernet I/O reference voltage max. current: 100 mA
C20	SDIO_A_IOPWR	PO	1.8 V 3.3 V	SDIO_A I/O reference voltage (switchable) max. current: 100 mA
T20	SDIO_B_IOPWR	PO	1.8 V	SDIO_B I/O reference voltage max. current: 100 mA
W17	RTC_PWR	P	3.0 V	RTC supply input[1]

Table 2: PWR (pin description)

[1] RTC_PWR may be sourced from a Carrier based Li-cell or Super Cap.

2.1.2 System Control

The following picture visualizes the system control (CTRL) topology of the module.

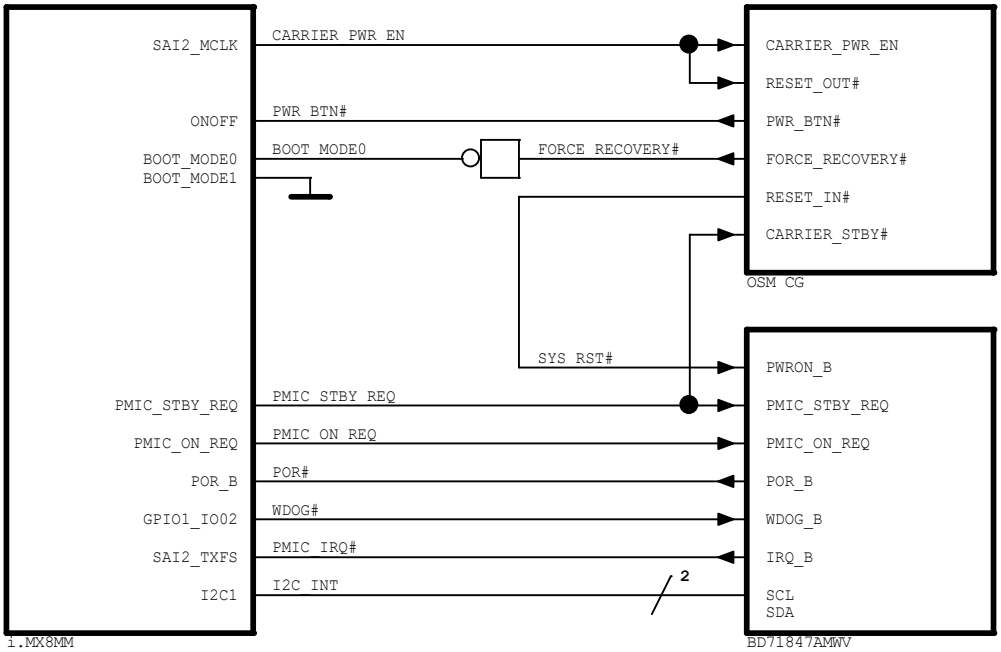

Figure 2: System Control (topology)

The following table shows the intended use of the CTRL pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V17	CARRIER_PWR_EN	SAI2_MCLK	O	1.8 V	HIGH active, intended to enable the power for peripherals on carrier
Y13	CARRIER_STBY#	PMIC_STBY_REQ	O	1.8 V	HIGH[2] active, indicates that module is in standby power state
U17	RESET_IN#	**BD71847AMWV:** PWRON_B	I	5.0 V[3]	PU 100k[3], logic LOW resets the module
Y14	RESET_OUT#	SAI2_MCLK	O	1.8 V	connected to CARRIER_PWR_EN
AA9	PWR_BTN#[1]	ONOFF	I	1.8 V	PU 10k, behavior depends on the configuration
T17	FORCE_RECOVERY#	BOOT_MODE0	I	1.8 V	PU 10k HIGH/FLOAT: module boots from internal fuses LOW: module is in USB Serial Download mode

Table 3: System Control (pin description)

[1] PWR_BTN# is debounced inside of the CPU.

[2] **Please note:** Inverted logic with respect to the definition in the OSM standard.

[3] **Please note:** OSM STD V.1.2 demands: PU 10k & 1.8 V I/O level & "*Carrier drives low to force a Module reset, floats the line otherwise*".

2.2 Interfaces

2.2.1 MISC

None of the "RESERVED", "Vendor Defined" & "COM_AREA" pins are connected on the module.

2.2.2 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
N17	JTAG_TCK(SWCLK)	JTAG_TCK	I	1.8 V	
N19	JTAG_TMS(SWDIO)	JTAG_TMS	I	1.8 V	
P17	JTAG_TDI	JTAG_TDI	I	1.8 V	
R17	JTAG_TDO(SWO)	JTAG_TDO	O	1.8 V	
R19	JTAG_nTRST	JTAG_TRST_B	I	1.8 V	PU 10k

Table 4: JTAG (pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A53 and Cortex®-M4 cores via serial console. See chapter UART.

2.2.3 UART

The module provides four Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
A14	UART_A_RX	UART2_RXD	I	1.8 V	
B13	UART_A_TX	UART2_TXD	O	1.8 V	
C13	UART_A_RTS	SAI3_RXC	O	1.8 V	
C14	UART_A_CTS	SAI3_RXD	I	1.8 V	
D14	UART_B_RX	UART3_RXD	I	1.8 V	
D13	UART_B_TX	UART3_TXD	O	1.8 V	
D15	UART_B_RTS	ECSPI1_MISO	O	1.8 V	
D16	UART_B_CTS	ECSPI1_SS0	I	1.8 V	
A22	UART_C_RX	UART4_RXD	I	1.8 V	Cortex®-M4 debug
B23	UART_C_TX	UART4_TXD	O	1.8 V	Cortex®-M4 debug

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
D22	UART_CON_RX	UART1_RXD	I	1.8 V	Cortex®-A53 debug
D23	UART_CON_TX	UART1_TXD	O	1.8 V	Cortex®-A53 debug

Table 5: UART (pin description)

2.2.4 Ethernet

The module provides one Reduced Gigabit Media-Independent Interface (RGMII) Ethernet (ETH) port. The following table shows the use of the ETH related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
H15	ETH_A_RGMII_TXD0	ENET_TD0	O	1.8 V	
G15	ETH_A_RGMII_TXD1	ENET_TD1	O	1.8 V	
H16	ETH_A_RGMII_TXD2	ENET_TD2	O	1.8 V	
G16	ETH_A_RGMII_TXD3	ENET_TD3	O	1.8 V	
K16	ETH_A_RGMII_TX_EN(_ER)	ENET_TX_CTL	O	1.8 V	
J15	ETH_A_RGMII_TX_CLK	ENET_TXC	O	1.8 V	
K15	ETH_A_RGMII_RXD0	ENET_RD0	I	1.8 V	
L15	ETH_A_RGMII_RXD1	ENET_RD1	I	1.8 V	
N15	ETH_A_RGMII_RXD2	ENET_RD2	I	1.8 V	
P15	ETH_A_RGMII_RXD3	ENET_RD3	I	1.8 V	
M15	ETH_A_RGMII_RX_DV(_ER)	ENET_RX_CTL	I	1.8 V	
R15	ETH_A_RGMII_RX_CLK	ENET_RXC	I	1.8 V	
T15	ETH_A_MDIO	ENET_MDIO	I/O	1.8 V	
T16	ETH_A_MDC	ENET_MDC	O	1.8 V	

Table 6: ETH (pin description)

2.2.5 GPIO

Besides the PWM signals, the module provides up to 24 additional, free programmable General Purpose Input/Output (GPIO) signals[1,2]. The following table shows the use of the GPIO related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
D17	GPIO_A_0	GPIO1_IO00	I/O	1.8 V	
E17	GPIO_A_1	GPIO1_IO01	I/O	1.8 V	
F17	GPIO_A_2	GPIO1_IO04	I/O	1.8 V	
G17	GPIO_A_3	GPIO1_IO05	I/O	1.8 V	
H17	GPIO_A_4	GPIO1_IO06	I/O	1.8 V	
J17	GPIO_A_5	GPIO1_IO07	I/O	1.8 V	
K17	GPIO_A_6	NAND_CE1_B	I/O	1.8 V	dual function: SPI_A_CS1#
L17	GPIO_A_7	ECSPI1_SCLK	I/O	1.8 V	dual function: SPI_B_CS1#
D19	GPIO_B_0	GPIO1_IO08	I/O	1.8 V	
E19	GPIO_B_1	GPIO1_IO09	I/O	1.8 V	
F19	GPIO_B_2	GPIO1_IO10	I/O	1.8 V	
G19	GPIO_B_3	GPIO1_IO11	I/O	1.8 V	
H19	GPIO_B_4	ECSPI1_MOSI	I/O	1.8 V	
J19	GPIO_B_5	SAI1_RDX7	I/O	1.8 V	
K19	GPIO_B_6	SAI1_RDX6	I/O	1.8 V	
L19	GPIO_B_7	SAI1_RDX5	I/O	1.8 V	
D3	GPIO_C_0	SAI1_RDX4	I/O	1.8 V	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
D4	GPIO_C_1	SAI1_RDX3	I/O	1.8 V	
E3	GPIO_C_2	SAI1_RDX2	I/O	1.8 V	
E4	GPIO_C_3	SAI1_RDX1	I/O	1.8 V	
F3	GPIO_C_4	SAI3_TXD	I/O	1.8 V	dual function: DISP_VDD_EN
F4	GPIO_C_5	SAI3_TXC	I/O	1.8 V	dual function: DISP_BL_EN
G3	GPIO_C_6	SAI2_TXC	I/O	1.8 V	dual function: CAM_A_PWR
G4	GPIO_C_7	SAI2_TXD0	I/O	1.8 V	dual function: CAM_A_RST#

Table 7: GPIO (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts, it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

2.2.6 SDIO

The module provides two Secure Digital Input Output (SDIO) interfaces. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E20	SDIO_A_CMD	SD2_CMD	I/O	1.8 V[1] 3.3 V[1]	
F21	SDIO_A_CLK	SD2_CLK	O	1.8 V[1] 3.3 V[1]	
G20	SDIO_A_D0	SD2_DATA0	I/O	1.8 V[1] 3.3 V[1]	
G21	SDIO_A_D1	SD2_DATA1	I/O	1.8 V[1] 3.3 V[1]	
H20	SDIO_A_D2	SD2_DATA2	I/O	1.8 V[1] 3.3 V[1]	
H21	SDIO_A_D3	SD2_DATA3	I/O	1.8 V[1] 3.3 V[1]	
J21	SDIO_A_CD#	SD2_CD_B	I	1.8 V[1] 3.3 V[1]	PU 10k
D20	SDIO_A_WP	SD2_WP	I	1.8 V[1] 3.3 V[1]	PU 10k
D21	SDIO_A_PWR_EN	SD2_RESET_B	O	1.8 V[1] 3.3 V[1]	
K21	SDIO_B_CMD	NAND_WP_B	I/O	1.8 V	
K20	SDIO_B_CLK	NAND_WE_B	O	1.8 V	
L20	SDIO_B_D0	NAND_DATA04	I/O	1.8 V	
L21	SDIO_B_D1	NAND_DATA05	I/O	1.8 V	
M21	SDIO_B_D2	NAND_DATA06	I/O	1.8 V	
N20	SDIO_B_D3	NAND_DATA07	I/O	1.8 V	
N21	SDIO_B_D4	NAND_RE_B	I/O	1.8 V	
P20	SDIO_B_D5	NAND_CE2_B	I/O	1.8 V	
P21	SDIO_B_D6	NAND_CE3_B	I/O	1.8 V	
R21	SDIO_B_D7	NAND_CLE	I/O	1.8 V	
T21	SDIO_B_CD#	SAI2_RXC	I	1.8 V	PU 10k
U20	SDIO_B_WP	SAI2_RXD0	I	1.8 V	PU 10k

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
U21	SDIO_B_PWR_EN	NAND_READY_B	O	1.8 V	

Table 8: SDIO (pin description)

[1] As SDIO_A is intended to be used with SD/MMC cards, the I/O voltage is dynamically switchable between 3.3 V & 1.8 V on the module. The level of SDIO_A_IOPWR depends on the internal signal SDIO_A_VSEL (CPU pad: GPIO1_IO03):

- SDIO_A_VSEL = LOW: SDIO_A_IOPWR = 3.3 V (default)
- SDIO_A_VSEL = HIGH: SDIO_A_IOPWR = 1.8 V

2.2.7 PWM

The module provides up to four free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E18	PWM_0	SAI3_MCLK	O	1.8 V	dual function: DISP_BL_PWM
F18	PWM_1	SPDIF_EXT_CLK	O	1.8 V	
G18	PWM_2	SPDIF_RX	O	1.8 V	
H18	PWM_3	SPDIF_TX	O	1.8 V	

Table 9: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

2.2.8 Analog Signals

No Analog to Digital Converter (ADC) is implemented on the module.

2.2.9 SPI

The module provides two Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V15	SPI_A_SDO_(IO0)[1]	NAND_DATA00	I/O	1.8 V	
U15	SPI_A_SDI_(IO1)[1]	NAND_DATA01	I/O	1.8 V	
W16	SPI_A_WP_(IO2)[1]	NAND_DATA02	I/O	1.8 V	
W15	SPI_A_HOLD_(IO3)[1]	NAND_DATA03	I/O	1.8 V	
Y15	SPI_A_CS0#	NAND_CE0_B	O	1.8 V	
K17	SPI_A_CS1#	NAND_CE1_B	O	1.8 V	dual function: GPIO_A_6
U16	SPI_A_SCK	NAND_ALE	O	1.8 V	
Y22	SPI_B_SDI	ECSPI2_MISO	I	1.8 V	
Y23	SPI_B_SDO	ECSPI2_MOSI	O	1.8 V	
AA23	SPI_B_CS0#	ECSPI2_SS0	O	1.8 V	
L17	SPI_B_CS1#	ECSPI1_SCLK	O	1.8 V	dual function: GPIO_A_7
Y21	SPI_B_SCK	ECSPI2_SCLK	O	1.8 V	

Table 10: SPI (pin description)

[1] F&S describes SPI_A as QuadSPI by default.

2.2.10 I2S

The module provides one Inter-IC Sound (I2S) interface. The following table shows the use of the I2S related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V21	I2S_A_DATA_IN	SAI5_RXD0	I	1.8 V	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
W21	I2S_A_DATA_OUT	SAI5_RXD3	O	1.8 V	
W18	I2S_A_LRCLK[1]	SAI5_RXD1	I/O	1.8 V	
W20	I2S_A_BITCLK[1]	SAI5_RXD2	I/O	1.8 V	
V18	I2S_MCLK	SAI5_MCLK	O	1.8 V	

Table 11: I2S (pin description)

[1] Output, if module acts in Master Mode. Input, if module acts in Slave Mode.

2.2.11 CAN

No Controller Area Network Interface (CAN) is implemented on the module

2.2.12 USB

The module provides two Universal Serial Busses (USB)[1], including controllers and PHYs. The following table shows the use of the USB related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB13	USB_A_D_N	USB1_DN	I/O	USB	
AC14	USB_A_D_P	USB1_DP	I/O	USB	
AB14	USB_A_ID	USB1_ID	I	1.8 V	PU 10k
AC15	USB_A_OC#	GOIO1_IO13	I	1.8 V	PU 10k
AB16	USB_A_VBUS	USB1_VBUS	I	5.0 V	USB VBUS detection on the PHY port A[2]
AC16	USB_A_EN	GOIO1_IO12	O	1.8 V	
AB23	USB_B_D_N	USB2_DN	I/O	USB	
AC22	USB_B_D_P	USB2_DP	I/O	USB	
AB22	USB_B_ID	USB2_ID	I	1.8 V	PU 10k
AC21	USB_B_OC#	GOIO1_IO15	I	1.8 V	PU 10k
AB20	USB_B_VBUS	USB2_VBUS	I	5.0 V	USB VBUS detection on the PHY port B[2]
AC20	USB_B_EN	GOIO1_IO14	O	1.8 V	

Table 12: USB (pin description)

[1] USB_A: USB 2.0 OTG & USB_B: USB 2.0 OTG.

[2] Must always be connected to the respective USB VBUS rail.

2.2.13 I2C

The module provides four Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
INT[1]	RTC	0x51	Real Time Clock on the module
	PMIC	0x48	Power Management IC on the module
A	EEPROM	0x50	EEPROM on the module (accessible from carrier)
	I2C_A		general I2C on carrier
B	I2C_B		general I2C on carrier
C	CAM_A_I2C[2]		I2C, related to camera on carrier
	PCIe_SM_I2C[2]		I2C, related to PCIe on carrier

Table 13: I2C (usage)

[1] I2C_INT is for internal use only.

[2] PCIe_SM_I2C & CAM_A_I2C are firmly connected on the module.

The following table shows the use of the I2C related pins on the module[1].

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AA15	I2C_A_SCL	I2C2_SCL	I/O	1.8 V	PU 2k2
AA16	I2C_A_SDA	I2C2_SDA	I/O	1.8 V	PU 2k2
AA20	I2C_B_SCL	I2C3_SCL	I/O	1.8 V	PU 2k2
AA21	I2C_B_SDA	I2C3_SDA	I/O	1.8 V	PU 2k2

Table 14: I2C (pin description)

[1] PCIe_SM_I2C & CAM_A_I2C are described in their respective section.

2.2.14 PCIe

The module provides one Peripheral Component Interconnect (PCI) Express interface, including controller and PHY. The following table shows the use of the PCIe related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB1	PCIe_A_HSI0_P[1]	PCIE_RXN_P	I	PCIe	
AB2	PCIe_A_HSI0_N[1]	PCIE_RXN_N	I	PCIe	
AC2	PCIe_A_HSO0_P[1]	PCIE_TXN_P	O	PCIe	
AC3	PCIe_A_HSO0_N[1]	PCIE_TXN_N	O	PCIe	
W2	PCIe_CLKREQ#	SAI3_RXFS	I	1.8 V	PU 10k
V2	PCIe_A_PERST#	SAI5_RXFS	O	1.8 V	
W1	PCIe_REFCLK_P	PCIE_CLK_P	O	PCIe	
Y1	PCIe_REFCLK_N	PCIE_CLK_N	O	PCIe	
T2	PCIe_WAKE#	SAI5_RXC	I	1.8 V	PU 10k
U1	PCIe_SMDAT	I2C4_SDA	I/O	1.8 V	PU 2k2, dual function: CAM_A_SDA
T1	PCIe_SMCLK	I2C4_SCL	O	1.8 V	PU 2k2, dual function: CAM_A_SCL
R2	PCIe_SM_ALERT#	SAI3_TXFS	I	1.8 V	PU 2k2

Table 15: PCIe (pin description)

[1] AC coupled on carrier.

2.2.15 MIPI CSI

The module provides one 4 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI):

- complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2.

The following table shows the use of the MIPI CSI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C1	CSI_A_DATA0_N	MIPI_CSI_D0_N	I	MIPI CSI	
B1	CSI_A_DATA0_P	MIPI_CSI_D0_P	I	MIPI CSI	
A2	CSI_A_DATA1_N	MIPI_CSI_D1_N	I	MIPI CSI	
A3	CSI_A_DATA1_P	MIPI_CSI_D1_P	I	MIPI CSI	
A5	CSI_A_DATA2_N	MIPI_CSI_D2_N	I	MIPI CSI	
A6	CSI_A_DATA2_P	MIPI_CSI_D2_P	I	MIPI CSI	
B6	CSI_A_DATA3_N	MIPI_CSI_D3_N	I	MIPI CSI	
B7	CSI_A_DATA3_P	MIPI_CSI_D3_P	I	MIPI CSI	
B3	CSI_A_CLOCK_N	MIPI_CSI_CLK_N	I	MIPI CSI	
B4	CSI_A_CLOCK_P	MIPI_CSI_CLK_P	I	MIPI CSI	
C2	CAM_MCK	CLOCKOUT1	O	1.8 V	
C3	CAM_A_SDA	I2C4_SDA	I/O	1.8 V	PU 2k2, dual function: PCIe_SMDAT
C4	CAM_A_SCL	I2C4_SCL	O	1.8 V	PU 2k2, dual function: PCIe_SMCLK

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
G3	CAM_A_PWR	SAI2_TXC	O	1.8 V	dual function: GPIO_C_6
G4	CAM_A_RST#	SAI2_TXD0	O	1.8 V	dual function: GPIO_C_7

Table 16: CSI (pin description)

2.2.16 MIPI DSI

The module provides one 4 lane Display Serial Interface (DSI), defined by the Mobile Industry Processor Interface Alliance (MIPI):

- complaint with MIPI DSI specification v1.01r11 and MIPI D-PHY specification v1.2.

The following table shows the use of the MIPI DSI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB11	DSI_DATA0_N	MIPI DSI_D0_N	O	MIPI DSI	
AB10	DSI_DATA0_P	MIPI DSI_D0_P	O	MIPI DSI	
AC9	DSI_DATA1_N	MIPI DSI_D1_N	O	MIPI DSI	
AC8	DSI_DATA1_P	MIPI DSI_D1_P	O	MIPI DSI	
AC6	DSI_DATA2_N	MIPI DSI_D2_N	O	MIPI DSI	
AC5	DSI_DATA2_P	MIPI DSI_D2_P	O	MIPI DSI	
AB5	DSI_DATA3_N	MIPI DSI_D3_N	O	MIPI DSI	
AB4	DSI_DATA3_P	MIPI DSI_D3_P	O	MIPI DSI	
AB8	DSI_CLOCK_N	MIPI DSI_CLK_N	O	MIPI DSI	
AB7	DSI_CLOCK_P	MIPI DSI_CLK_P	O	MIPI DSI	
AA3	DSI_TE	SAI2_RXFS	O	1.8 V	DSI panel tearing effect signal
F3	DISP_VDD_EN	SAI3_TXD	O	1.8 V	dual function: GPIO_C_4
F4	DISP_BL_EN	SAI3_TXC	O	1.8 V	dual function: GPIO_C_5
E18	DISP_BL_PWM	SAI3_MCLK	O	1.8 V	dual function: PWM_0

Table 17: DSI (pin description)

2.3 Internal Peripherals on the Module

2.3.1 LPDDR4

The module contains one 32-bit LPDDR4 SDRAM which operates with up to 3000 MT/s.

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to the internal I2C bus (I2C_INT, address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

2.3.4 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50).

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
V_{5V}	main power input voltage at the V_5V_IN pins	-0.30	6.00	V
V_{RTC}	RTC battery input voltage at the RTC_PWR pin	-0.50	6.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.30	V_{DD} + 0.30	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.50	V

Table 18: Absolute Maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{5V}	main power input[1]		4.50	5.00	5.50	V
I_{5V}					2.5	A
V_{RTC}	RTC battery input	contact: **W17** V_{RTC} = 3.0 V	1.20	3.00	5.50	V
I_{RTC}				350	480	nA
USB VBUS	PHY detection of USB VBUS	contact: **AB16, C9**		5.00		V
$V_{VCC\_2\_TEST}$	supply output (for testing purposes)	contact: **M19**		1.80		V
$I_{VCC\_2\_TEST}$					50	mA
$V_{VCC\_4\_TEST}$	supply output (for carrier peripherals)	contact: **Y20**		3.30		V
$I_{VCC\_4\_TEST}$					200	mA
$V_{VCC\_OUT\_IO}$	supply output (general I/O reference)	contact: **U18**		1.80		V
$I_{VCC\_OUT\_IO}$					100	mA
V_{ETH_IOPWR}	supply output (Ethernet I/O reference)	contact: **M17**		1.80		V
I_{ETH_IOPWR}					100	mA
$V_{SDIO\_A\_IOPWR}$	supply output (SDIO_A I/O reference)	contact: **C20**		1.80	3.30	V
$I_{SDIO\_A\_IOPWR}$					100	mA
$V_{SDIO\_B\_IOPWR}$	supply output (SDIO_B I/O reference)	contact: **T20**		1.80		V
$I_{SDIO\_B\_IOPWR}$					100	mA
V_{IH}	I/O high-level input voltage	V_{DD} = 1.8 V / 3.3 V	0.7 · V_{DD}	V_{DD}	V_{DD} + 0.2	V
V_{IL}	I/O low-level I/O input voltage		-0.20		0.3 · V_{DD}	V
V_{OH}	I/O high-level output voltage		0.8 · V_{DD}		V_{DD}	V
V_{OL}	I/O low-level I/O output voltage		0		0.2 · V_{DD}	V
I_{GPIO_OUT}	I/O drive strength (general)				12	mA
$T_{OPERATE}$	operating temperature range[2]	C TEMP grade	0		70	°C
		I TEMP grade	-25		85	°C
		XI TEMP grade	-40		85	°C
$T_{STORAGE}$	storage temperature range		-40		85	°C
$t_{STORAGE}$	storage time	no environmental control		6	months	
		T_{AMB} = 25 °C ± 5 °C humidity max. 60 %		12	months	

Table 19: Recommended Operating Conditions

[1] The OSM standard requires 5.0 V ± 5 %, but the module is tested and validated within the specified range.

[2] An external cooling solution may be required to cover the entire range.

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

Please see the following webpage: www.fsembedded.com/en/support/certifications/

5.3 Important Notice

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