# Hardware Documentation

*FS 8MM OSM™-SF*
*for HW Revision 1.10*

Preliminary

Version 004
(2024-11-14)

Elektronik Systeme


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# About This Document

This document describes how to use the FS 8MM OSM™-SF (later only module) board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

# ESD Requirements

All F&S hardware products are electrostatic sensitive devices. All products are handled and packaged according to electrostatic discharge (ESD) guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

# History

| Date | V | Platform | A,M,R | Chapter | Description | Au |
|---|---|---|---|---|---|---|
| 08.09.2021 | 001 | All | - | | Initial Version | GI |
| 07.12.2021 | 002 | All | M | 9 | Updated | GI |
| 06.05.2024 | 003 | All | A,M,R | All | New HW revision | SM |
| 14.11.2024 | 004 | All | M | 5.2 | Voltage ranges corrected | UK |
| | | | | | | |

| | |
|---|---|
| V | Version |
| A,M,R | Added, Modified, Removed |
| Au | Author |

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# 1 General

## 1.1 Block Diagram

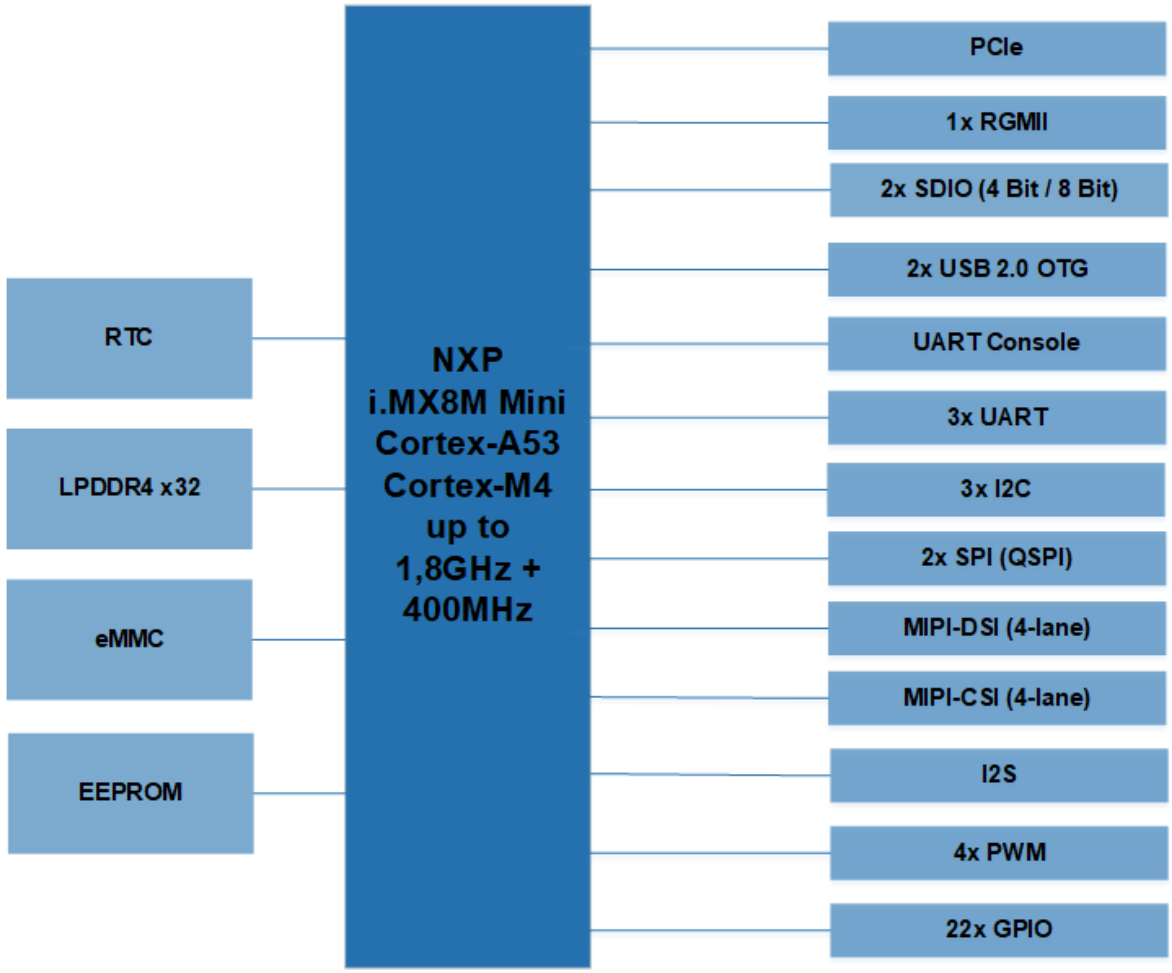


*Figure 1: Block diagram*

## 1.2 Dimensions

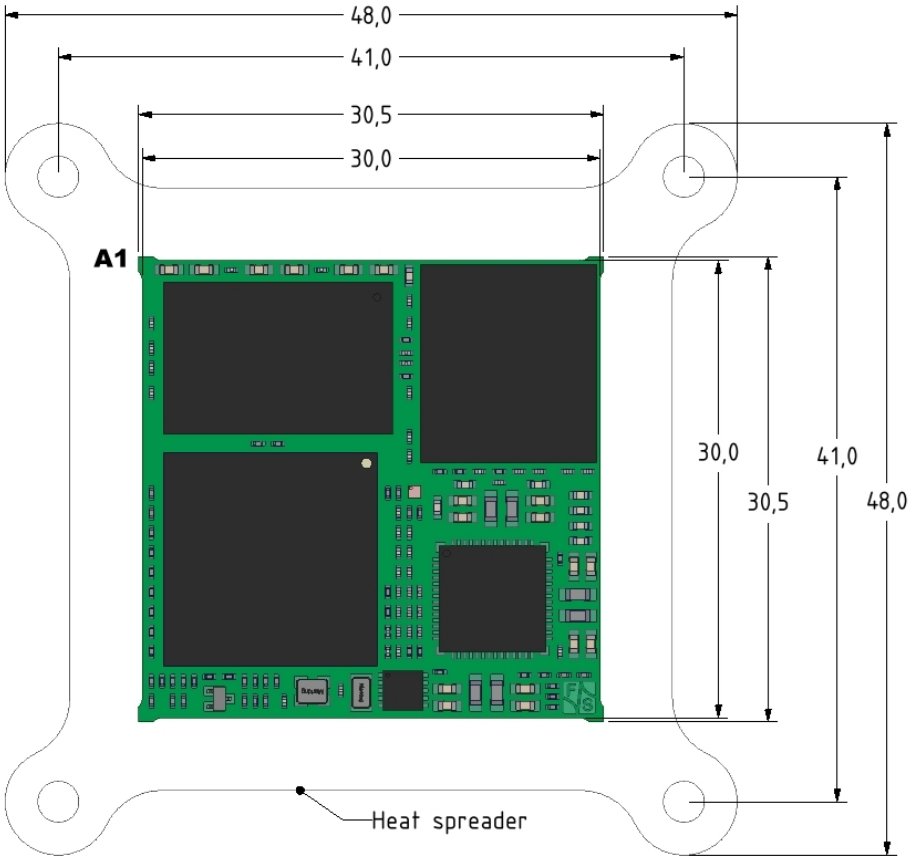


Figure 2: OSM8MM top view with heat spreader, all dimensions in mm

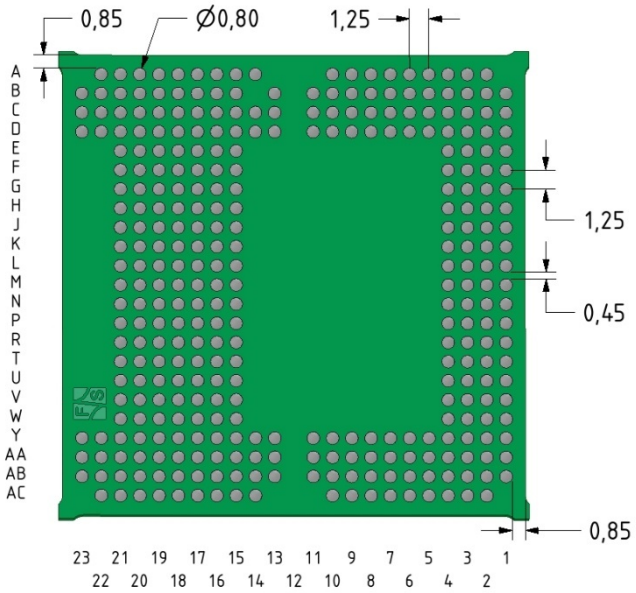


Figure 3: OSM8MM bottom view with pin numbers, all dimensions in mm

## 1.3 General Information

| Dimensions | Description |
|---|---|
| **General tolerance** | ± 0.10 mm |
| **PCB Thickness** | 1.20 mm ± 0.12 mm |
| **Part height on top side** | 1.50 mm |
| **Part height on bottom side** | No Parts on bottom side |
| **Weight** | Approx. 12.00 g |
| **Pin count** | 332 (connected: 221) |

*Table 1: General information*

**Note:** 3D Step model, footprint and schematic symbol can be downloaded from www.fs-net.de

## 1.4 Contact Characteristics

Referred to the OSM HW Specification V1.1 this module has a standard height and can be soldered directly on the carrier board. A cutout area or spacer is not needed. The module is using LGA (Land grid array) as default contact type. FTGA (Fused tin grid array) is optionally available.

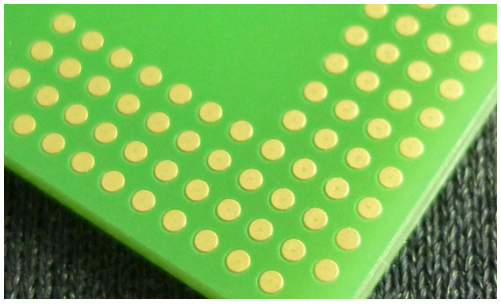

Figure 4: LGA

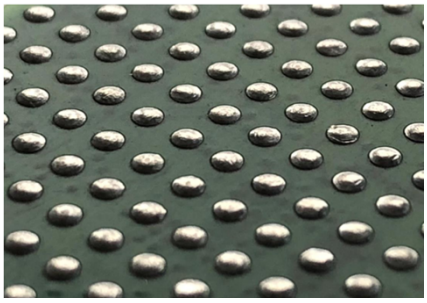

Figure 5: FTGA

## 1.5 Cooling

As a base for the cooling concept, F&S offers a heat spreader for OSM™ Size S modules. They can be ordered via F&S web shop, Part No.: **MHS.OSM.1**. For more information see documentation on the F&S website.

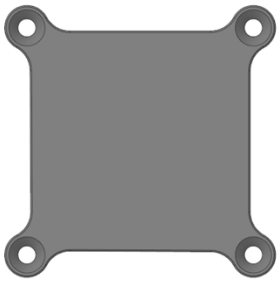

Figure 6: Heat spreader

## 1.6 Contact Grid Signal Description

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| A2 | CSI_DATA1_N | MIPI_CSI_D1_N | I | | |
| A3 | CSI_DATA1_P | MIPI_CSI_D1_P | I | | |
| A4 | GND | | PWR | GND | |
| A5 | CSI_DATA2_N | MIPI_CSI_D2_N | I | | |
| A6 | CSI_DATA2_P | MIPI_CSI_D2_P | I | | |
| A7 | GND | | PWR | GND | |
| A10 | GND | | PWR | GND | |
| A14 | UART_A_RX | UART2_RXD | I | 1.8V | |
| A22 | UART_C_RX | UART4_RXD | I | 1.8V | |
| B1 | CSI_DATA0_P | MIPI_CSI_D0_P | I | | |
| B2 | GND | | PWR | GND | |
| B3 | CSI_CLOCK_N | MIPI_CSI_CLK_N | I | | |
| B4 | CSI_CLOCK_P | MIPI_CSI_CLK_P | I | | |
| B5 | GND | | PWR | GND | |
| B6 | CSI_DATA3_N | MIPI_CSI_D3_N | I | | |
| B7 | CSI_DATA3_P | MIPI_CSI_D3_P | I | | |
| B8 | GND | | PWR | GND | |
| B9 | GND | | PWR | GND | |
| B13 | UART_A_TX | UART2_TXD | O | 1.8V | |
| B23 | UART_C_TX | UART4_TXD | O | 1.8V | |
| C1 | CSI_DATA0_N | MIPI_CSI_D0_N | I | | |
| C2 | CAM_MCK | CLKOUT1 | O | | |
| C3 | I2C_CAM_SDA/CSI_TX_N | I2C4_SDA | I/O | 1.8V | PU: 2k2 |
| C4 | I2C_CAM_SCL/CSI_TX_P | I2C4_SCL | O | 1.8V | PU: 2k2 |
| C20 | SDIO_A_IOPWR | | PWR | 1.8V/3.3V | |
| C11 | GND | | PWR | GND | |
| C13 | UART_A_RTS | SAI3_RXC | O | 1.8V | |
| C14 | UART_A_CTS | SAI3_RXD | I | 1.8V | |
| D1 | GND | | PWR | GND | |
| D3 | GPIO_C_0 | SAI1_RXD4 | I/O | 1.8V | |
| D4 | GPIO_C_1 | SAI1_RXD3 | I/O | 1.8V | |
| D5 | GND | | PWR | GND | |
| D8 | GND | | PWR | GND | |
| D13 | UART_B_TX | UART3_TXD | O | 1.8V | |
| D14 | UART_B_RX | UART3_RXD | I | 1.8V | |
| D15 | UART_B_RTS | ECSPI1_MISO | O | 1.8V | |
| D16 | UART_B_CTS | ECSPI1_SS0 | I | 1.8V | |
| D17 | GPIO_A_0 | GPIO1_IO00 | I/O | 1.8V | |
| D18 | GND | | PWR | GND | |
| D19 | GPIO_B_0 | GPIO1_IO08 | I/O | 1.8V | |
| D20 | SDIO_A_WP | SD2_WP | I | 1.8V/3.3V | PU: 10k |
| D21 | SDIO_A_PWR_EN | SD2_RESET_B | O | 1.8V/3.3V | |
| D22 | UART_CON_RX | UART1_RXD | I | 1.8V | |

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| D23 | UART_CON_TX | UART1_TXD | O | 1.8V | |
| E2 | GND | | PWR | GND | |
| E3 | GPIO_C_2 | SAI1_RXD2 | I/O | 1.8V | |
| E4 | GPIO_C_3 | SAI1_RXD1 | I/O | 1.8V | |
| E15 | GND | | PWR | GND | |
| E17 | GPIO_A_1 | GPIO1_IO01 | I/O | 1.8V | |
| E18 | PWM_0/DISP_BL_PWM | SAI3_MCLK | O | 1.8V | |
| E19 | GPIO_B_1 | GPIO1_IO09 | I/O | 1.8V | |
| E20 | SDIO_A_CMD | SD2_CMD | I/O | 1.8V/3.3V | |
| E21 | GND | | PWR | GND | |
| F3 | GPIO_C_4/DISP_VDD_EN | SAI3_TXD | I/O | 1.8V | |
| F4 | GPIO_C_5/DISP_BL_PWM | SAI3_TXC | I/O | 1.8V | |
| F16 | GND | | PWR | GND | |
| F17 | GPIO_A_2 | GPIO1_IO04 | I/O | 1.8V | |
| F18 | PWM_1 | SPDIF_EXT_CLK | O | 1.8V | |
| F19 | GPIO_B_2 | GPIO1_IO10 | I/O | 1.8V | |
| F20 | GND | | PWR | GND | |
| F21 | SDIO_A_CLK | SD2_CLK | O | 1.8V/3.3V | |
| G3 | CAM_PWR/GPIO_C_6 | SAI2_TXC | I/O | 1.8V | |
| G4 | CAM_RST#/GPIO_C_7 | SAI2_TXD0 | I/O | 1.8V | |
| G15 | ETH_A_(S)(R)(G)MII_TXD1 | ENET_TD1 | O | 1.8V | |
| G16 | ETH_A_(S)(R)(G)MII_TXD3 | ENET_TD3 | O | 1.8V | |
| G17 | GPIO_A_3 | GPIO1_IO05 | I/O | 1.8V | |
| G18 | PWM_2 | SPDIF_RX | O | 1.8V | |
| G19 | GPIO_B_3 | GPIO1_IO11 | I/O | 1.8V | |
| G20 | SDIO_A_D0 | SD2_DATA0 | I/O | 1.8V/3.3V | |
| G21 | SDIO_A_D1 | SD2_DATA1 | I/O | 1.8V/3.3V | |
| H2 | GND | | PWR | GND | |
| H4 | GND | | PWR | GND | |
| H15 | ETH_A_(S)(R)(G)MII_TXD0 | ENET_TD0 | O | 1.8V | |
| H16 | ETH_A_(S)(R)(G)MII_TXD2 | ENET_TD2 | O | 1.8V | |
| H17 | GPIO_A_4 | GPIO1_IO06 | I/O | 1.8V | |
| H18 | PWM_3 | SPDIF_TX | O | 1.8V | |
| H19 | GPIO_B_4 | ECSPI1_MOSI | I/O | 1.8V | |
| H20 | SDIO_A_D2 | SD2_DATA2 | I/O | 1.8V/3.3V | |
| H21 | SDIO_A_D3 | SD2_DATA3 | I/O | 1.8V/3.3V | |
| J15 | ETH_A_(R)(G)MII_TX_CLK | ENET_TXC | I/O | 1.8V | |
| J16 | GND | | PWR | GND | |
| J17 | GPIO_A_5 | GPIO1_IO07 | I/O | 1.8V | |
| J19 | GPIO_B_5 | SAI1_RXD7 | I/O | 1.8V | |
| J20 | GND | | PWR | GND | |
| J21 | SDIO_A_CD# | SD2_CD_B | I | 1.8V/3.3V | PU: 10k |
| K15 | ETH_A_(S)(R)(G)MII_RXD0 | ENET_RD0 | I | 1.8V | |
| K16 | ETH_A_(R)(G)MII_TX_EN(_ER) | ENET_TX_CTL | I | 1.8V | |
| K17 | GPIO_A_6/SPI_A_CS1# | NAND_CE1_B | I/O | 1.8V | |

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| K19 | GPIO_B_6 | SAI1_RXD6 | I/O | 1.8V | |
| K20 | SDIO_B_CLK | NAND_WE_B | O | 1.8V | |
| K21 | SDIO_B_CMD | NAND_WP_B | I/O | 1.8V | |
| L2 | GND | | PWR | GND | |
| L4 | GND | | PWR | GND | |
| L15 | ETH_A_(S)(R)(G)MII_RXD1 | ENET_RD1 | I | 1.8V | |
| L17 | GPIO_A_7/SPI_B_CS1# | ECSPI1_SCLK | I/O | 1.8V | |
| L18 | GND | | PWR | GND | |
| L19 | GPIO_B_7 | SAI1_RXD5 | I/O | 1.8V | |
| L20 | SDIO_B_D0 | NAND_DATA04 | I/O | 1.8V | |
| L21 | SDIO_B_D1 | NAND_DATA05 | I/O | 1.8V | |
| M15 | ETH_A_(R)(G)MII_RX_DV(_ER) | ENET_RX_CTL | I | 1.8V | |
| M16 | GND | | PWR | GND | |
| M17 | ETH_IOPWR | | PWR | 1.8V | |
| M19 | VCC_2_TEST | | PWR | 1.8V | |
| M20 | GND | | PWR | GND | |
| M21 | SDIO_B_D2 | NAND_DATA06 | I/O | 1.8V | |
| N15 | ETH_A_(R)(G)MII_RXD2 | ENET_RD2 | I | 1.8V | |
| N17 | JTAG_TCK(SWCLK) | JTAG_TCK | I | 1.8V | |
| N19 | JTAG_TMS(SWDIO) | JTAG_TMS | I | 1.8V | |
| N20 | SDIO_B_D3 | NAND_DATA07 | I/O | 1.8V | |
| N21 | SDIO_B_D4 | NAND_RE_B | I/O | 1.8V | |
| P2 | GND | | PWR | GND | |
| P4 | GND | | PWR | GND | |
| P15 | ETH_A_(R)(G)MII_RXD3 | ENET_RD3 | I | 1.8V | |
| P17 | JTAG_TDI | JTAG_TDI | I | 1.8V | |
| P18 | GND | | PWR | GND | |
| P20 | SDIO_B_D5 | NAND_CE2_B | I/O | 1.8V | |
| P21 | SDIO_B_D6 | NAND_CE3_B | I/O | 1.8V | |
| R1 | GND | | PWR | GND | |
| R2 | PCIe_SM_ALERT# | SAI3_TXFS | I | 1.8V | PU: 2k2 |
| R15 | ETH_A_(R)(G)MII_RX_CLK | ENET_RXC | I/O | 1.8V | |
| R16 | GND | | PWR | GND | |
| R17 | JTAG_TDO(SWO) | JTAG_TDO | O | 1.8V | |
| R19 | JTAG_nTRST | JTAG_TRST_B | I | 1.8V | PU: 10k |
| R20 | GND | | PWR | GND | |
| R21 | SDIO_B_D7 | NAND_CLE | I/O | 1.8V | |
| T1 | PCIe_SMCLK | I2C4_SCL | O | 1.8V | PU: 2k2 |
| T2 | PCIe_WAKE# | SAI5_RXC | I | 1.8V | PU: 10k |
| T15 | ETH_MDIO | ENET_MDIO | I/O | 1.8V | PU: 10k |
| T16 | ETH_MDC | ENET_MDC | O | 1.8V | |
| T17 | FORCE_RECOVERY# | BOOT_MODE1 | I | 1.8V | PU: 10k |
| T20 | SDIO_B_IOPWR | | PWR | 1.8V | |
| T21 | SDIO_B_CD# | SAI2_RXC | I | 1.8V | PU: 10k |
| U1 | PCIe_SMDAT | I2C4_SDA | I/O | 1.8V | PU: 2k2 |

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| U2 | GND | | PWR | GND | |
| U4 | GND | | PWR | GND | |
| U15 | SPI_A_SDI_(IO0) | NAND_DATA00 | I/O | 1.8V | |
| U16 | SPI_A_SCK | NAND_ALE | O | 1.8V | |
| U17 | SYS_RST# | | I | 1.8V | PU: 100k |
| U18 | VCC_OUT_IO | | PWR | 1.8V | |
| U20 | SDIO_B_WP | SAI2_RXD0 | I | 1.8V | PU: 10k |
| U21 | SDIO_B_PWR_EN | NAND_READY_B | O | 1.8V | |
| V1 | GND | | PWR | GND | |
| V15 | SPI_A_SDO_(IO1) | NAND_DATA01 | I | 1.8V | |
| V16 | GND | | PWR | GND | |
| V17 | CARRIER_PWR_EN | SAI2_MCLK | O | 1.8V | |
| V18 | I2S_MCLK | SAI5_MCLK | O | 1.8V | |
| V2 | PCIe_A_PERST# | SAI5_RXFS | O | 1.8V | |
| V20 | GND | | PWR | GND | |
| V21 | I2S_A_DATA_IN | SAI5_RXD0 | I | 1.8V | |
| W1 | PCIe_REFCLK_P | PCIE_CLK_P | O | | |
| W2 | PCIe_CLKREQ# | SAI3_RXFS | I | 1.8V | PU: 10k |
| W3 | GND | | PWR | GND | |
| W15 | SPI_A_/HOLD_(IO3) | NAND_DATA03 | I/O | 1.8V | |
| W16 | SPI_A_/WP_(IO2) | NAND_DATA02 | I/O | 1.8V | |
| W17 | RTC_PWR | | PWR | 3.0V | e.g. Li-Cell |
| W18 | I2S_LRCLK | SAI5_RXD1 | I/O | 1.8V | |
| W20 | I2S_BITCLK | SAI5_RXD2 | I/O | 1.8V | |
| W21 | I2S_A_DATA_OUT | SAI5_RXD3 | O | 1.8V | |
| Y1 | PCIe_REFCLK_N | PCIE_CLK_N | O | | |
| Y2 | GND | | PWR | GND | |
| Y8 | VCC_IN_5V_Y8 | | PWR | 5.0V | |
| Y9 | VCC_IN_5V_Y9 | | PWR | 5.0V | |
| Y10 | VCC_IN_5V_Y10 | | PWR | 5.0V | |
| Y11 | VCC_IN_5V_Y11 | | PWR | 5.0V | |
| Y15 | SPI_A_CS0# | NAND_CE0_B | O | 1.8V | |
| Y17 | VCC_IN_5V_Y17 | | PWR | 5.0V | |
| Y18 | GND | | PWR | GND | |
| Y21 | SPI_B_SCK | ECSPI2_SCLK | O | 1.8V | |
| Y22 | SPI_B_SDI | ECSPI2_MISO | I | 1.8V | |
| Y23 | SPI_B_SDO | ECSPI2_MOSI | O | 1.8V | |
| AA1 | GND | | PWR | GND | |
| AA3 | DSI_TE | SAI2_RXFS | I | 1.8V | |
| AA4 | GND | | PWR | GND | |
| AA7 | GND | | PWR | GND | |
| AA8 | GND | | PWR | GND | |
| AA9 | PWR_BTN# | ONOFF | I | 1.8V-5.0V | PU: 10k |
| AA10 | GND | | PWR | GND | |
| AA11 | GND | | PWR | GND | |

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| AA14 | GND | | PWR | GND | |
| AA15 | I2C_A_SCL | | O | 1.8V | PU: 2k2 |
| AA16 | I2C_A_SDA | | I/O | 1.8V | PU: 2k2 |
| AA17 | GND | | PWR | GND | |
| AA19 | GND | | PWR | GND | |
| AA20 | I2C_B_SCL | I2C3_SCL | O | 1.8V | PU: 2k2 |
| AA21 | I2C_B_SDA | I2C3_SDA | I/O | 1.8V | PU: 2k2 |
| AA22 | GND | | PWR | GND | |
| AA23 | SPI_B_CS0# | ECSPI2_SS0 | O | 1.8V | |
| AB1 | PCIe_A_HSI0_P | PCIE_RXN_P | I | | |
| AB2 | PCIe_A_HSI0_N | PCIE_RXN_N | I | | |
| AB3 | GND | | PWR | GND | |
| AB4 | DSI_DATA3_P | MIPI_DSI_D3_P | O | | |
| AB5 | DSI_DATA3_N | MIPI_DSI_D3_N | O | | |
| AB6 | GND | | PWR | GND | |
| AB7 | DSI_CLOCK_P | MIPI_DSI_CLK_P | O | | |
| AB8 | DSI_CLOCK_N | MIPI_DSI_CLK_N | O | | |
| AB9 | GND | | PWR | GND | |
| AB10 | DSI_DATA0_P | MIPI_DSI_D0_P | O | | |
| AB11 | DSI_DATA0_N | MIPI_DSI_D0_N | O | | |
| AB13 | USB_A_D_N | USB1_DN | I/O | | |
| AB14 | USB_A_ID | USB1_ID | I | 1.8V | PU: 10k |
| AB15 | GND | | PWR | GND | |
| AB16 | USB_A_VBUS | USB1_VBUS | I | 5.0V | |
| AB20 | USB_B_VBUS | USB2_VBUS | I | 5.0V | |
| AB21 | GND | | PWR | GND | |
| AB22 | USB_B_ID | USB2_ID | I | 1.8V | PU: 10k |
| AB23 | USB_B_D_N | USB2_DN | I/O | 3.3V | |
| AC2 | PCIe_A_HSO0_P | PCIE_TXN_P | O | | |
| AC3 | PCIe_A_HSO0_N | PCIE_TXN_N | O | | |
| AC4 | GND | | PWR | GND | |
| AC5 | DSI_DATA2_P | MIPI_DSI_D2_P | O | | |
| AC6 | DSI_DATA2_N | MIPI_DSI_D2_N | O | | |
| AC7 | GND | | PWR | GND | |
| AC8 | DSI_DATA1_P | MIPI_DSI_D1_P | O | | |
| AC9 | DSI_DATA1_N | MIPI_DSI_D1_N | O | | |
| AC10 | GND | | PWR | GND | |
| AC14 | USB_A_D_P | USB1_DP | I/O | 3.3V | |
| AC15 | USB_A_OC# | GPIO1_IO13 | I | 1.8V | PU: 10k |
| AC16 | USB_A_EN | GPIO1_IO12 | O | 1.8V | |
| AC20 | USB_B_EN | GPIO1_IO14 | O | 1.8V | |
| AC21 | USB_B_OC# | GPIO1_IO15 | I | 1.8V | PU: 10k |
| AC22 | USB_B_D_P | USB2_DP | I/O | 3.3V | |

***Note:*** *Not listed contacts are not connected.*

*Table 2: Pin list of contact grid*

# 2 Interface Descriptions

## 2.1 USB 2.0

The module supports two USB 2.0 OTG interfaces. For a host only configuration connect the ID signal to GND.
For external ports on carrier board an ESD protection and EMV actions are required. Place them as near as possible to the USB connectors.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| AB13 | USB_A_D_N | USB1_DN | I/O | 3.3V | |
| AB14 | USB_A_ID | USB1_ID | I | 1.8V | PU: 10k |
| AB16 | USB_A_VBUS | USB1_VBUS | I | 5.0V | |
| AB20 | USB_B_VBUS | USB2_VBUS | I | 5.0V | |
| AB22 | USB_B_ID | USB2_ID | I | 1.8V | PU: 10k |
| AB23 | USB_B_D_N | USB2_DN | I/O | 3.3V | |
| AC14 | USB_A_D_P | USB1_DP | I/O | 3.3V | |
| AC15 | USB_A_OC# | GPIO1_IO13 | I | 1.8V | PU: 10k |
| AC16 | USB_A_EN | GPIO1_IO12 | O | 1.8V | |
| AC20 | USB_B_EN | GPIO1_IO14 | O | 1.8V | |
| AC21 | USB_B_OC# | GPIO1_IO15 | I | 1.8V | PU: 10k |
| AC22 | USB_B_D_P | USB2_DP | I/O | 3.3V | |

*Table 3: USB pins on contact grid*

## 2.2 SDIO

The module supports two SDIO interfaces. SDIO_A with 4 data bits, and SDIO_B with 8 data bits.

For specification and licensing please refer the website of the SD Association http://www.sd-card.org.

The supply voltage of SD_A (SD_A_IOPWR) is switched by software between 1.8V and 3.3V.

The supply voltage of SD_B (SD_B_IOPWR) is fixed on 1.8V.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| C20 | SDIO_A_IOPWR | | PWR | 1.8V/3.3V | |
| D20 | SDIO_A_WP | SD2_WP | I | 1.8V/3.3V | PU: 10k |
| D21 | SDIO_A_PWR_EN | SD2_RESET_B | O | 1.8V/3.3V | |
| E20 | SDIO_A_CMD | SD2_CMD | I/O | 1.8V/3.3V | |
| F21 | SDIO_A_CLK | SD2_CLK | O | 1.8V/3.3V | |
| G20 | SDIO_A_D0 | SD2_DATA0 | I/O | 1.8V/3.3V | |
| G21 | SDIO_A_D1 | SD2_DATA1 | I/O | 1.8V/3.3V | |
| H20 | SDIO_A_D2 | SD2_DATA2 | I/O | 1.8V/3.3V | |
| H21 | SDIO_A_D3 | SD2_DATA3 | I/O | 1.8V/3.3V | |
| J21 | SDIO_A_CD# | SD2_CD_B | I | 1.8V/3.3V | PU: 10k |

| | | | | | |
|---|---|---|---|---|---|
| K20 | SDIO_B_CLK | NAND_WE_B | O | 1.8V | |
| K21 | SDIO_B_CMD | NAND_WP_B | I/O | 1.8V | |
| L20 | SDIO_B_D0 | NAND_DATA04 | I/O | 1.8V | |
| L21 | SDIO_B_D1 | NAND_DATA05 | I/O | 1.8V | |
| M21 | SDIO_B_D2 | NAND_DATA06 | I/O | 1.8V | |
| N20 | SDIO_B_D3 | NAND_DATA07 | I/O | 1.8V | |
| N21 | SDIO_B_D4 | NAND_RE_B | I/O | 1.8V | |
| P20 | SDIO_B_D5 | NAND_CE2_B | I/O | 1.8V | |
| P21 | SDIO_B_D6 | NAND_CE3_B | I/O | 1.8V | |
| R21 | SDIO_B_D7 | NAND_CLE | I/O | 1.8V | |
| T20 | SDIO_B_IOPWR | | PWR | 1.8V | |
| T21 | SDIO_B_CD# | SAI2_RXC | I | 1.8V | PU: 10k |
| U20 | SDIO_B_WP | SAI2_RXD0 | I | 1.8V | PU: 10k |
| U21 | SDIO_B_PWR_EN | NAND_READY_B | O | 1.8V | |

*Table 4: SDIO pins on contact grid*

## 2.3 SPI

The module supports two SPI Interfaces. There are no pull ups on the module.

| Pin | Default Function | Internal Pad | Type | Voltage |
|---|---|---|---|---|
| K17 | GPIO_A_6/SPI_A_CS1# | NAND_CE1_B | I/O | 1.8V |
| L17 | GPIO_A_7/SPI_B_CS1# | ECSPI1_SCLK | I/O | 1.8V |
| U15 | SPI_A_SDI_(IO0) | NAND_DATA00 | I/O | 1.8V |
| U16 | SPI_A_SCK | NAND_ALE | O | 1.8V |
| V15 | SPI_A_SDO_(IO1) | NAND_DATA01 | I | 1.8V |
| W15 | SPI_A_/HOLD_(IO3) | NAND_DATA03 | I/O | 1.8V |
| W16 | SPI_A_/WP_(IO2) | NAND_DATA02 | I/O | 1.8V |
| Y15 | SPI_A_CS0# | NAND_CE0_B | O | 1.8V |
| Y21 | SPI_B_SCK | ECSPI2_SCLK | O | 1.8V |
| Y22 | SPI_B_SDI | ECSPI2_MISO | I | 1.8V |
| Y23 | SPI_B_SDO | ECSPI2_MOSI | O | 1.8V |
| AA23 | SPI_B_CS0# | ECSPI2_SS0 | O | 1.8V |

*Table 5: SPI pins on contact grid*

## 2.4 I²C

The module supports up to 3 I2C Interfaces. All I²C interfaces are working on 1.8V level.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| C3 | I2C_CAM_SDA/CSI_TX_N | I2C4_SDA | I/O | 1.8V | PU: 2k2 |
| C4 | I2C_CAM_SCL/CSI_TX_P | I2C4_SCL | O | 1.8V | PU: 2k2 |
| AA15 | I2C_A_SCL | | O | 1.8V | PU: 2k2 |
| AA16 | I2C_A_SDA | | I/O | 1.8V | PU: 2k2 |
| AA20 | I2C_B_SCL | I2C3_SCL | O | 1.8V | PU: 2k2 |
| AA21 | I2C_B_SDA | I2C3_SDA | I/O | 1.8V | PU: 2k2 |

*Table 6: I2C pins on contact grid*

## 2.5 UART

The module provides 4 UART channels with:

- 7 or 8 bit data words,
- 1 or 2 stop bits
- programmable parity (even, odd or none)
- Programmable baud rates up to 5 Mbps
- UART_A & _B have flow control signals

We recommend to use UART_CON for debugging and service only.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| A14 | UART_A_RX | UART2_RXD | I | 1.8V | |
| A22 | UART_C_RX | UART4_RXD | I | 1.8V | |
| B13 | UART_A_TX | UART2_TXD | O | 1.8V | |
| B23 | UART_C_TX | UART4_TXD | O | 1.8V | |
| C13 | UART_A_RTS | SAI3_RXC | O | 1.8V | |
| C14 | UART_A_CTS | SAI3_RXD | I | 1.8V | |
| D13 | UART_B_TX | UART3_TXD | O | 1.8V | |
| D14 | UART_B_RX | UART3_RXD | I | 1.8V | |
| D15 | UART_B_RTS | ECSPI1_MISO | O | 1.8V | |
| D16 | UART_B_CTS | ECSPI1_SS0 | I | 1.8V | |
| D22 | UART_CON_RX | UART1_RXD | I | 1.8V | |
| D23 | UART_CON_TX | UART1_TXD | O | 1.8V | |

*Table 7: SPI pins on contact grid*

## 2.6 Ethernet

The module supports one 10/100/1000Mbit LAN interface via RGMII signals.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| G15 | ETH_A_(S)(R)(G)MII_TXD1 | ENET_TD1 | O | 1.8V | |
| G16 | ETH_A_(S)(R)(G)MII_TXD3 | ENET_TD3 | O | 1.8V | |
| H15 | ETH_A_(S)(R)(G)MII_TXD0 | ENET_TD0 | O | 1.8V | |
| H16 | ETH_A_(S)(R)(G)MII_TXD2 | ENET_TD2 | O | 1.8V | |
| J15 | ETH_A_(R)(G)MII_TX_CLK | ENET_TXC | I/O | 1.8V | |
| K15 | ETH_A_(S)(R)(G)MII_RXD0 | ENET_RD0 | I | 1.8V | |
| K16 | ETH_A_(R)(G)MII_TX_EN(_ER) | ENET_TX_CTL | I | 1.8V | |
| L15 | ETH_A_(S)(R)(G)MII_RXD1 | ENET_RD1 | I | 1.8V | |
| M15 | ETH_A_(R)(G)MII_RX_DV(_ER) | ENET_RX_CTL | I | 1.8V | |
| M17 | ETH_IOPWR | | PWR | 1.8V | |
| N15 | ETH_A_(R)(G)MII_RXD2 | ENET_RD2 | I | 1.8V | |
| P15 | ETH_A_(R)(G)MII_RXD3 | ENET_RD3 | I | 1.8V | |
| R15 | ETH_A_(R)(G)MII_RX_CLK | ENET_RXC | I/O | 1.8V | |
| T15 | ETH_MDIO | ENET_MDIO | I/O | 1.8V | PU: 10k |
| T16 | ETH_MDC | ENET_MDC | O | 1.8V | |

*Table 8: Ethernet pins on contact grid*

## 2.7 I2S

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| V18 | I2S_MCLK | SAI5_MCLK | O | 1.8V | |
| V21 | I2S_A_DATA_IN | SAI5_RXD0 | I | 1.8V | |
| W18 | I2S_LRCLK | SAI5_RXD1 | I/O | 1.8V | |
| W20 | I2S_BITCLK | SAI5_RXD2 | I/O | 1.8V | |
| W21 | I2S_A_DATA_OUT | SAI5_RXD3 | O | 1.8V | |

*Table 9: I²S pins on contact grid*

## 2.8 MIPI DSI

The module supports one quad lane MIPI DSI interface with following features:

- Compliant to MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- active pixel rate of 140 Mpixel/s at max 200MHz
- maximum of 1.5 Gbps per lane
- resolution up to 1080p60 or 1920x1200p60 at 24bit RGB

| Pin | Default Function | Internal Pad | Type | Voltage |
|---|---|---|---|---|
| AA3 | DSI_TE | SAI2_RXFS | I | 1.8V |
| AB4 | DSI_DATA3_P | MIPI_DSI_D3_P | O | |
| AB5 | DSI_DATA3_N | MIPI_DSI_D3_N | O | |
| AB7 | DSI_CLOCK_P | MIPI_DSI_CLK_P | O | |
| AB8 | DSI_CLOCK_N | MIPI_DSI_CLK_N | O | |
| AB10 | DSI_DATA0_P | MIPI_DSI_D0_P | O | |
| AB11 | DSI_DATA0_N | MIPI_DSI_D0_N | O | |
| AC5 | DSI_DATA2_P | MIPI_DSI_D2_P | O | |
| AC6 | DSI_DATA2_N | MIPI_DSI_D2_N | O | |
| AC8 | DSI_DATA1_P | MIPI_DSI_D1_P | O | |
| AC9 | DSI_DATA1_N | MIPI_DSI_D1_N | O | |

*Table 10: MIPI-DSI pins on contact grid*

## 2.9 MIPI CSI

The module supports one quad lance MIPI CSI interface with following features:

- Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2
- Pixel clock up to 200 MHz (at both nominal and overdrive voltage)
- Up to 150 Mpixel/s supported
- High speed: 80 Mbps to 1.5 Gbps; low power: 10Mbps

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| A2 | CSI_DATA1_N | MIPI_CSI_D1_N | I | | |
| A3 | CSI_DATA1_P | MIPI_CSI_D1_P | I | | |
| A5 | CSI_DATA2_N | MIPI_CSI_D2_N | I | | |
| A6 | CSI_DATA2_P | MIPI_CSI_D2_P | I | | |
| B1 | CSI_DATA0_P | MIPI_CSI_D0_P | I | | |
| B3 | CSI_CLOCK_N | MIPI_CSI_CLK_N | I | | |
| B4 | CSI_CLOCK_P | MIPI_CSI_CLK_P | I | | |
| B6 | CSI_DATA3_N | MIPI_CSI_D3_N | I | | |
| B7 | CSI_DATA3_P | MIPI_CSI_D3_P | I | | |
| C1 | CSI_DATA0_N | MIPI_CSI_D0_N | I | | |
| C3 | I2C_CAM_SDA/CSI_TX_N | I2C4_SDA | I/O | 1.8V | PU: 2k2 |
| C4 | I2C_CAM_SCL/CSI_TX_P | I2C4_SCL | O | 1.8V | PU: 2k2 |

*Table 11: MIPI-CSI pins on contact grid*

## 2.10 GPIOs

The GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered module, it´s not allowed to have a voltage at one of the GPIOs

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| D3 | GPIO_C_0 | SAI1_RXD4 | I/O | 1.8V | |
| D4 | GPIO_C_1 | SAI1_RXD3 | I/O | 1.8V | |
| E3 | GPIO_C_2 | SAI1_RXD2 | I/O | 1.8V | |
| E4 | GPIO_C_3 | SAI1_RXD1 | I/O | 1.8V | |
| F3 | GPIO_C_4/DISP_VDD_EN | SAI3_TXD | I/O | 1.8V | |
| F4 | GPIO_C_5/DISP_BL_PWM | SAI3_TXC | I/O | 1.8V | |
| G3 | CAM_PWR/GPIO_C_6 | SAI2_TXC | I/O | 1.8V | |
| G4 | CAM_RST#/GPIO_C_7 | SAI2_TXD0 | I/O | 1.8V | |
| D17 | GPIO_A_0 | GPIO1_IO00 | I/O | 1.8V | |
| E17 | GPIO_A_1 | GPIO1_IO01 | I/O | 1.8V | |
| F17 | GPIO_A_2 | GPIO1_IO04 | I/O | 1.8V | |
| G17 | GPIO_A_3 | GPIO1_IO05 | I/O | 1.8V | |
| H17 | GPIO_A_4 | GPIO1_IO06 | I/O | 1.8V | |
| J17 | GPIO_A_5 | GPIO1_IO07 | I/O | 1.8V | |
| K17 | GPIO_A_6/SPI_A_CS1# | NAND_CE1_B | I/O | 1.8V | |
| L17 | GPIO_A_7/SPI_B_CS1# | ECSPI1_SCLK | I/O | 1.8V | |
| D19 | GPIO_B_0 | GPIO1_IO08 | I/O | 1.8V | |
| E19 | GPIO_B_1 | GPIO1_IO09 | I/O | 1.8V | |
| F19 | GPIO_B_2 | GPIO1_IO10 | I/O | 1.8V | |
| G19 | GPIO_B_3 | GPIO1_IO11 | I/O | 1.8V | |
| H19 | GPIO_B_4 | ECSPI1_MOSI | I/O | 1.8V | |
| J19 | GPIO_B_5 | SAI1_RXD7 | I/O | 1.8V | |
| K19 | GPIO_B_6 | SAI1_RXD6 | I/O | 1.8V | |
| L19 | GPIO_B_7 | SAI1_RXD5 | I/O | 1.8V | |

*Table 12: GPIO Interface*

## 2.11 JTAG

JTAG is for debug only. Leave unconnected, if you don´t use JTAG.

Don´t put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

| Pin | Default Function | Internal Pad | Type | Voltage | Remarks |
|---|---|---|---|---|---|
| N17 | JTAG_TCK(SWCLK) | JTAG_TCK | I | 1.8V | |
| N19 | JTAG_TMS(SWDIO) | JTAG_TMS | I | 1.8V | |
| P17 | JTAG_TDI | JTAG_TDI | I | 1.8V | |
| P19 | JTAG_TDO(SWO) | NC | O | 1.8V | |
| R17 | JTAG_TDO(SWO) | JTAG_TDO | O | 1.8V | |

| | | | | | |
|---|---|---|---|---|---|
| R19 | JTAG_nTRST | JTAG_TRST_B | I | 1.8V | PU: 10k |

*Table 13: JTAG pins on contact grid*

## 2.12 PWM

PWMs are free programmable. On a non-powered module, it´s not allowed to have a voltage at one of the PWMs.

| Contact | Contact Name | Internal Pad | I/O | Voltage | Remarks |
|---|---|---|---|---|---|
| E18 | PWM_0/ DISP_BL_PWM | GPIO_IO06 | O | 1V8 | Dual function: DISP_BL_PWM |
| F18 | PWM_1 | GPIO_IO04 | O | 1V8 | |
| G18 | PWM_2 | GPIO_IO05 | O | 1V8 | |

*Table 14: PWM Interface*

# 3 eMMC

The module supports at a maximum eMMC 5.1 dual data rate.

The eMMC Flash technology (MLC / TLC) depends on the size. The eMMCs have limited erase cycles and data retention depending on the temperature. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

# 4 RTC

There is an dedicated real time clock (PCF85263ATL) on the module. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

# 5 Electrical characteristics

## 5.1 Absolute maximum ratings

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input Voltage range 3.3V IOs | -0.3 | 3.3 | 3.6 | V |
| Input Voltage range 1.8V IOs | -0.3 | 1.8 | 2.1 | V |
| Voltage on any IO with VDD_VIN off | | | 0.3 | V |
| USB VBUS | -0.3 | 5 | 5.6 | V |
| Maximum power consumption VDD_VBAT at 85°C | | | 0.6 | µA |
| Maximum output current VCC_IO | | | 100 | mA |

*Table 15: Absolute Maximum Ratings*

## 5.2 DC Electrical Characteristics

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VCC_IN_5V | Module main power | | 4.50 | 5.00 | 5.50 | V |
| RTC_PWR | RTC power | | 1.20 | 3.00 | 5.50 | V |
| USB_VBUS | USB supply voltage | | 4.50 | 5.00 | 5.50 | V |
| VCC_OUT_IO | 1.8V output for power enable on carrier board | | 1.71 | 1.80 | 1.89 | V |
| ETH_IOPWR | ETH voltage. It is used to provide the IO Voltage Level for all Ethernet inter-faces. Fixed to 1.8V. | | 1.71 | 1.80 | 1.89 | V |
| SDIO_A_IOPWR | IO voltage level. 3.3V or 1.8V. Switched by driver. | | | | | V |
| SDIO_B_IOPWR | IO voltage level. Fixed to 1.8V. | | 1.71 | 1.80 | 1.89 | V |
| $V_{ih}$ | High Level Input Voltage | | 0.70* VCC_OUT_IO | | VCC_OUT_IO | V |
| $V_{il}$ | Low Level Input Voltage | | 0 | | 0.30*OVDD | V |
| $V_{oh}$ | High Level Output Voltage | $I_{oh}$=0.10mA | VCC_OUT_IO - 0.15 | | | V |
| $V_{ol}$ | Low Level Output Voltage | $I_{ol}$=0.10mA | | | 0.15 | V |
| $I_o$ | Output current IOs 1V8 | 1.80V | | | 10.00 | mA |

| | | | | |
|---|---|---|---|---|
| $I_o$ | Output current IOs 3V3 | 3.30V | 5.00 | mA |
| $I_{VBAT}$ | Current consumption VBAT | VABAT = 3.30V<br>$T_{amb}$ = 25°C | 0.22 | µA |

*Table 16: DC Electrical Characteristics*

# 6 Thermal Specification

This Embedded Module is a high-performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors (housing, power consumption, heat spreader, airflow and many others).

In order to keep the lifetime of the system as long as possible ( please see NXP AN12468 https://www.nxp.com/docs/en/application-note/AN12468.pdf), the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
- For reducing the heat dissipation, CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS) as well as “Thermal throttling”, by an integrated temperature sensor.
    - The integrated sensor measures the die-temperature and lowers CPU clock or shut down CPU if needed.
    - DVFS lowers CPU clock and core voltage in accordance with the performance needed from the application.

For optimal use of DVFS, modify your software to only use peak performance only for short times.

The housing has big influence on the heat dissipation. There are many points to analyze:

- Is there the option of dissipating heat to the housing?
- Is there a possibility that the air can circulate in the housing?
- Is an active cooling possible?

The surrounding heat has a big effect to the temperature of the system.

**Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction!**

The following table shows nominal thermal specification of the module:

| Operating Ranges | Min | Typ. | Max | Unit |
|---|---|---|---|---|
| Consumer Grade Operating Temperature | 0.0 | | +70.0 | °C |
| Industrial Grade Operating Temperature | -20.0 | | +85.0 | °C |
| Extended Industrial Grade Operating Temperature | -40.0 | | +85.0 | °C |
| Junction Temperature i.MX8M Mini & i.MX8M Nano (C-Temp) | 0.0 | | +95.0 | °C |
| Junction Temperature i.MX8M Mini & i.MX8M Nano (I-Temp) | -40.0 | | +105.0 | °C |
| Junction to Package TOP ($\Psi_{JT}$) – i.MX8M Mini & Nano | | 0.2 | | °C/W |

*Table 17: Thermal Specification*

# 7 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

# 8 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

# 9 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

# 10 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **8.5Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **2Watt** to **4Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

**Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board**.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines

- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

# 11 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

# 12 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

# 13 Packaging

These F&S ESD-sensitive products are shipped either in ESD protective trays. One tray can hold 20 boards. An empty tray is used as top cover. The trays must be returned to F&S after use.

# 14 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.


*Figure 7: Matrix Code Sticker*

# 15 Appendix

## Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

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Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

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Specifications are subject to change without notice.

## Warranty Terms

**Hardware Warranties**
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