Hardware Documentation

FS 8ULP OSM-SF

for HW Revision 1.10

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Elektronik Systeme

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About This Document

This document describes how to use the FS 8ULP OSM-SF (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com/en/osm.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/07.2025	All	A, M, R	All	Initial version for HW Revision 1.10	SM UK

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1 Overview

1.1 Additional Documentation

The “OSM Implementation Guide” contains information which are the same for all F&S OSM products, e.g. the

- mechanical description,
- general OSM contact grid signal description,
- handling information.

The latest version can be downloaded from www.fsembedded.com/en/osm.

1.2 General Parameter

Parameter	Description
Dimensions (L x W x H)	(30.0 x 30.0 x 2.6) mm
Weight	≈ 5 g
Pin Count	332 (228 used)

Table 1: General Parameter

1.3 Block Diagram

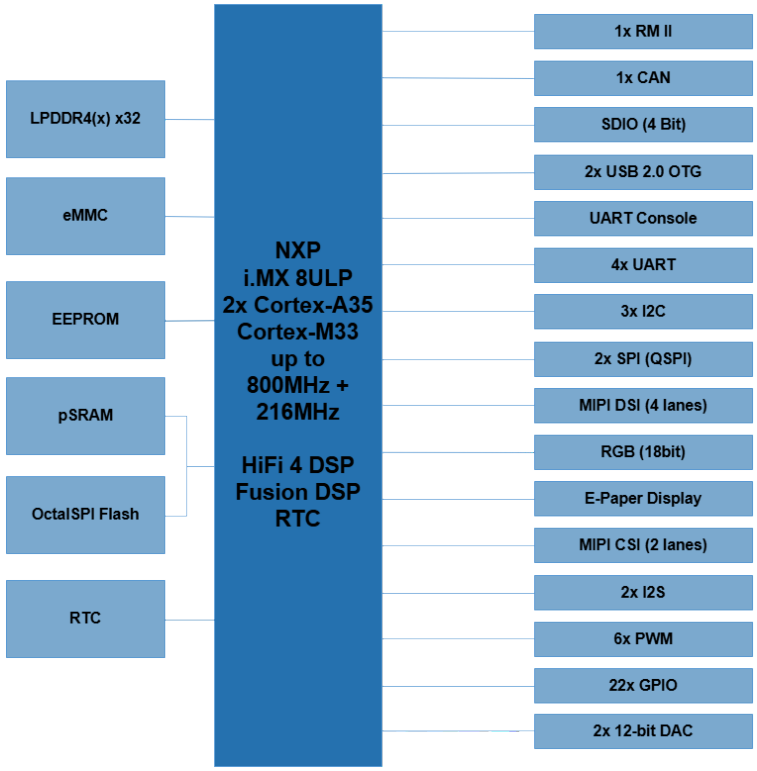


Figure 1: Block Diagram

Note: This diagram shows the maximum available features. The availability depends on the configuration.

1.4 Design Data

To ease the implementation, F&S provides the “OSM Carrier Board Design Library” which contains

- a schematic symbol (Altium & Cadence) including module-specific implementation information,
- the footprint (Altium & Cadence, baseboard side),
- a 3D model.

The latest version can be downloaded from www.fsembedded.com/en/osm.

2 Detailed Description

To increase clarity, the GND[1] pins and all pins which are not connected on the module are not listed in the following sections.

[1] All GND pins are connected on the module. F&S highly recommends to connect all of them on the carrier.

2.1 Power and Management

2.1.1 Power Supply

The following table shows the intended use of the power (PWR) pins on the module.

Contact #	Contact Name	I/O	Voltage	Comments
M19	VCC_2_TEST	PO	1.8 V	V_1V8 intended for testing purposes max. current: 50 mA
Y16	VCC_3_TEST	PO	3.3 V (1.8 V)[2]	V_PTF intended to supply carrier peripherals max. current: 100 mA
Y20	VCC_4_TEST	PO	3.3 V	V_3V3 intended to supply carrier peripherals max. current: 750 mA
Y8, Y9, Y10, Y11, Y17,	VCC_IN_5V	P	5.0 V	main power supply input
U18	VCC_OUT_IO	PO	1.8 V	general I/O reference voltage max. current: 100 mA
M17	ETH_IOPWR	PO	1.8 V	Ethernet I/O reference voltage max. current: 100 mA
C20	SDIO_A_IOPWR	PO	1.8 V	SDIO_A I/O reference voltage max. current: 100 mA
W17	RTC_PWR	P	3.0 V	RTC supply input[1]

Table 2: PWR (pin description)

[1] RTC_PWR may be sourced from a Carrier based Li-cell or Super Cap.

[2] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I²C).

2.1.2 Erratum ERR052513: Parametric Shift on FSGPIO Output Driver

According to iMX8ULPA2_P40A (Mask Set Errata), Erratum ERR052513, NXP observed a parametric shift over time on the FSGPIO (Fail-Safe GPIO) output drivers of PTA, PTE & PTF when the IO bank is supplied by voltages above 1.98 V.

This shift only impacts the pin output driver capability and does not impact the pin analog or pin digital input functionality.

Note: In TN00188 (FSGPIO Failure Risk Assessment), NXP states that the parametric shift can be represented by a reduced output driving capability of the low-side transistor of the output driver (NMOS). The degraded output low drive current (IOL) leads to a longer fall time t_F and an increased output low voltage level (VOL). In addition, NXP describes six factors that have an impact on the speed of the degradation:

- I/O bank supply voltage (a lower voltage significantly reduces the speed of degradation)
- Signal toggling frequency (a higher frequency represents a faster degradation)
- Toggle rate (a higher toggle rate represents a faster degradation)
- Temperature (a lower effective junction temperature represents a faster degradation)
- Pin output driver configuration (slower degradation with a high drive strength and standard slew rate configuration)
- Loading capacitance (should be minimized)

For an assessment of whether this Erratum has an impact on a specific application, TN00188 contains a failure analysis and tables with estimated worst case IOL values as a function of the above parameters for different mission profiles. The latest versions of the documents

- iMX8ULPA2_P40A Mask Set Errata,
- TN00188 FSGPIO Failure Risk Assessment (login required)

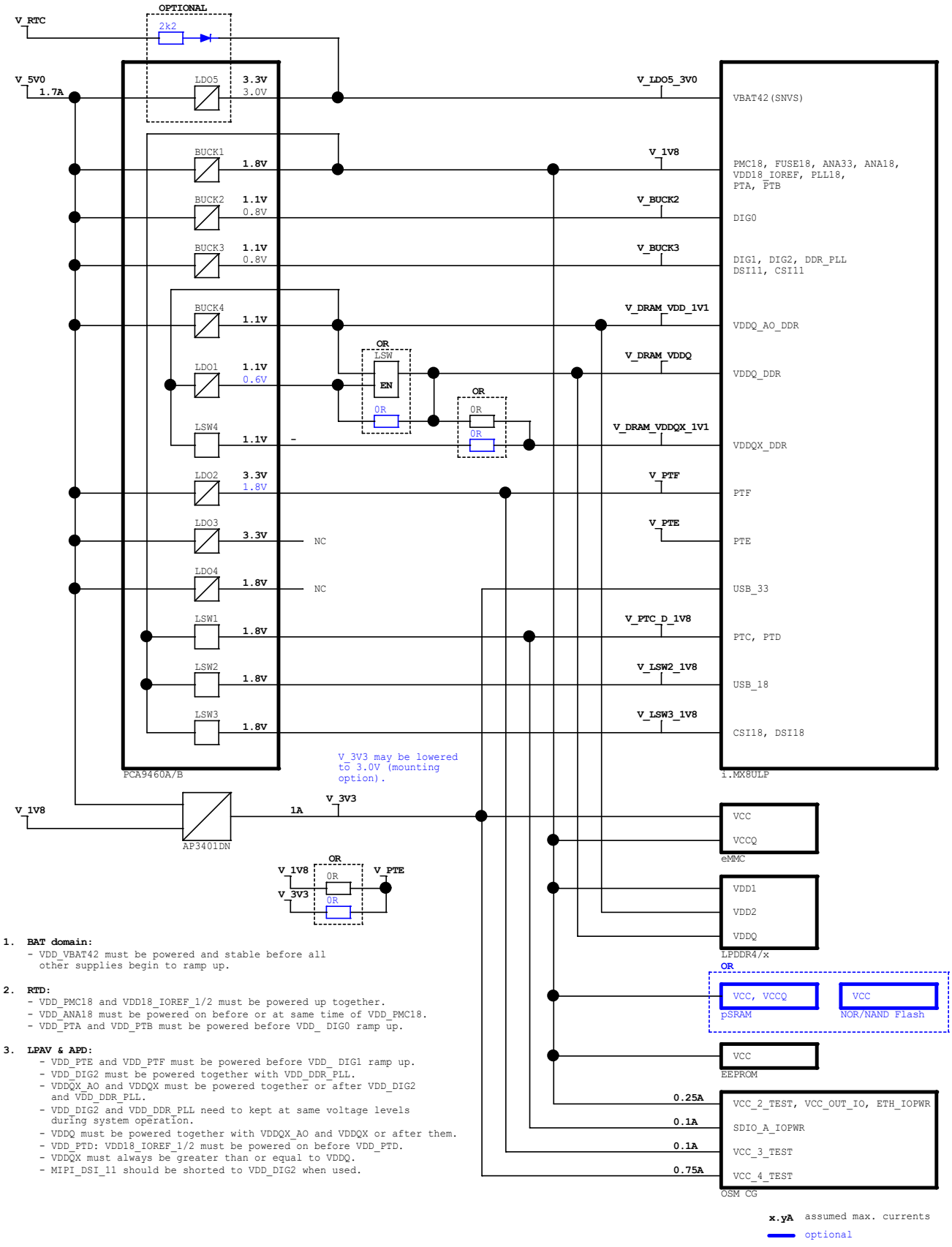
can be downloaded from the NXP website.

The NXP FSGPIO failure analysis shows that lowering the I/O bank supply voltage is a very effective approach to slow down the parametric shift over time. The module contains an adjustable DC/DC converter which generates the general 3.3 V supply voltage V_3V3 that may be lowered to V_3V3_{min} = 3.0 V (mounting option), if needed.

Peripherals on the carrier may be supplied with V_3V3 and up to 0.75 A by the module.

2.1.3 PWR Topology

The following picture visualizes the power (PWR) topology of the module.



1. **BAT domain:**
   - VDD_VBAT42 must be powered and stable before all other supplies begin to ramp up.

2. **RTD:**
   - VDD_PMC18 and VDD18_IOREF_1/2 must be powered up together.
   - VDD_ANA18 must be powered on before or at same time of VDD_PMC18.
   - VDD_PTA and VDD_PTB must be powered before VDD_ DIG0 ramp up.

3. **LPAV & APD:**
   - VDD_PTE and VDD_PTF must be powered before VDD_ DIG1 ramp up.
   - VDD_DIG2 must be powered together with VDD_DDR_PLL.
   - VDDQX_AO and VDDQX must be powered together or after VDD_DIG2 and VDD_DDR_PLL.
   - VDD_DIG2 and VDD_DDR_PLL need to kept at same voltage levels during system operation.
   - VDDQ must be powered together with VDDQX_AO and VDDQX or after them.
   - VDD_PTD: VDD18_IOREF_1/2 must be powered on before VDD_PTD.
   - VDDQX must always be greater than or equal to VDDQ.
   - MIPI_DSI_11 should be shorted to VDD_DIG2 when used.

Figure 2: Power (topology)

2.1.4 System Control

The following picture visualizes the system control (CTRL) topology of the module.

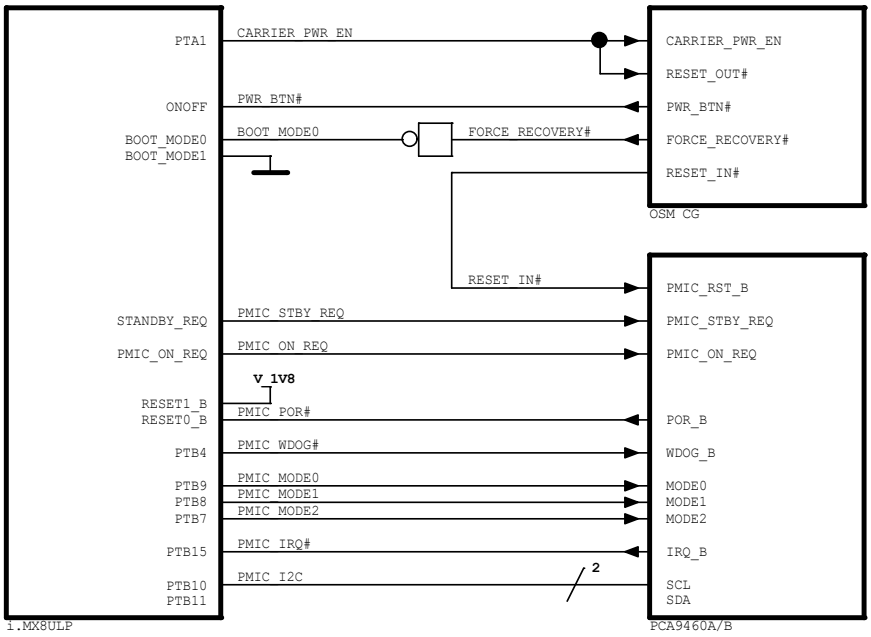


Figure 3: System Control (topology)

The following table shows the intended use of the CTRL pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V17	CARRIER_PWR_EN	PTA1	O	1.8 V	HIGH active, intended to enable the power for peripherals on carrier
U17	RESET_IN#	**PCA9460A/B:** PMIC_RST_B	I	5.0 V	PU 10k, logic LOW resets the module
Y14	RESET_OUT#	PTA1	O	1.8 V	connected to CARRIER_PWR_EN
AA9	PWR_BTN#[1]	ONOFF	I	1.8 V	PU 10k, behavior depends on the configuration
T17	FORCE_RECOVERY#	BOOT_MODE0	I	1.8 V	PU 10k HIGH/FLOAT: module boots from internal fuses LOW: module is in USB Serial Download mode

Table 3: System Control (pin description)

[1] PWR_BTN# is debounced inside of the CPU.

2.2 Interfaces

2.2.1 MISC

None of the “RESERVED” & “COM_AREA” pins are connected on the module. The following table shows the intended use of the vendor defined pins[1].

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C16	Vendor Defined	RESET0_B	I	1.8 V	PU 100k, experimental feature, must be left unconnected on the carrier
D6	Vendor Defined	DAC0_OUT	O	1.8 V	reference voltage: VCC_OUT_IO
D7	Vendor Defined	DAC1_OUT	O	1.8 V	reference voltage: VCC_OUT_IO
P16	Vendor Defined	RESET1_B	I	1.8 V	PU 100k, experimental feature, must be left unconnected on the carrier

Table 4: Vendor Defined (pin description)

[1] The OSM standard doesn't define dedicated pins for Digital-Analog-Converter (DAC) outputs on size-S modules.

2.2.2 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
N17	JTAG_TCK(SWCLK)	PTA23	I	1.8 V	
N19	JTAG_TMS(SWDIO)	PTA20	I	1.8 V	
P17	JTAG_TDI	PTA22	I	1.8 V	
R17	JTAG_TDO(SWO)	PTA21	O	1.8 V	
R19	JTAG_nTRST	PTA19	I	1.8V	

Table 5: JTAG (pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A35 and Cortex®-M33 cores via serial console. See chapter UART.

2.2.3 UART

The module provides five Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
A14	UART_A_RX	PTE11	I	1.8 V (3.3 V)[1]	
B13	UART_A_TX	PTE10	O	1.8 V (3.3 V)[1]	
C13	UART_A_RTS	PTE9	O	1.8 V (3.3 V)[1]	
C14	UART_A_CTS	PTE8	I	1.8 V (3.3 V)[1]	
D14	UART_B_RX	PTA3	I	1.8 V	
D13	UART_B_TX	PTA2	O	1.8 V	
D15	UART_B_RTS	PTA17	O	1.8 V	
D16	UART_B_CTS	PTA16		1.8 V	
A22	UART_C_RX	PTB3	I	1.8 V	Cortex®-M33 debug (RTD)
B23	UART_C_TX	PTB2	O	1.8 V	Cortex®-M33 debug (RTD)
C23	UART_D_TX	PTA10	I	1.8 V	
C22	UART_D_RX	PTA11	O	1.8 V	
D22	UART_CON_RX	PTE7	I	1.8 V (3.3 V)[1]	Cortex®-A35 debug (APD)
D23	UART_CON_TX	PTE6	O	1.8 V (3.3 V)[1]	Cortex®-A35 debug (APD)

Table 6: UART (pin description)

[1] V_PTE (PTE domain voltage) can alternatively be connected to V_3V3 as a mounting option.

2.2.4 Ethernet

The module provides one Reduced Media-Independent Interface (RMII) Ethernet (ETH) port. The following table shows the use of the ETH related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
H15	ETH_A_RMII_TXD0	PTE23	O	1.8 V (3.3 V)[1,2]	
G15	ETH_A_RMII_TXD1	PTE22	O	1.8 V (3.3 V)[1,2]	
K16	ETH_A_RMII_TX_EN(_ER)	PTE16	O	1.8 V (3.3 V)[1,2]	
J15	ETH_A_RMII_TX_CLK	PTE3	O	1.8 V (3.3 V)[1,2]	
K15	ETH_A_RMII_RXD0	PTE21	I	1.8 V (3.3 V)[1,2]	
L15	ETH_A_RMII_RXD1	PTE20	I	1.8 V (3.3 V)[1,2]	
L16	ETH_A_RMII_RX_ER	PTE17	I	1.8 V (3.3 V)[1,2]	
M15	ETH_A_RMII_RX_DV(_ER)	PTE18	I	1.8 V (3.3 V)[1,2]	

R15	ETH_A_RMII_RX_CLK	PTE19	I	1.8 V (3.3 V)[1,2]	
T15	ETH_A_MDIO	PTE14	I/O	1.8 V (3.3 V)[1,2]	
T16	ETH_A_MDC	PTE15	O	1.8 V (3.3 V)[1,2]	

Table 7: ETH (pin description)

[1] V_PTE (PTE domain voltage) can alternatively be connected to V_3V3 as a mounting option.

[2] It is important to consider the fact that ETH_IOPWR (Ethernet I/O reference voltage) is fixed to 1.8 V in all cases.

2.2.5 GPIO

Besides the PWM signals, the module provides up to 22 additional, free programmable General Purpose Input/Output (GPIO) signals[1,2]. The i.MX8ULP processor contains Standard-GPIOs (STGPIO, domains: PTC, PTD) and Fail-Safe-GPIOs (FS-GPIO, domains: PTA, PTB, PTE, PTF). The following table shows the use of the GPIO related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
D17	GPIO_A_0	PTC0	I/O	1.8 V	
E17	GPIO_A_1	PTC3	I/O	1.8 V	
F17	GPIO_A_2	PTC11	I/O	1.8 V	
G17	GPIO_A_3[3]	PTC13	I/O	1.8 V	
H17	GPIO_A_4[3]	PTC14	I/O	1.8 V	
J17	GPIO_A_5[3]	PTC15	I/O	1.8 V	
K17	GPIO_A_6[3]	PTC17	I/O	1.8 V	dual function: SPI_A_CS1#
L17	GPIO_A_7	PTA8	I/O	1.8 V	dual function: SPI_B_CS1#
D19	GPIO_B_0[3]	PTC16	I/O	1.8 V	
E19	GPIO_B_1	PTB5	I/O	1.8 V	
F19	GPIO_B_2	PTB6	I/O	1.8 V	
G19	GPIO_B_3	PTA0	I/O	1.8 V	
H19	GPIO_B_4	PTA24	I/O	1.8 V	
J19	GPIO_B_5	PTF31	I/O	3.3 V (1.8 V)[4]	
K19	GPIO_B_6	PTF30	I/O	3.3 V (1.8 V)[4]	
L19	GPIO_B_7	PTF29	I/O	3.3 V (1.8 V)[4]	
D3	GPIO_C_0	PTE0	I/O	1.8 V (3.3 V)[5]	
D4	GPIO_C_1	PTE1	I/O	1.8 V (3.3 V)[5]	
F3	GPIO_C_4	PTF4	I/O	3.3 V (1.8 V)[4]	dual function: DISP_VDD_EN
F4	GPIO_C_5	PTF3	I/O	3.3 V (1.8 V)[4]	dual function: DISP_BL_EN
G3	GPIO_C_6	PTB13	I/O	1.8 V	dual function: CAM_A_PWR
G4	GPIO_C_7	PTB14	I/O	1.8 V	dual function: CAM_A_RST#

Table 8: GPIO (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts, it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

[3] Not available when pSRAM / OctalSPI Flash is mounted.

[4] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I²C).

[5] V_PTE (PTE domain voltage) can alternatively be connected to V_3V3 as a mounting option.

2.2.6 SDIO

The module provides one Secure Digital Input Output (SDIO) interface. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E20	SDIO_A_CMD	PTD23	I/O	1.8 V[1]	
F21	SDIO_A_CLK	PTD22	O	1.8 V[1]	
G20	SDIO_A_D0	PTD21	I/O	1.8 V[1]	
G21	SDIO_A_D1	PTD20	I/O	1.8 V[1]	
H20	SDIO_A_D2	PTD19	I/O	1.8 V[1]	
H21	SDIO_A_D3	PTD18	I/O	1.8 V[1]	
J21	SDIO_A_CD#	PTD16	I	1.8 V[1]	PU 10k
D20	SDIO_A_WP	PTD17	I	1.8 V[1]	PU 10k
D21	SDIO_A_PWR_EN	PTD15	O	1.8 V[1]	

Table 9: SDIO (pin description)

[1] When SDIO_A is intended to be used with SD/MMC cards, a suitable level-translator is required on the carrier.

2.2.7 PWM

The module provides up to six free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
E18	PWM_0	PTF5	O	1.8 V	dual function: DISP_BL_PWM
F18	PWM_1	PTA9	O	1.8 V	
G18	PWM_2	PTA18	O	1.8 V	
H18	PWM_3	PTC1	O	1.8 V	
J18	PWM_4	PTC2	O	1.8 V	
K18	PWM_5[3]	PTC12	O	1.8 V	

Table 10: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

[3] Not available when pSRAM / OctalSPI Flash is mounted.

2.2.8 Analog Signals

The i.MX8ULP processor contains two dedicated Digital-Analog-Converter (DAC) outputs[1]. For the use of the DAC related pins on the module, please see chapter 2.1.1 MISC.

[1] Analog-Digital-Converter (ADC) and comparator inputs of the i.MX8ULP are available as secondary function of some PTA- & PTB domain I/Os. Please contact us for more information about the possibilities of using secondary functions in non-OSM-standard-conform configurations.

2.2.9 SPI

The module provides two Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V15	SPI_A_SDO_(IO0)[1,2]	PTC22	I/O	1.8 V	
U15	SPI_A_SDI_(IO1)[1,2]	PTC21	I/O	1.8 V	
W16	SPI_A_WP_(IO2)[1,2]	PTC20	I/O	1.8 V	
W15	SPI_A_HOLD_(IO3)[1,2]	PTC19	I/O	1.8 V	
Y15	SPI_A_CS0#	PTC23	O	1.8 V	
K17	SPI_A_CS1#[2]	PTC17	O	1.8 V	dual function: GPIO_A_6
U16	SPI_A_SCK[2]	PTC18	O	1.8 V	
Y22	SPI_B_SDI	PTA4	I	1.8 V	
Y23	SPI_B_SDO	PTA5	O	1.8 V	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AA23	SPI_B_CS0#	PTA7	O	1.8 V	
L17	SPI_B_CS1#	PTA8	O	1.8 V	dual function: GPIO_A_7
Y21	SPI_B_SCK	PTA6	O	1.8 V	

Table 11: SPI (pin description)

[1] F&S describes SPI_A as QuadSPI by default.

[2] Not available when pSRAM / OctalSPI Flash is mounted.

2.2.10 I2S

The module provides two Inter-IC Sound (I2S) interfaces. The following table shows the use of the I2S related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
V21	I2S_A_DATA_IN	PTC4	I	1.8 V	
W21	I2S_A_DATA_OUT	PTC7	O	1.8 V	
W18	I2S_A_LRCLK[1]	PTC9	I/O	1.8 V	shared with I2S_B
W20	I2S_A_BITCLK[1]	PTC8	I/O	1.8 V	shared with I2S_B
V19	I2S_B_DATA_IN	PTC5	I	1.8 V	
W19	I2S_B_DATA_OUT	PTC6	O	1.8 V	
T18	I2S_B_LRCLK[1]	PTC9	I/O	1.8 V	shared with I2S_A
T19	I2S_B_BITCLK[1]	PTC8	I/O	1.8 V	shared with I2S_A
V18	I2S_MCLK	PTC10	O	1.8 V	

Table 12: I2S (pin description)

[1] Output, if module acts in Master Mode. Input, if module acts in Slave Mode.

2.2.11 CAN

The module provides one Controller Area Network Interface (CAN). The following table shows the use of the CAN related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AC17	CAN_A_TX	PTA12	O	1.8 V	
AB17	CAN_A_RX	PTA13	I	1.8 V	

Table 13: CAN (pin description)

2.2.12 USB

The module provides two On-the-Go (OTG) Universal Serial Busses (USB), including controllers and PHYs. The following table shows the use of the USB related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB13	USB_A_D_N	USB0_DN	I/O	USB	
AC14	USB_A_D_P	USB0_DP	I/O	USB	
AB14	USB_A_ID	PTD12	I	1.8 V	PU 10k
AC15	USB_A_OC#	PTD14	I	1.8 V	PU 10k
AB16	USB_A_VBUS	USB0_VBUS_DETECT	I	5.0 V	USB VBUS detection port A[1]
AC16	USB_A_EN	PTD13	O	1.8 V	
AB13	USB_B_D_N	USB1_DN	I/O	USB	
AC14	USB_B_D_P	USB1_DP	I/O	USB	
AB14	USB_B_ID	PTE4	I	1.8 V (3.3 V)[2]	PU 10k
AC15	USB_B_OC#	PTE5	I	1.8 V (3.3 V)[2]	PU 10k

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB16	USB_B_VBUS	USB1_VBUS_DETECT	I	5.0 V	USB VBUS detection port B[1]
AC16	USB_B_EN	PTE2	O	1.8 V (3.3 V)[2]	

Table 14: USB (pin description)

[1] Must always be connected to the respective USB VBUS rail.

[2] V_PTE (PTE domain voltage) can alternatively be connected to V_3V3 as a mounting option.

2.2.13 I2C

The module provides four Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
PMIC[1]	PMIC	0x32	Power Management IC on the module
A	RTC	0x51	Real Time Clock on the module (accessible from carrier)
	EEPROM	0x50	EEPROM on the module (accessible from carrier)
	I2C_A		general I2C on carrier
B	I2C_B		general I2C on carrier
C	CAM_A_I2C		I2C, related to camera on carrier

Table 15: I2C (usage)

[1] For internal use only.

The following table shows the use of the I2C related pins on the module[1].

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AA15	I2C_A_SCL	PTE12	I/O	1.8 V (3.3 V)[2]	PU 2k2
AA16	I2C_A_SDA	PTE13	I/O	1.8 V (3.3 V)[2]	PU 2k2
AA20	I2C_B_SCL	PTA14	I/O	1.8 V	PU 2k2
AA21	I2C_B_SDA	PTA15	I/O	1.8 V	PU 2k2

Table 16: I2C (pin description)

[1] CAM_A_I2C is described in its respective section.

[2] V_PTE (PTE domain voltage) can alternatively be connected to V_3V3 as a mounting option.

2.2.14 MIPI CSI

The module provides one 2 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI), compliant with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.1. The following table shows the use of the MIPI CSI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
C1	CSI_A_DATA0_N	MIPI_CSI1_D0_N	I	MIPI CSI	
B1	CSI_A_DATA0_P	MIPI_CSI1_D0_P	I	MIPI CSI	
A2	CSI_A_DATA1_N	MIPI_CSI1_D1_N	I	MIPI CSI	
A3	CSI_A_DATA1_P	MIPI_CSI1_D1_P	I	MIPI CSI	
B3	CSI_A_CLOCK_N	MIPI_CSI1_CLK_N	I	MIPI CSI	
B4	CSI_A_CLOCK_P	MIPI_CSI1_CLK_P	I	MIPI CSI	
C2	CAM_MCK	PTB12	O	1.8 V	
C3	CAM_A_SDA	PTB1	I/O	1.8 V	PU 2k2
C4	CAM_A_SCL	PTB0	O	1.8 V	PU 2k2
G3	CAM_A_PWR	PTB13	O	1.8 V	dual function: GPIO_C_6
G4	CAM_A_RST#	PTB14	O	1.8 V	dual function: GPIO_C_7

Table 17: CSI (pin description)

2.2.15 MIPI DSI

The module provides one 4 lane MIPI Display Serial Interface (DSI), compliant with MIPI DSI specification 1.1 and supports MIPI D-PHY specification v2.1. The following table shows the use of the DISP related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
AB11	DSI_DATA0_N	DSI_DATA0_N	O	MIPI DSI	
AB10	DSI_DATA0_P	DSI_DATA0_P	O	MIPI DSI	
AC9	DSI_DATA1_N	DSI_DATA1_N	O	MIPI DSI	
AC8	DSI_DATA1_P	DSI_DATA1_P	O	MIPI DSI	
AC6	DSI_DATA2_N	DSI_DATA2_N	O	MIPI DSI	
AC5	DSI_DATA2_P	DSI_DATA2_P	O	MIPI DSI	
AB5	DSI_DATA3_N	DSI_DATA3_N	O	MIPI DSI	
AB4	DSI_DATA3_P	DSI_DATA3_P	O	MIPI DSI	
AB8	DSI_CLOCK_N	DSI_CLK_N	O	MIPI DSI	
AB7	DSI_ CLOCK _P	DSI_CLK_P	O	MIPI DSI	
AA3	DSI_TE	PTF28	O	3.3 V (1.8 V)[1]	DSI panel tearing effect signal
F3	DISP_VDD_EN	PTF4	O	3.3 V (1.8 V)[1]	dual function: GPIO_C_4
F4	DISP_BL_EN	PTF3	O	3.3 V (1.8 V)[1]	dual function: GPIO_C_5
E18	DISP_BL_PWM	PTF5	O	3.3 V (1.8 V)[1]	dual function: PWM_0

Table 18: DISP (pin description)

[1] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I^2C).

2.2.16 RGB

The module provides one 18-bit RGB Display Interface which is compatible with the OSM standard[1]. The following table shows the use of the RGB related pins on the module.

[1] Under certain circumstances, it is also possible to support a 24-bit RGB Display. Please contact us for more information about the possibilities of using secondary functions in non-OSM-standard-conform configurations.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
Y7	RGB_R0	PTF23	O	3.3 V (1.8 V)[1]	
AA6	RGB_R1	PTF22	O	3.3 V (1.8 V)[1]	
Y6	RGB_R2	PTF21	O	3.3 V (1.8 V)[1]	
AA5	RGB_R3	PTF20	O	3.3 V (1.8 V)[1]	
Y5	RGB_R4	PTF19	O	3.3 V (1.8 V)[1]	
Y4	RGB_R5	PTF18	O	3.3 V (1.8 V)[1]	
W4	RGB_G0	PTF17	O	3.3 V (1.8 V)[1]	
V3	RGB_G1	PTF16	O	3.3 V (1.8 V)[1]	
V4	RGB_G2	PTF15	O	3.3 V (1.8 V)[1]	
U3	RGB_G3	PTF14	O	3.3 V (1.8 V)[1]	
T3	RGB_G4	PTF13	O	3.3 V (1.8 V)[1]	
T4	RGB_G5	PTF12	O	3.3 V (1.8 V)[1]	
R4	RGB_B0	PTF11	O	3.3 V (1.8 V)[1]	
R3	RGB_B1	PTF10	O	3.3 V (1.8 V)[1]	
P3	RGB_B2	PTF9	O	3.3 V (1.8 V)[1]	
N3	RGB_B3	PTF8	O	3.3 V (1.8 V)[1]	
N4	RGB_B4	PTF7	O	3.3 V (1.8 V)[1]	
M3	RGB_B5	PTF6	O	3.3 V (1.8 V)[1]	
M4	RGB_CLK	PTF24	O	3.3 V (1.8 V)[1]	

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
L3	RGB_VSYNC	PTF25	O	3.3 V (1.8 V)[1]	
K3	RGB_HSYNC	PTF26	O	3.3 V (1.8 V)[1]	
K4	RGB_DISP	PTF1	O	3.3 V (1.8 V)[1]	
J4	RGB_DE	PTF27	O	3.3 V (1.8 V)[1]	
J3	RGB_RESET#	PTF0	O	3.3 V (1.8 V)[1]	
H3	RGB_CS#	PTF2	O	3.3 V (1.8 V)[1]	

Table 19: RGB (pin description)

[1] V_PTF (PTF domain voltage) can be changed in steps of 50 mV (programmable via I^2C).

2.2.17 E-Paper Display

The i.MX8ULP processor contains an Electrophoretic Display Controller (EPDC). Therefore, and under certain circumstances, the module offers the possibility to support E-Paper displays[1].

[1] Please contact us for more information about the possibilities of using secondary functions in non-OSM-standard-conform configurations.

2.3 Internal Peripherals on the Module

2.3.1 LPDDR4 / LPDDR4x

The module contains one 32-bit LPDDR4/x[1] SDRAM which operates with up to 1056 MT/s.

[1] optional

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 pSRAM / OctalSPI Flash

The module offers the possibility of mounting a pSRAM or OctalSPI Flash as an additional memory[1]. The following picture visualizes the pSRAM / OctaclSPI Flash options.

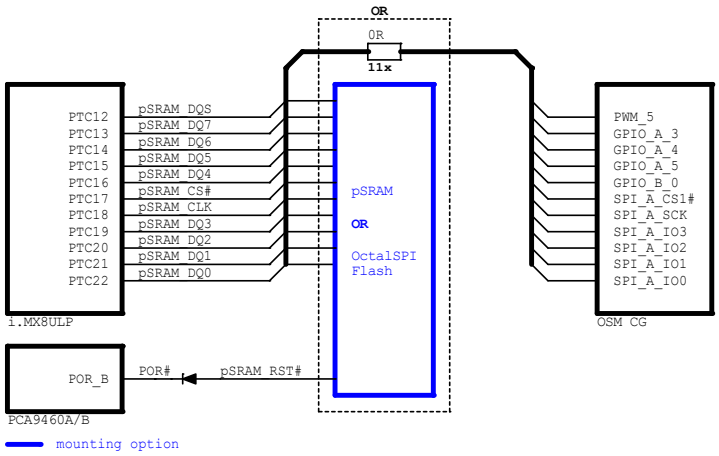


Figure 4: pSRAM / OctalSPI Flash (mounting option)

[1] SPI_A, some GPIOs & PWM_5 are not available at the contact grid, when this option is used.

2.3.4 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to I2C_A (address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

Optionally, the discrete RTC can be replaced by the internal RTC of the i.MX8ULP. With this option, the security batt domain of the i.MX8ULP remains supplied, even if the rest of the module itself is not supplied. The disadvantage is a significant higher battery current. The following picture visualizes the RTC options.

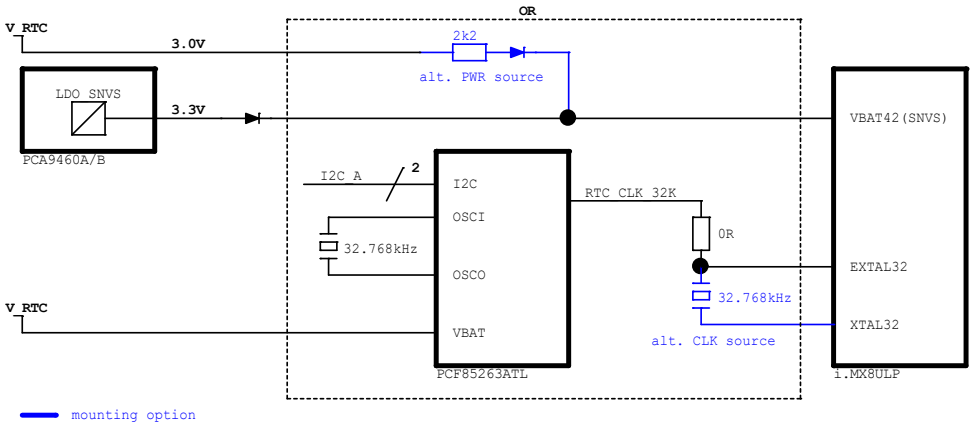


Figure 5: RTC (mounting options)

2.3.5 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50).

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
V_{5V}	main power input voltage at the V_5V_IN pins	-0.50	6.00	V
V_{RTC}	RTC battery input voltage at the RTC_PWR pin	-0.30	4.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.15	V_{DD} + 0.15	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.60	V

Table 20: Absolute Maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
General						
V_{5V}	main power input[1]		4.50	5.00	5.50	V
I_{5V}					1.70	A
V_{RTC}	RTC battery input	contact: **W17** V_{RTC} = 3.0 V	2.50	3.00	4.00	V
I_{RTC}				0.35	100	µA
USB VBUS	PHY detection of USB VBUS	contact: **AB16, AB20**		5.00		V
$V_{VCC\_2\_TEST}$	supply output (for testing purposes)	contact: **M19**		1.80		V
$I_{VCC\_2\_TEST}$					50	mA
$V_{VCC\_3\_TEST}$	supply output (for carrier peripherals)	contact: **Y16**	1.80	3.30		V
$I_{VCC\_3\_TEST}$					100	mA
$V_{VCC\_4\_TEST}$	supply output (for carrier peripherals)	contact: **Y20**	3.00	3.30		V
$I_{VCC\_4\_TEST}$					750	mA
$V_{VCC\_OUT\_IO}$	supply output (general I/O reference)	contact: **U18**		1.80		V
$I_{VCC\_OUT\_IO}$					100	mA
V_{ETH_IOPWR}	supply output (Ethernet I/O reference)	contact: **M17**		1.80		V
I_{ETH_IOPWR}					100	mA
$V_{SDIO\_A\_IOPWR}$	supply output (SDIO_A I/O reference)	contact: **C20**		1.80		V
$I_{SDIO\_A\_IOPWR}$					100	mA
Standard GPIO (STGPIO)						
V_{IH}	STGPIO I/O high-level input voltage	V_{DD} = 1.8 V (PTB, PTC, PTD)	0.7 · V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	STGPIO I/O low-level I/O input voltage		0		0.3 · V_{DD}	V
V_{OH}	STGPIO I/O high-level output voltage		0.8 · V_{DD}		V_{DD}	V
V_{OL}	STGPIO I/O low-level I/O output voltage				0.125 · V_{DD}	V
Fail-Safe GPIO (FSGPIO)						
V_{IH}	FSGPIO I/O high-level input voltage	V_{DD} = 1.8 V / 3.3 V (PTE, PTF) PTA: V_{DD} = 1.8 V	1.35	V_{DD}	V_{DD}	V
V_{IL}	FSGPIO I/O low-level I/O input voltage		0		0.54	V
V_{OH}	FSGPIO I/O high-level output voltage		V_{DD} – 0.5		V_{DD}	V
V_{OL}	FSGPIO I/O low-level I/O output voltage				0.5	V
12-bit DAC						
C_L	output load capacitance			50	100	pF

I_L	output load current				±1	mA
$VDAC_{OUTL}$	DAC low level output voltage	R_L = 18 kΩ, C_L = 50 pF	0		0.15[3]	V
$VDAC_{OUTH}$	DAC high level output voltage		1.65[3]		1.80	V
Temperatures						
$T_{OPERATE}$	operating temperature range[2]	C TEMP grade	0		70	°C
		I TEMP grade	-25		85	°C
		XI TEMP grade	-40		85	°C
$T_{STORAGE}$	storage temperature range		-40		85	°C
$t_{STORAGE}$	storage time	no environmental control		6	months	
		T_{AMB} = 25 °C ± 5 °C humidity max. 60 %		12	months	

Table 21: Recommended Operating Conditions

[1] The OSM standard requires 5.0 V ± 5 %, but the module is tested and validated within the specified range.

[2] An external cooling solution may be required to cover the entire range.

[3] It is recommended to operate the DAC in the output voltage range between 0.15 V … 1.65 V.

4 Packaging & Labels

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5 Appendix

5.1 Second source rules

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