Hardware Documentation

armStoneMX8ULP

for HW Revision 1.00

Version 005/03.2026

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About This Document

This document describes how to use the armStoneMX8ULP (further named as armStone) with mechanical and electrical information. The latest version of this document can be found at: www.fs-net.de.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

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History

Version/Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
002/01.2025	-	-	All	Initial Version	SM
004/11.2025	-	A	2.1.2	Add chapter : “Erratum ERR052513”	SM
005/03.2026	-	M	2.9	LVDS max. resolution corrected	UK

Table of Content

Tables

Figures

1 Overview

1.1 Additional Documentation

This armStone contains an adapted FS 8ULP OSM-SF.

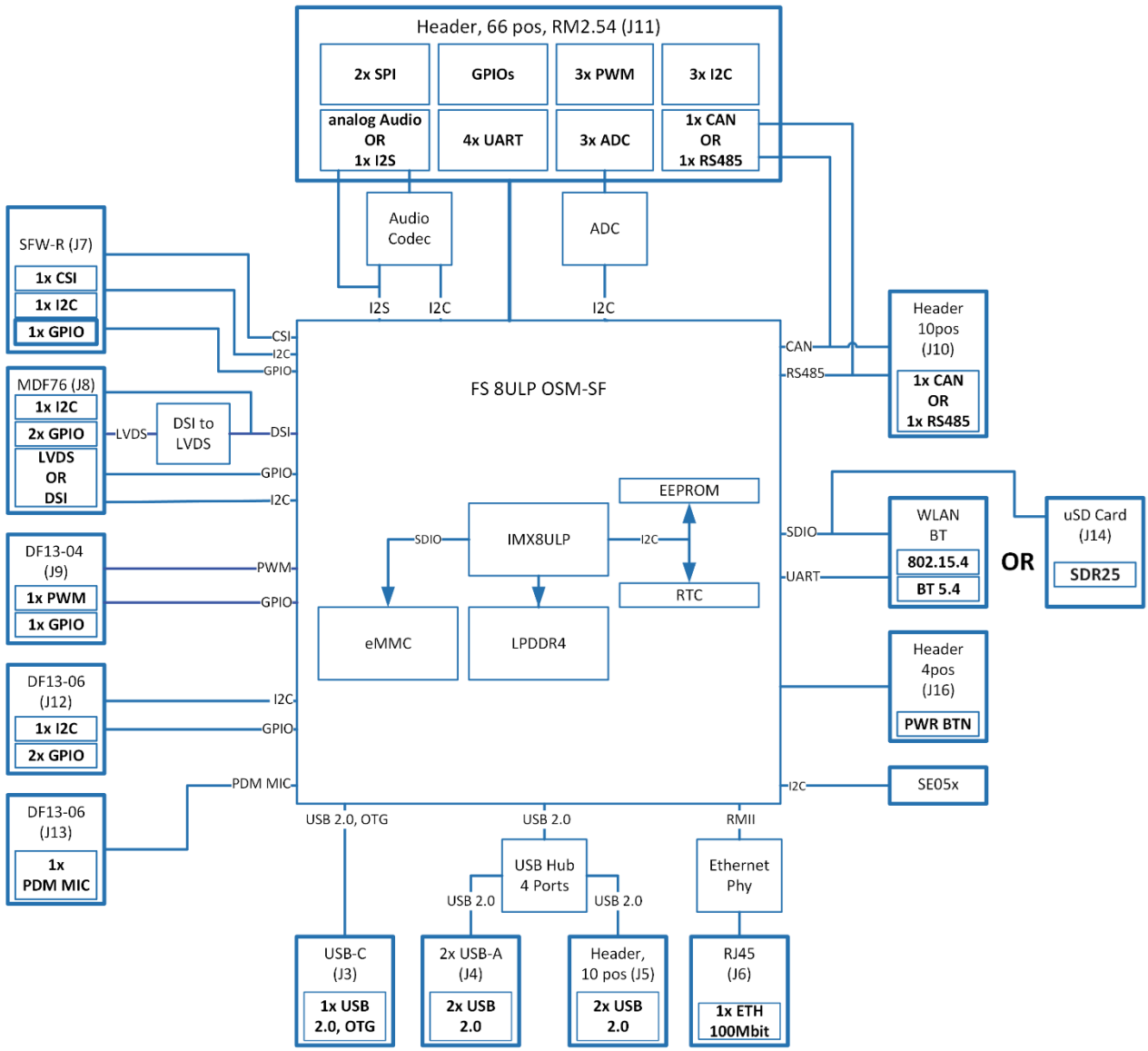
The latest versions of the documents can be found on www.fs-net.de.

1.2 General Parameter

Parameter	Description
Dimension	100.0 mm x 72.0 mm x 19.5 mm
Weight	≈ 50.0 g
Operating Temperature	-25.0 °C … +85.0 °C
Mounting Holes	4x Ø 3.2 mm

Table 1: General parameter

1.3 Block Diagram

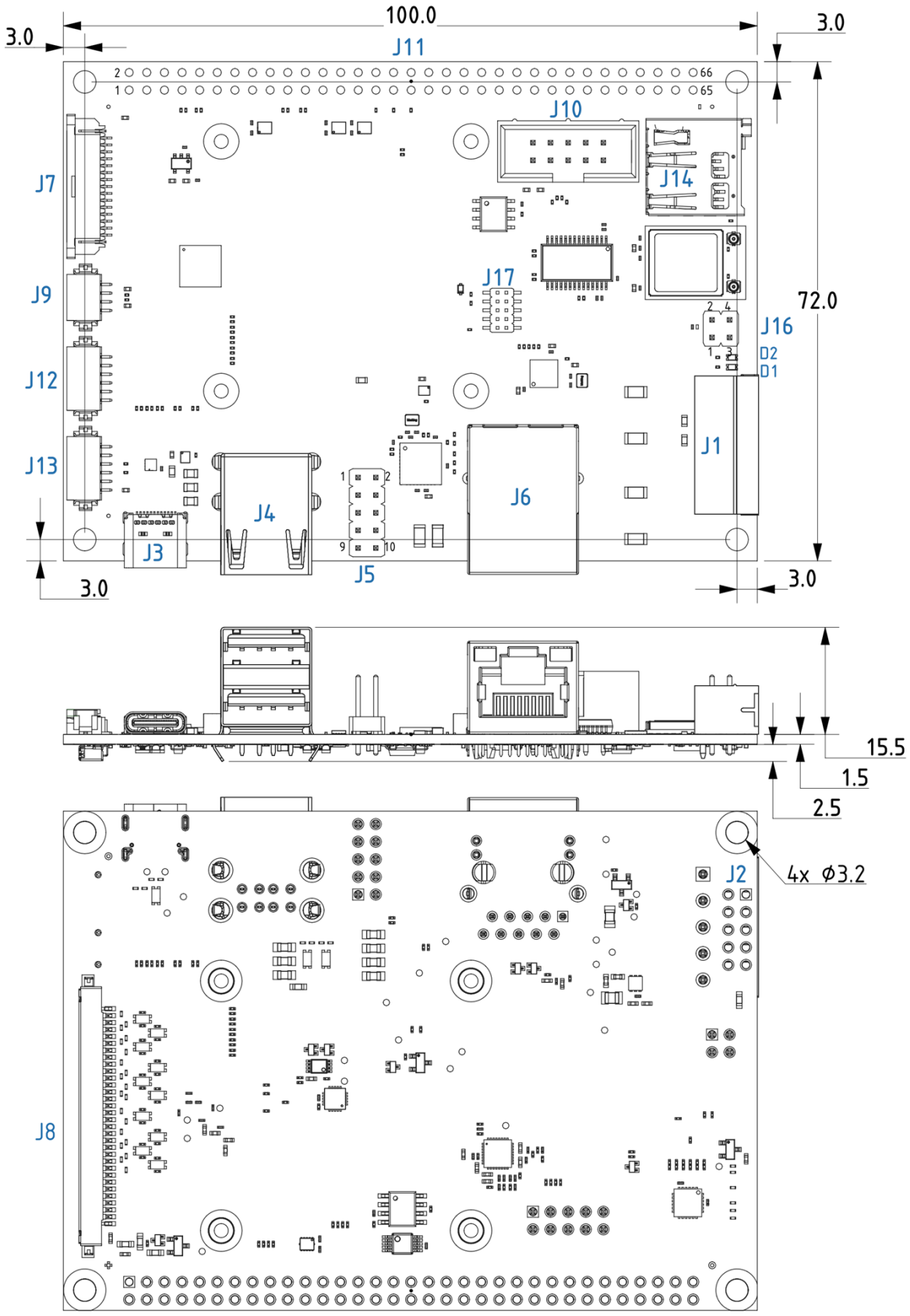


Note: This diagram shows the maximum available features. The availability depends on the configuration.

Figure 1: Block diagramm

1.4 Dimensions and Connectors

1.4.1 Technical Drawing



Note: All dimensions are in mm.

Figure 2: Technical drawing

1.4.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Power Input	Phoenix Contact, MC 1,5/5-G-3,81	Phoenix Contact, MC 1,5/ 5-ST-3,81
J2	Power Input (optional)	2x5 pos RM: 2.54 mm	
J3	1x USB 2.0, OTG	Type C	
J4	2x USB 2.0	2x Type A	
J5	2x USB 2.0	2x5 pos RM: 2.54 mm	
J6	Ethernet	RJ45	
J7	Camera	Amphenol, SFW15R-1	FPC cable, 15pos, Pitch: 1.00 mm[1]
J8	Display	Hirose, MDF76GW-30S-1H	JAE, FI-X30H[1]
J9	Backlight Connector	Hirose, DF13-04	Hirose, DF13-4S-1.25C[1]
J10	RS485 / CAN	2x5 pos RM: 2.54 mm, shrouded	
J11	Feature Connector	2x33 pos RM. 2.54 mm	
J12	General Purpose Connector	Hirose, DF13-06	Hirose, DF13-6S-1.25C[1]
J13	PDM Microphone	Hirose, DF13-06	Hirose, DF13-6S-1.25C[1]
J14	SD Card	Micro SD	
J16	Power Button & LED	2x2 pos RM: 2.54 mm	
J17	JTAG	2x5 pos RM: 1.27 mm	
D1	5.0 V indicator	LED yellow	
D2	3.3 V indicator	LED yellow	

[1]Connectors and preassembled cables are available for purchase at www.fs-net.de.

Table 2: Connector description

1.5 Variants

Variant	Processor	Memory	ADC	SPI B	RS485	UART B RTS/CTS	CAN Transceiver	Wifi	Bluetooth	uSD Card	USB Hub	Ethernet 100 Mbit	LVDS	MIPI-DSI	MIPI-CSI	PDM MIC In	Audio Codec	T_{AMB}
V2I	NXP i.MX 8ULP (MIMX8UD5CVP08SC) 2x A35 (800MHz) 1x M33 (216 MHz) Hifi 4 DSP (600 MHz)	1 GB LPDDR4 8 GB eMMC 64 kbit EEPROM	✓	✓	✓	✓	✓			✓	✓	✓	✓		✓	✓	✓	-25 °C to +85 °C
V4I	NXP i.MX 8ULP 2x A35 (800MHz) 1x M33 (216 MHz) Hifi 4 DSP (600 MHz)	2 GB LPDDR4 8 GB eMMC 64 kbit EEPROM	✓	✓	✓		✓	✓	✓		✓	✓	✓		✓	✓	✓	-25 °C to +85 °C

Table 3: Variants description

2 Detailed Description

2.1 Power Management

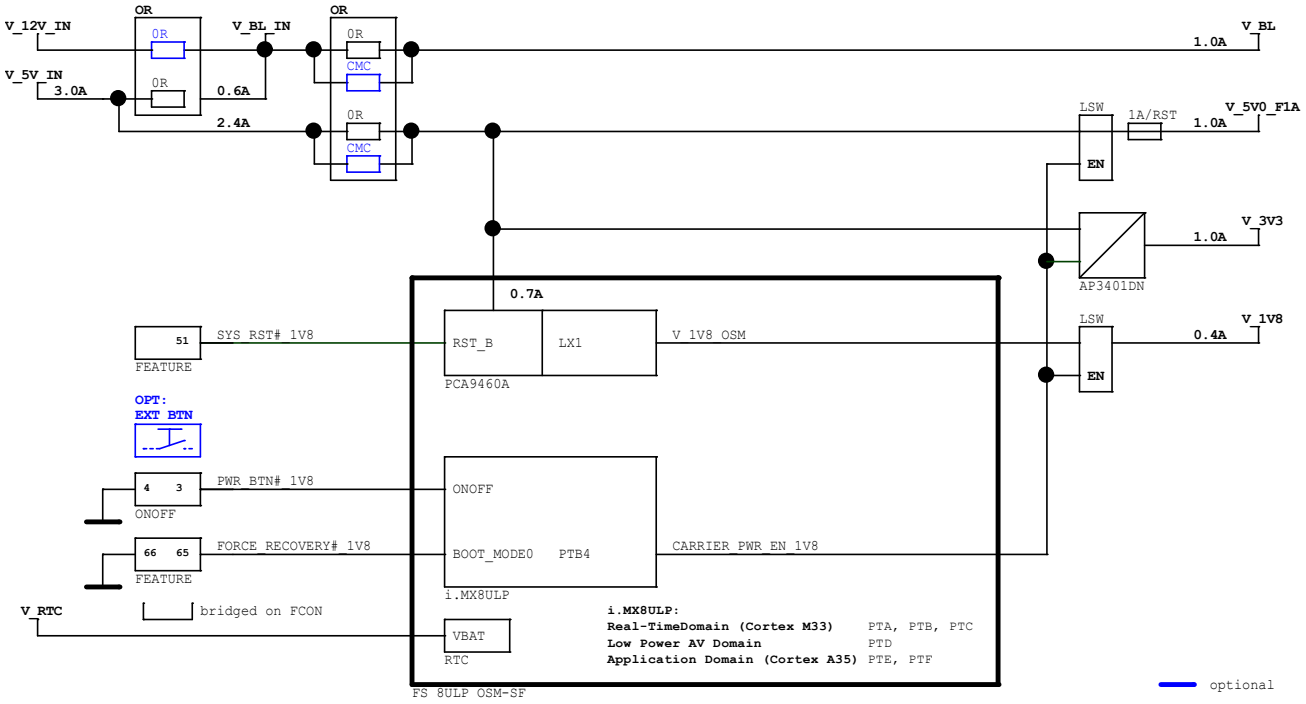


Figure 3: Block diagram power supply & system control

2.1.1 Power Supply

There are three different power rails. The RTC (Real Time Clock) and the backlight only must be connected when needed.

Commonly the armStone is supplied via J1.

The backlight supply is directly routed to J9 (see chapter 2.9.4). This simplifies the wiring and is optimized for the usage of the ADP-NT24V4[1] power supply module.

[1]More Information can be found on www.fs-net.de

Pin	Signal Name	Voltage	I/O	Description
1				GND
2	V_RTC	3.0 V	PWR	RTC supply input
3	V_5V_IN	5.0 V	PWR	Main power supply Input
4				GND
5	V_12V_IN	12.0 V	PWR	Backlight supply input

Table 4: J1 pin description

2.1.2 Erratum ERR052513: Parametric Shift on FSGPIO Output Driver

According to iMX8ULPA2_P40A (Mask Set Errata), Erratum ERR052513, NXP observed a parametric shift over time on the FSGPIO (Fail-Safe GPIO) output drivers of PTA, PTE & PTF when the IO bank is supplied by voltages above 1.98 V.

This shift only impacts the pin output driver capability and does not impact the pin analog or pin digital input functionality.

Note: In TN00188 (FSGPIO Failure Risk Assessment), NXP states that the parametric shift can be represented by a reduced output driving capability of the low-side transistor of the output driver (NMOS). The degraded output low drive current (IOL) leads to a longer fall time t_F and an increased output low voltage level (VOL). In addition, NXP describes six factors that have an impact on the speed of the degradation:

- I/O bank supply voltage (a lower voltage significantly reduces the speed of degradation)
- Signal toggling frequency (a higher frequency represents a faster degradation)
- Toggle rate (a higher toggle rate represents a faster degradation)

- Temperature (a lower effective junction temperature represents a faster degradation)
- Pin output driver configuration (slower degradation with a high drive strength and standard slew rate configuration)
- Loading capacitance (should be minimized)

For an assessment of whether this Erratum has an impact on a specific application, TN00188 contains a failure analysis and tables with estimated worst case IOL values as a function of the above parameters for different mission profiles. The latest versions of the documents

- iMX8ULPA2_P40A Mask Set Errata,
- TN00188 FSGPIO Failure Risk Assessment (login required)

can be downloaded from the NXP website.

The NXP FSGPIO failure analysis shows that lowering the I/O bank supply voltage is a very effective approach to slow down the parametric shift over time. The module contains an adjustable DC/DC converter which generates the general 3.3 V supply voltage V_3V3 that may be lowered to V_3V3_{min} = 3.0 V (mounting option), if needed.

2.1.3 System Control

There are various external signals to control the armStone (see Table 5). The peripheral hardware on the armStone can be internally turned on and off with the CARRIERE_PWR_EN_1V8 signal (see Figure 3). As a simple control, two LEDs indicate the peripheral voltages V_5V0_F1A (D1) and V_3V3 (D2).

Pin	Signal	Voltage	I/O	PU/PD	Description
51	SYS_RST#	5.0 V	I	PU 100k	System reset, low active
65	FORCE_RECOVERY#	1.8 V	I	PU 10k	Selects recovery mode over USB OTG, low active
66	GND				

Table 5: Control signal description (J11)

Pin	Signal	Voltage	I/O	PU/PD	Description
1	LED_3V3	3.3 V	O	PU 1.5k	Contact for an external LED, same as D2
2	GND				
3	PWR_BTN#	1.8 V	I	PU 10k	Power button, low active, debounced
4	GND				

Table 6: Control signal description (J16)

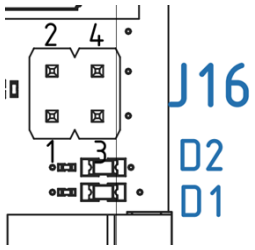


Figure 4: Detailed view of J16

2.2 I2C

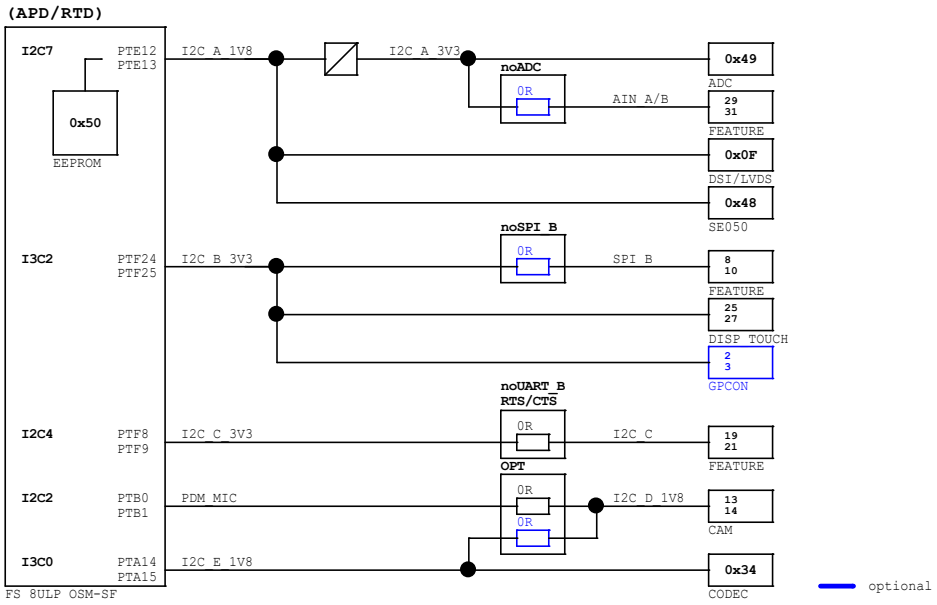


Figure 5: Block diagram I2C

There are six I2C buses available (one is for internal use only). All channels have 2.2 kΩ pull up resistors. The buses are connected to the following components.

Ch.	Voltage	Connected Part	Adress	Description
Int	1.8 V	RTC	0x51	Internal real time clock
		PMIC	0x32	Internal power management chip
A	3.3 V	ADC	0x49	Analog digital converter, if used
		J11	-	Feature Connector
	1.8 V	EEPROM	0x50	Internal EEPROM
		DSI / LVDS conv.	0x0F	DSI to LVDS converter, if LVDS option is used
		SE050	0x48	Security chip
B	3.3 V	J8	-	Display connector
		J11	-	Feature Connector, when SPI B is not used
		J12	-	General purpose connector
C	3.3 V	J11	-	Feature Connector
D	1.8 V	J7	-	Camera connector, when PDM microphone is **not used**
E	1.8 V	Audio Codec	0x34	Audio codec, if used
		J7	-	Camera connector, when PDM microphone is **used**

Table 7: I2C usage

2.3 CAN

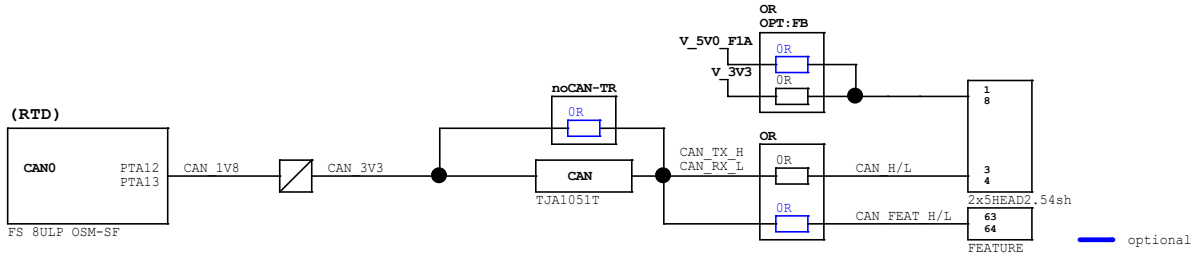


Figure 6: Block diagram CAN

The armStone has one CAN bus with a “transceiver option“ (including a 120 Ω termination) and “no transceiver option”.

CAN is normally connected to J10 (see Table 8) but can optionally be routed to J11 (see Table 14). In this case RS485 is removed from J11 and connected to J10.

Pin	Signal	Voltage	I/O	Description
1	V_CAN	3.3 V /5.0 V	PWR	Supply voltage that can be either connected to V_3V3 or V_5V0
2	GND			
3	CAN_L (RS485 N)		I/O	Optional CAN_RX[1]
4	CAN_H (RS485 P)		I/O	Optional CAN_TX[1]
5	GND			
6	n.c.			
7	n.c.			
8	V_CAN	3.3 V /5.0 V	PWR	Supply voltage that can be either connected to V_3V3 or V_5V0
9	n.c.			
10	n.c.			

[1]In case of missing transceiver

Table 8: J10 pin description

2.4 Serial

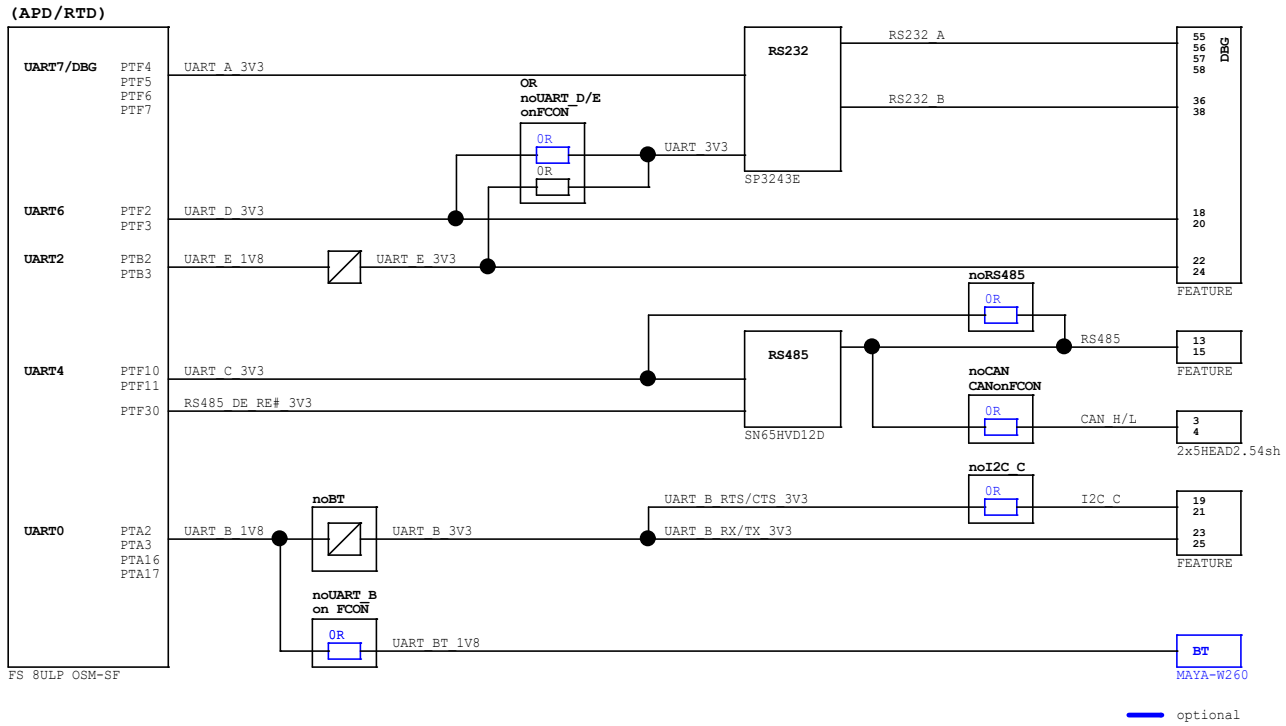


Figure 7: Block diagram Serial

2.4.1 UART

The armStone has five UART channels. Four of these channels (UART B to E) are directly available, depending on the feature options. All UARTs can be connected to the Feature Connector (J11).

2.4.2 RS232

The armStone has a 2-channel RS232 transceiver (RS232 A and RS232 B). The debug port is dedicated to UART A.

As an option, RS232 B (default: UART E) can be connected to UART D. The respective other UART (D or E) can be used on the Feature Connector (J11).

2.4.3 RS485

The armStone has one RS485 transceiver (including a 120 Ω termination) which is connected to UART C. RS485 is normally connected to the Feature Connector (J11, see Table 14) but can optionally be routed to J10 (see Table 8). In this case CAN is removed from J10 and connected to J11.

UART C can also be directly connected to J11.

2.5 USB

2.5.1 USB OTG

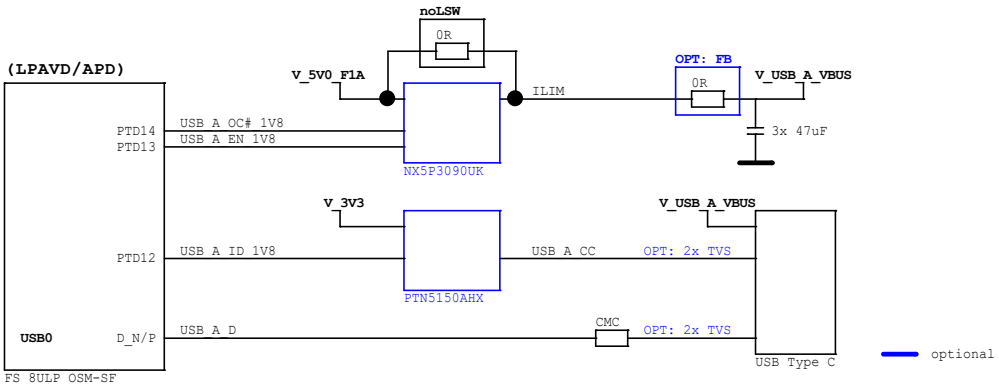


Figure 8: Block diagram USB OTG

The armStone has one USB 2.0 OTG port on connector J3. This port is used as a boot source for recovery.

As an option TVS diodes for ESD protection and a ferrite bead for supply filtering can be mounted. It is also possible to define the port permanently as an upstream facing port (UFP) or downstream facing port (DFP) for cost reduction[1].

[1]In the case of an UFP port, the recovery functionality is disabled.

2.5.2 USB Host

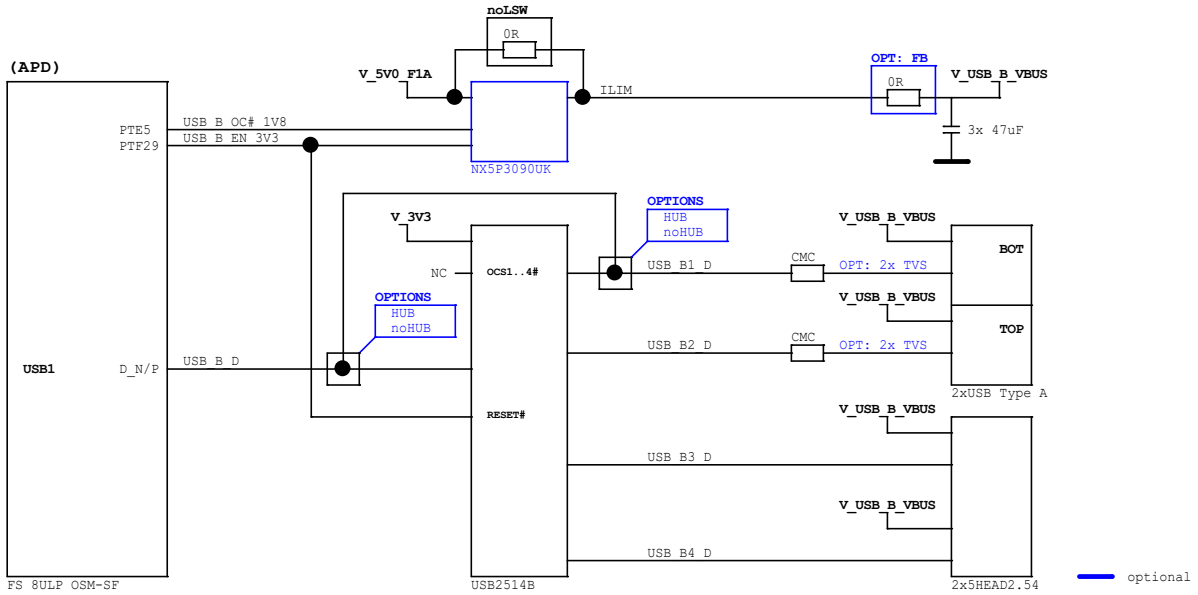


Figure 9: Block diagram USB host

Ther are four USB 2.0 host ports on two connectors (J4, J5). All ports are connected to a USB hub[1]. All ports share the same voltage domain. This domain can be switched and current limited[2].

Optional the supply of these ports can be filtered by a ferrite bead. The ports on J4 can be ESD protected by TVS diodes additionaly[3]. J5 is for internal use and has no additional ESD protection[3] or signal filtering option.

For the pinning of J5 see Table 9 and Figure 10.

[1]For cost optimization, a reduction to one port on J4 is possible.
[2]Optinal feature
[3]The USB hub is ESD protected up to 4kV (HBM)

Pin	Signal	Voltage	I/O	Description
1	V_USB_B_VBUS	5.0 V	PWR	USB supply
2				
3	USB_B3_D_N		I/O	USB data negative on hub port 3
4	USB_B4_D_N		I/O	USB data positive on hub port 3
5	USB_B3_D_P		I/O	USB data negative on hub port 4
6	USB_B4_D_P		I/O	USB data positive on hub port 4
7	GND			
8				
9	Shield			
10				

Table 9: J5 pin description

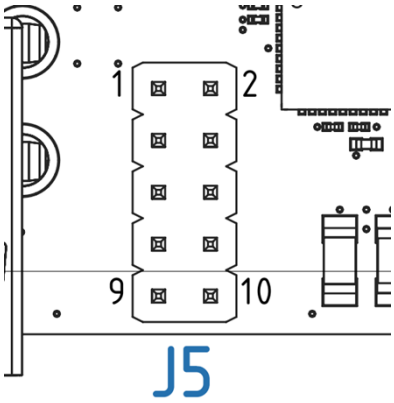


Figure 10: Detailed view of J5

2.6 Ethernet

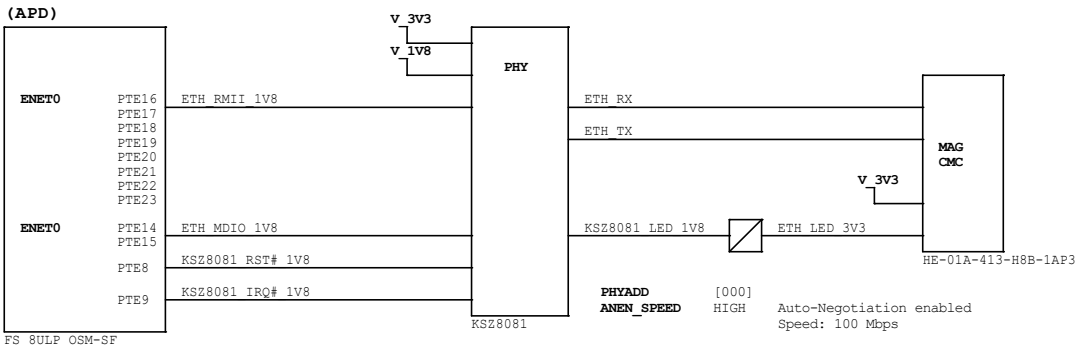


Figure 11: Block diagram ethernet

The armStone uses a Microchip KSZ8081 physical layer transceiver (PHY) for one 100 Mbit/s ethernet port on J6. The PHY address is set to [000]. Only the green LED of J6 is connected[1].

[1]LED function: No Link = OFF, Link = ON, Act = Toggle

2.7 Micro SD Card

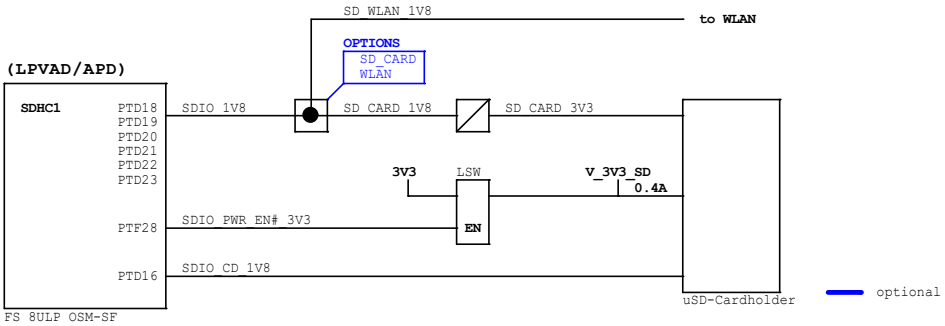


Figure 12: Block diagram microSD card

The armStone has a µSD card slots that supports High Speed mode with a Frequency up to 50 MHz and a data rate up to 25 MB/s.

2.8 Wi-Fi and Bluetooth

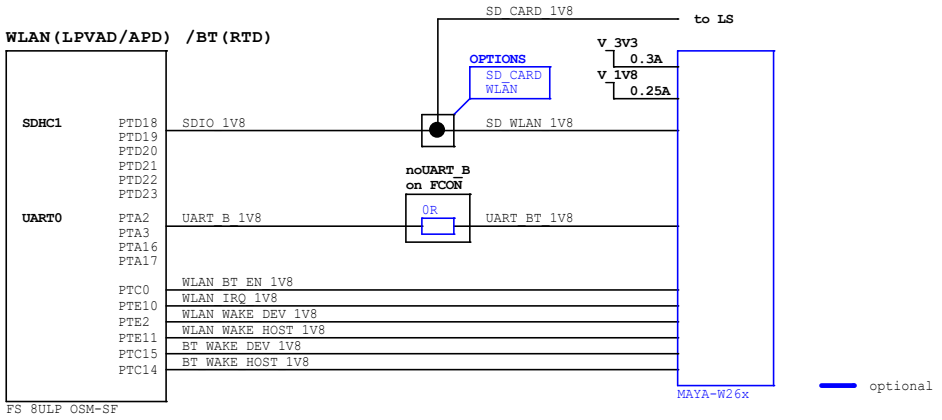


Figure 13: Block diagram Wi-Fi and Bluetooth

For Wi-Fi 6 and Bluetooth v5.4 functionality a ublox Maya-W26x module can optionally be implemented. This feature excludes the usage of the microSD card slot and UART B on the Feature Connector.

2.9 Display

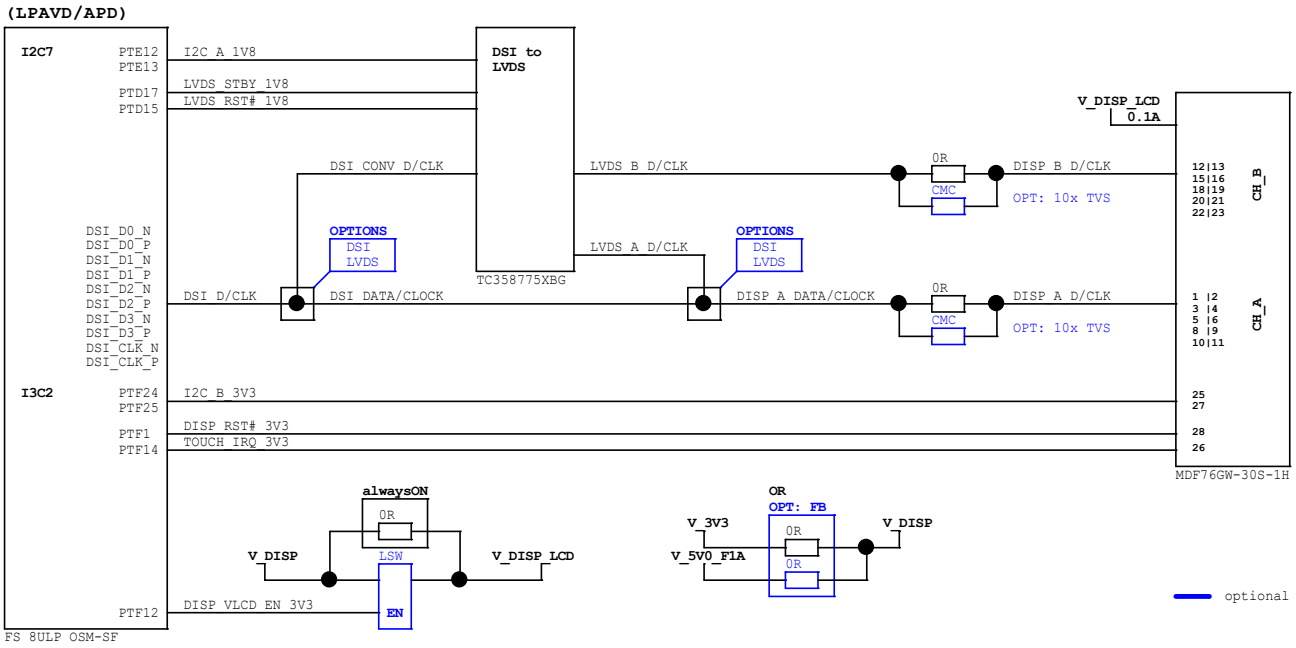


Figure 14: Block diagram display

There are two mutually exclusive display ports available on J8, with different standards. All display signals can optionally be filtered with common mode chokes and ESD protected by TVS diodes.

J8 also includes an I2C bus and two GPIOs for display control.

As an option the display supply is switchable.

2.9.1 DSI

The i.MX8ULP natively provides a 4-lane DSI interface. It supports MIPI Specification for D-PHY v2.1. The maximum resolution is (1920 x 1080) pixel at 60fps.

2.9.2 LVDS

As an alternative, the TC358775XBG from Toshiba converts the DSI signals into a dual link LVDS display port. The maximum resolution is (1920 x 1080) pixel at 60fps.

2.9.3 Connector

Pin	Signal	Voltage	I/O	PU/PD	Description
1	DISP_D0_N		O		DSI or LVDS A data 0 negative
2	DISP_D0_P		O		DSI or LVDS A data 0 positive
3	DISP_D1_N		O		DSI or LVDS A data 1 negative
4	DISP _D1_P		O		DSI or LVDS A data 1 positive
5	DISP _D2_N		O		DSI or LVDS A data 2 negative
6	DISP _D2_P		O		DSI or LVDS A data 2 positive
7	GND				
8	DISP _CLK_N		O		DSI or LVDS A clock negative
9	DISP _CLK_P		O		DSI or LVDS A clock positive
10	DISP _D3_N		O		DSI or LVDS A data 3 negative
11	DISP _D3_P		O		DSI or LVDS A data 3 positive
12	LVDS_B_D0_N		O		LVDS B data 0 negative
13	LVDS_B_D0_P		O		LVDS B data 0 positive
14	GND				
15	LVDS_B_D1_N		O		LVDS B data 1 negative
16	LVDS_B_D1_P		O		LVDS B data 1 positive
17	GND				
18	LVDS_B_D2_N		O		LVDS B data 2 negative
19	LVDS_B_D2_P		O		LVDS B data 2 positive
20	LVDS_B_CLK_N		O		LVDS B clock negative
21	LVDS_B_CLK_P		O		LVDS B clock positive
22	LVDS_B_D3_N		O		LVDS B data 3 negative
23	LVDS_B_D3_P		O		LVDS B data 3 positive
24	GND				
25	I2C_B_SDA	3.3 V	I/O	PU 2.2k	I2C B signal data
26	TOUCH_IRQ	3.3 V	I/O		GPIO for touch sensor interrupt events
27	I2C_B_SCL	3.3 V	O	PU 2.2k	I2C B signal clock
28	DISP_RST#	3.3 V	I/O		GPIO for display reset
29	V_DISP	3.3 V / 5.0 V	PWR		Supply voltage
30					

Table 10: J8 pin description

2.9.4 Backlight

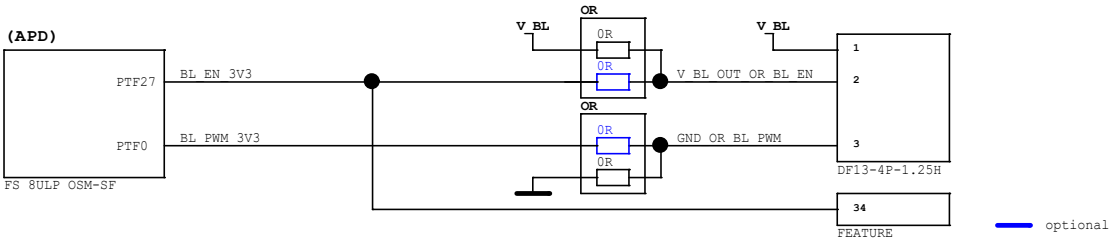


Figure 15: Block diagram backlight supply

The connector (J9) to supply a display backlight is directly routed from the supply input connector J1 (see Table 4). As default, the backlight is supplied by an individual source. Optionally the backlight supply can be connected to the V_5V0 module input voltage (see chapter 2.1).

There is also the option of two control signals on J9.

Pin	Signal	I/O	Description
1	V_BL	PWR	Supply voltage pin for a display backlight
2	V_BL (opt. BL_EN[1])	PWR (O)	Optional GPIO for backlight enable
3	GND (opt. BL_PWM)	PWR (O)	Optional PWM (pulse width modulation) for backlight dimming
4	GND		

[1]Permament available at Feature Connector pin 34

Table 11: J9 pin description

2.10 Camera

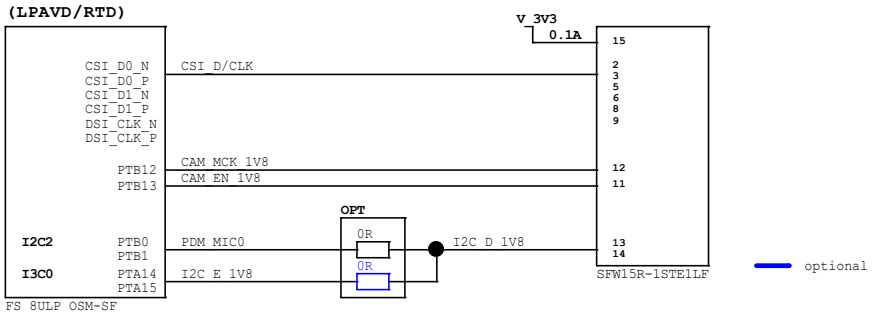


Figure 16: Block diagram camera

The armStone supports one 2-lane MIPI CSI camera interface on connector J7.

Pin	Signal	Voltage	I/O	PU/PD	Description
1	GND				
2	CSI_D0_N		I		CSI data 0 negative
3	CSI_D0_P		I		CSI data 0 positive
4	GND				
5	CSI_D1_N		I		CSI data 1 negative
6	CSI_D1_P		I		CSI data 1 positive
7	GND				
8	CSI_CLK_N		I		CSI clock negative
9	CSI_CLK_P		I		CSI clock positive
10	GND				
11	CAM_EN_1V8	1.8 V	O		GPIO for camera enable

12	CAM_MCK_1V8	1.8 V	O		Master clock
13	I2C_D_SCL_1V8	1.8 V	O	PU 2.2k	I2C D signal clock[1]
14	I2C_D_SDA_1V8	1.8 V	I/O	PU 2.2k	I2C D signal data[1]
15	V_3V3	3.3 V	PWR		Supply voltage

[1]Optional I2C E, when PDM microphone is used.

Table 12: J7 pin description

2.11 PDM Microphone

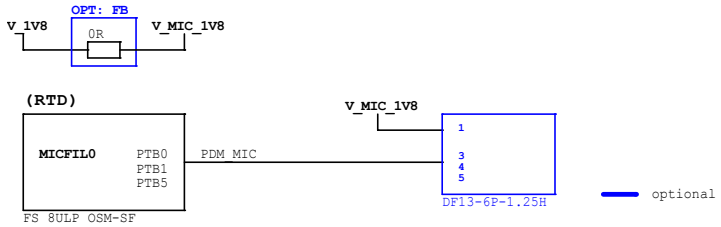


Figure 17: Block diagram PDM microphone

The i.MX8ULP supports a PDM microphone. The armStone has an optional connector for this function[1]. A ferrite bead can be applied to filter the supply voltage.

[1]The use of the PDM microphone will change the I2C channel at the camera interface.

2.12 General Purpose Connector

For generic external devices, like sensors, the general purpose connector J12 delivers some general signals and a supply.

Pin	Signal	Voltage	I/O	PU/PD	Description
1	V_3V3	3.3 V	PWR		3.3 V supply output, max. 0.5 A[1]
2	I2C_B_SDA_3V3	3.3 V	O	PU 2.2k	I2C B signal clock
3	I2C_B_SCL_3V3	3.3 V	I/O	PU 2.2k	I2C B signal data
4	GPIO_4_3V3	3.3 V	I/O		general purpose I/O
5	GPIO_5_3V3	3.3 V	I/O		general purpose I/O
6	GND				

[1]Max. 0.5 A overall including 3.3 V rail on Feature Connector

Table 13: J12 pin description

2.13 Feature Connector

The Feature Connector (J11) gives easy access to the most important signals and buses. To increase variety and flexibility, many of the pins have secondary options (further called opt.).

2.13.1 Pin List

Pin	Signal	Voltage	I/O	PU/PD	Description
1	V_3V3	3.3 V	PWR		3.3 V supply output[1]
2	V_5V0	5.0 V	PWR		5.0 V supply output[2]
3	GPIO_3	3.3 V	I/O		general purpose I/O
4	SPI_B_SCK	3.3 V	O		SPI B serial data clock
5	GPIO_5	3.3 V	I/O		general purpose I/O
6	SPI_B_CS0#	3.3 V	O		SPI B master chip Select 0
7	GPIO_7	3.3 V	I/O		general purpose I/O
8	SPI_B_SDO	3.3 V	O		SPI B serial data output (opt. I2C_B_SCL, 3.3V, PU 2.2k)

9	GPIO_9	3.3 V	I/O		general purpose I/O
10	SPI_B_SDI	3.3 V	I		SPI B serial data input (opt. I2C_B_SDA, 3.3V, PU 2.2k)
11	GND				
12	SPI_A_SCK	3.3 V	O		SPI A serial data clock
13	RS485_P		I/O		RS485 data positive
14	SPI_A_CS0#	3.3 V	O		SPI A master chip select 0
15	RS485_N		I/O		RS485 data negative
16	SPI_A_SDO	3.3 V	O		SPI A serial data output
17	SPI_A_SDI	3.3 V	I		SPI A serial data input
18	UART_D_TX	3.3 V	O		UART D transmit output
19	I2C_C_SCL	3.3 V	O	PU 2.2k	I2C C signal clock (opt. UART_B_RTS, 3.3V)
20	UART_D_RX	3.3 V	I		UART D receive input
21	I2C_C_SDA	3.3 V	I/O	PU 2.2k	I2C C signal data (opt. UART_B_CTS, 3.3V)
22	UART_E_TX	3.3 V	O		UART E transmit output
23	UART_B_TX	3.3 V	O		UART B transmit output
24	UART_E_RX	3.3 V	I		UART E receive input
25	UART_B_RX	3.3 V	I		UART B receive input
26	GPIO_26	3.3 V	I/O		general purpose I/O
27	GND				
28	PWM_1	3.3 V	O		PWM capable GPIO 1
29	AIN_A		I		Analog input channel A (opt. I2C_A_SDA, 3.3V, PU 2.2k)
30	PWM_2	3.3 V	O		PWM capable GPIO 2
31	AIN_B		I		Analog input channel B (opt. I2C_A_SCL, 3.3V, PU 2.2k)
32	PWM_3	3.3 V	O		PWM capable GPIO 3
33	AIN_C		I		Analog input channel C (opt. ADS1015_ALERT, 3.3V)
34	BL_EN	3.3 V	I/O		backlight enable signal
35	AIN_D		I		Analog input channel D
36	RS232_B_RXD		I		RS232 B receive input
37	GND				
38	RS232_B_TXD		O		RS232 B transmit output
39	V_3V3	3.3 V	PWR		3.3 V supply output[1]
40	V_5V0	5.0 V	PWR		5.0 V supply output[2]
41	AU_MIC_IN		I		Audio microphone in right (opt. I2S_DATA_OUT, 1.8V)
42	GND				
43	n.c.				
44	AU_LINE_IN_R		I		analog audio IN, right channel (opt. I2S_MCLK, 1.8V)
45	AU_OUT_R		O		analog audio OUT, right channel (opt. I2S_DATA_IN, 1.8V)
46	GND				
47	GND				
48	AU_LINE_IN_L		I		analog audio IN, left channel (opt. I2S_LRCLK, 1.8V)
49	AU_OUT_L		O		analog audio OUT, left channel (opt. I2S_BITCLK, 1.8V)
50	GND				
51	SYS_RST#	1.8 V	I		Reset input, low active
52	V_3V3	3.3 V	PWR		3.3 V supply output[1]
53	n.c.				

54	n.c.				
55	RS232_A_RXD		I		RS232 A receive input
56	RS232_A_RTS		I		RS232 A “Request to Send” handshake signal
57	RS232_A_TXD		O		RS232 A transmit output
58	RS232_A_CTS		O		RS232 A “Clear to Send” handshake signal
59	n.c.				
60	n.c.				
61	GND				
62	V_5V0	5.0 V	PWR		5.0 V supply output[2]
63	CAN_L		I/O		CAN Low, terminated with 120Ω (opt. CAN_RX, 3.3V, PU 4.7k)
64	CAN_H		I/O		CAN High, terminated with 120Ω (opt. CAN_TX, 3.3V)
65	FORCE_RECOVERY#	1.8 V	I		HIGH: Boot from Fuses LOW: Serial Donwloader
66	GND				

[1]Max 0.5 A overall on 3.3 V rail.
[2]Max 0.5 A overall on 5.0 V rail

Table 14: J11 pin description

2.13.2 SPI

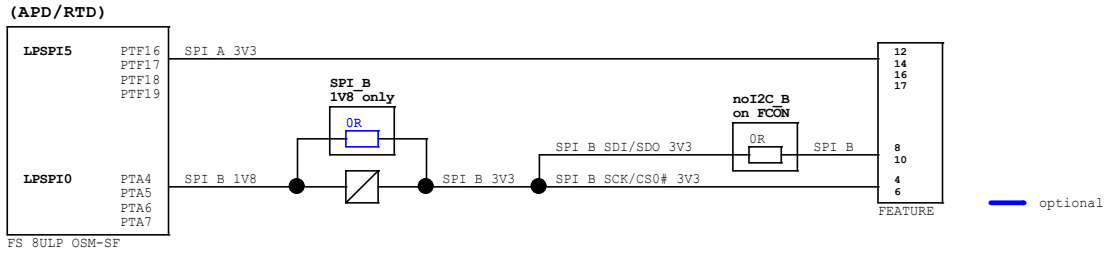


Figure 18: Block diagram SPI

The armStones supports two SPI channels1. SPI B is available at 1.8V or 3.3V level. The usage of I2C B on the feature connecter excludes SPI B.

2.13.3 PWM

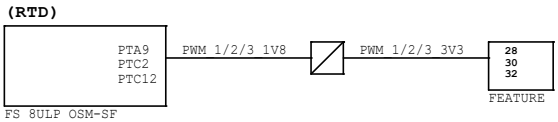


Figure 19: Block diagram PWM

The armStone has three PWM-capable outputs with a 3.3V level.

2.13.4 ADC

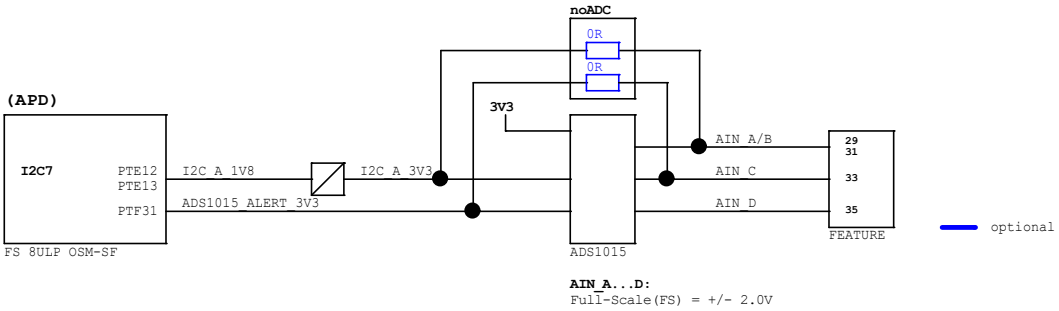


Figure 20: Block diagram ADC

The armStone has three analog inputs[1]. The input voltage range is from -2.0 V to 2.0 V with a 12-bit resolution. The analog digital converter (ADC) is connected to I2C A (address: 0x49).

[1]Alternatively I2C A and one GPIO can be directly connected to the Feature Connector.

2.13.5 GPIO

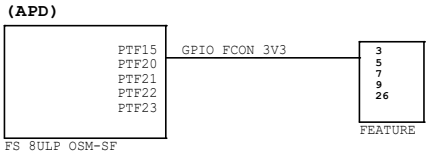


Figure 21: Block diagram GPIOs

The armStone supports five dedicated GPIOs on a 3.3 V level. Depending on the configuration, additional GPIOs may be available.

2.13.6 Audio / I2S

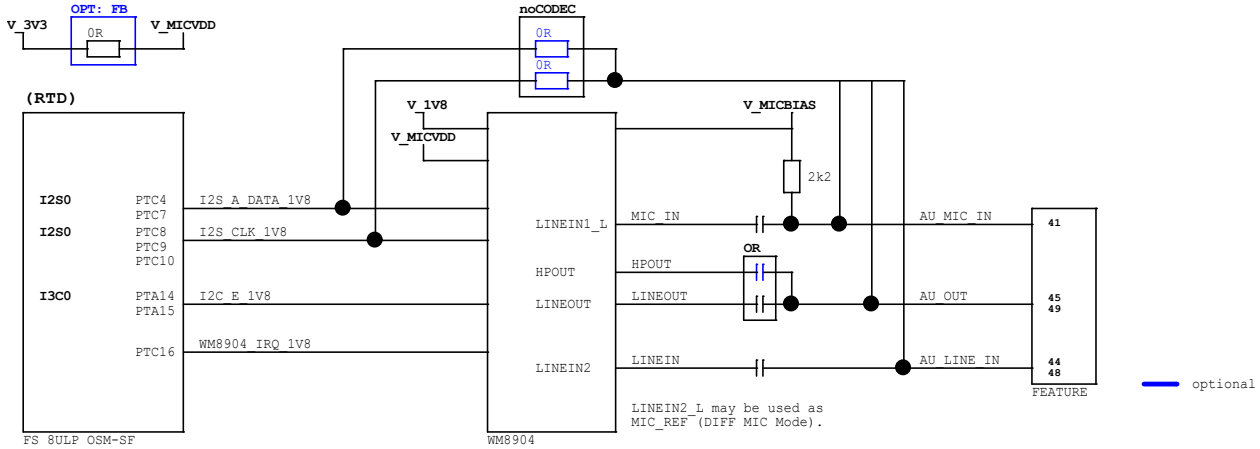


Figure 22: Block diagram audio / I2S

For analog audio applications, the WM8904 codec is mounted[1]. Depending on the configuration, the output can either be used for a headphone or LINE signals.

If needed, the microphone supply can be filtered by a ferrite bead.

[1] Alternatively to the codec, I2S signals are directly accessible at the Feature Connector (mounting option).

2.14 EEPROM

The armStone contains a 64Kb EEPROM (Type: N24S64B) which is connected to I2C_A (address: 0x50).

2.15 eMMC

The eMMC technology has limited erasing cycles and data retention depends on the temperature. It is important to know that high temperature above 50°C impacts data retention of eMMC[1], independently if the device is powered or not.

[1]Please contact us for more information about data retention on eMMCs in high temperature environments.

2.16 RTC

The armStone contains a real time clock (RTC, Type: PCF85263ATL) which is connected to the internal I2C of the OSM module (address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC[1] even if the armStone itself is not powered.

[1]**IMPORTANT NOTE:** There is no reverse current protection implemented for V_RTC on the armStone.

2.17 EdgeLock SE05x

Optionally, the security chip SE05x from NXP can be applied for security functionalities. It is connected to I2C A (address: 0x48).

3 Characteristics

3.1 Absolute Maximum Ratings

Description	Min	Max	Unit
Power Input			
Supply voltage	-0.30	6.00	V
Real time clock supply voltage	-0.50	6.50	V
Signal Input			
SPI A (3.3 V)	-0.30	3.96	V
GPIOs (3.3 V)			
UART C, D (3.3 V)			
I2C B (3.3 V)			
SPI B (1.8 V)	-0.30	1.98	V
GPIOs (1.8 V)			
I2C A, E, D (1,8 V)			
I2S (1.8 V)			
CAN (1.8 V)			
UART B, E (1.8 V)			
PDM MIC			
SPI B (3.3 V)	-0.50	6.50	V
UART B, E			
CAN			
PWM			
I2C A (3.3V)	-0.50	7.00	V
ADC IN	-0.30	3.60	V
LINE IN, MIC	-0.30	2.10	V
CAN with transceiver	-58.00	58.00	V
RS485	-9.00	14.00	V
RS232 (RxD, CTS)	-25.00	25.00	V
USB CC	-0.50	5.30	V
USB VBUS	-0.50	28.00	V

Table 15: Absolute maximum ratings

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
General						
V_5V_IN	Module main voltage		4.50	5.00	5.50	V
V_RTC	Real time clock voltage		1.20	3.00	5.50	V
V_12V_IN	Backlight voltage			12.00	24.00	V
V_USB_VBUS			4.50	5.00	5.50	V
V_3V3			3.15	3.30	3.45	V
V_1V8			1.71	1.80	1.89	V
V_CAN	Voltage output at J10. default = 3.3 V, optional = 5.0 V	default	3.15	3.30	3.45	V
		optional	4.50	5.00	5.50	V
V_DISP_LCD	Supply voltage for LCD display at J8. default = 3.3 V, optional = 5.0 V	default	3.15	3.30	3.45	V
		optional	4.50	5.00	5.50	V
$V_{IN\_HIGH\_3V3}$	High-level input voltage, 3.3 V signals		2.15		3.30	V
$V_{IN\_LOW\_3V3}$	Low-level input voltage, 3.3 V signals		0.00		1.15	V
$V_{IN\_HIGH\_1V8}$	High-level input voltage, 1.8 V signals		1.35		1.80	V
$V_{IN\_LOW\_1V8}$	Low-level input voltage, 1.8 V signals		0.00		0.45	V
$I_{V\_3V3\_OUT}$	Output current at Feature Connector				0.50[1]	A
$I_{V\_5V0\_OUT}$	Output current at Feature Connector				0.50[2]	A
P_{V_BL}	Current compatibility of backlight supply				7.00	W
$I_{V\_USB\_VBUS}$	Output current for all USB ports combined				1.00[2]	A
$I_{V\_DISP\_LCD}$	Output current at connector J8 pin	at 3.30 V			0.15[1]	A
		at 5.00 V			0.10[2]	A
I_{V_CAN}	Output current at connector J10 pin	at 3.30 V			0.15[1]	A
		at 5.00 V			0.10[2]	A
I_{V_BL}	Current through backlight path				1.00[3]	A
Analog Input / Output						
FSR_{ADC}	ADC full scale input voltage range	0 dBFS	-2.00		2.00	V
$FSR_{AU\_LINE\_IN}$	Audio LINE IN full scale input level	0 dBFS		0.500		VRMS
$FSR_{AU\_MIC\_IN}$	Audio MIC IN full scale input level	single ended 0 dBFS		0.019		VRMS
		differential 0 dBFS		0.032		VRMS
$FSR_{AU\_LINE\_OUT}$	Audio LINE OUT full scale output level	0 dBFS		1.00		VRMS
$P_{AU\_HP\_OUT}$	Audio headphone output power	0 dBFS 15 Ω … 30 Ω		30.00		mW
Storage						
T_{STORE}	Storage time	room temperature, no humidity control		12[4]	months	

[1] Overall max current is 1.00 A ($I_{V\_3V3\_OUT}$, $I_{V\_DISP\_LCD}$ @ 3.3 V, I_{V_CAN} @ 3.3 V all together)
[2] Overall max current is 1.00 A ($I_{V\_5V0\_OUT}$, $I_{V\_DISP\_LCD}$ @ 5.0 V, I_{V_CAN} @ 5.0 V all together)
[3] Current is limited to 0.60 A if backlight is supplied by V_5V_IN (mounting option).
[4] For longer storage time, vacuum dry packs are recommended

Table 16: Recommended operating conditions

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fs-net.de/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

Please contact sales@fs-net.de for RoHS and REACH statements.

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