Hardware Documentation

PicoCOM™A5
for HW Revision 1.30

Version 1.8
(2021-05-18)

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About This Document

This document describes how to use the PicCOM™A5 board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A, M, R	Chapter	Description	Au
2013-02-14	0.1	PicoCOMA5		*	New document	TM
2013-06-13	0.2	PicoCOMA5	M	3.3, 4	Add 2nd LAN option, correct PU&PD, correct features, add 2nd CAN	KW
2013-06-27	0.3	PicoCOMA5	M	3.3, 4	Alternate pin functions added, correct Host to USB2.0	KW
2013-07-03	0.4	PicoCOMA5	M	5	Add minimum voltage for USB VBUS	KW
2013-08-26	0.5	PicoCOMA5	M	4	Correct secondary CAN function on I2C signals	KW
2013-09-13	0.6	PicoCOMA5	M	4 4 5	Change PD to PU for LCDPOW and CFLPOW for HW 1.2 Add details for second CAN for HW Rev 1.2 Add details for RTC power consumtion bug	KW
2014-08-11	0.6	PicoCOMA5	M	*	Changed to new Company CI	JG
2014-08-14	1.0	PicoCOMA5	A	5	Add power consumption	KW
2014-08-14	1.1	PicoCOMA5	M	5	Correct typ. RTC battery consumption by measurement failure	KW
2014-09-19	1.2	PicoCOMA5	M	3.3	Added IO49 and IO50 to table.	HF
2014-09-22	1.2	PicoCOMA5	A	4.3, 4.7, 4.8 5.3 6	Added tables about position of interfaces. Explain what interface is compatible to PicoCOM standard. Add ESD and EMV notes Add storage conditions	HF KW
2014-10-06	1.3	PicoCOMA5	A	4.3	Added table UART FIFO depth	HF
2015-03-30	1.4	PicoCOMA5	A	4.9	Added tables about position of SD card interface. Explain what interface is compatible to PicoCOM standard.	HF
2015-07-02	1.5	PicoCOMA5	M	1	Add pin 1, pin 2 and pin 80 mark on dimension	KW
2015-07-03	1.6	PicoCOMA5	M	4.3	Correct IO for pin 69	KW
2015-08-12	1.7	PicoCOMA5	M	3.3 4.9	Add more “low active” comments and rename SDHC_CD to SDHC_CDn, LCDPOW to LCDPOWn and CFLPOW to CFLPOWn to make it more clear	KW
2021-05-07	1.8	PicoCOMA5	M	*	Update to new F&S Documentation template Update for new PCP Revision 1.30	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

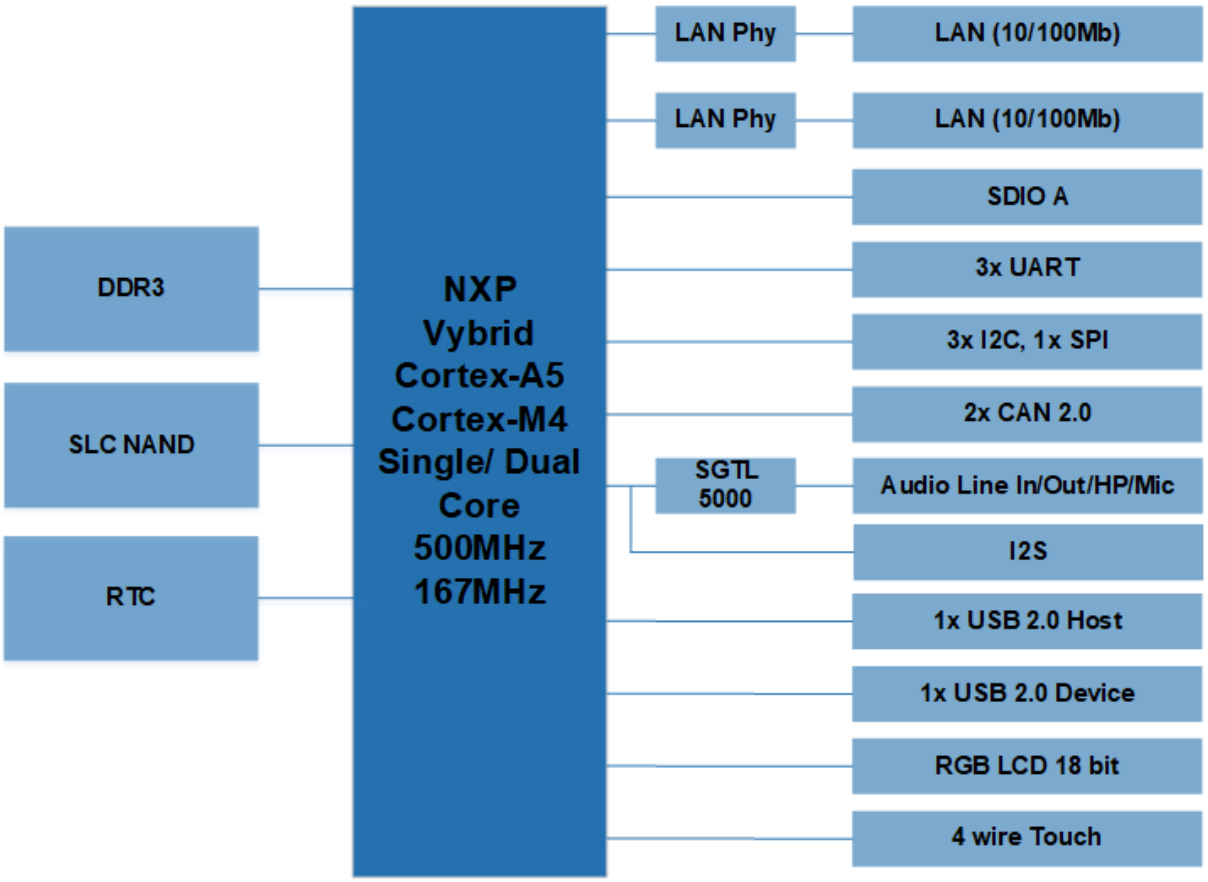

Figure 1: Block Diagram

2 Mechanical Dimension

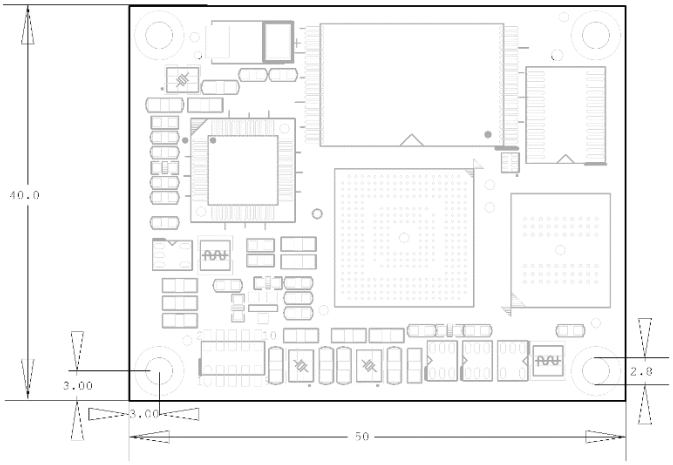

Figure 2: Mechanical Dimension Top

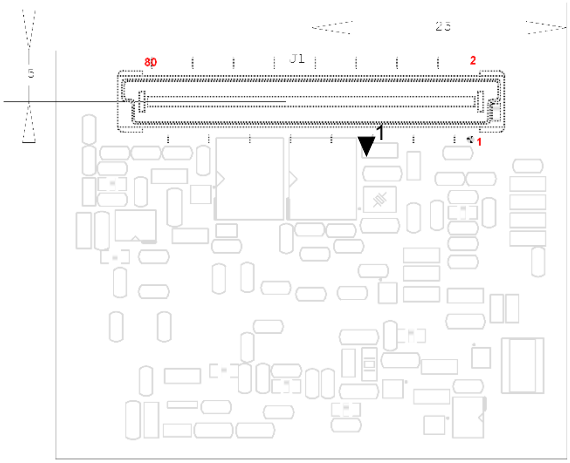

Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	50mm x 40mm
PCB Thickness	1.6mm ± 0.1mm
Height of the parts on the top side	Max. 3mm
Height of the parts on the bottom side	Max. 2.0mm
Pin Pitch of Connector	0.8mm
Mounting holes diameter	2.8mm
Mounting holes are isolated from signal ground	

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 B2B Connectors

PicoCOMA5 is using a 80 contacts connectors from manufacturer TycoElectronics.

Part number: 5177984-3

Part number counterpart:

5mm stacking height: TycoElectronics 5177983-3

9mm stacking height: TycoElectronics 5-5179009-3

13mm stacking height: TycoElectronics 5-5179010-3

Pin	Signal	CPU Pad	GPIO Number	I/O	Voltage	Remarks
1	LAN0_TX-	-	-	I/Odiff	-	
2	LAN0_RX-	-	-	I/Odiff	-	
3	LAN0_TX+	-	-	I/Odiff	-	
4	LAN0_RX+	-	-	I/Odiff	-	
5	V33			PWR	3.3V	Supply Voltage Input
6	V33			PWR	3.3V	Supply Voltage Input
7	GND			PWR	GND	
8	GND			PWR	GND	
9	VBAT	-	-	PWR	3.0V	RTC Battery Input
10	nRES	-	-	I	3.3V	Power on reset Input; onboard Pull-up 10k*⁶
11	CTS1	PTB7	IO47	I	3.3V	*²
12	SDHC_CDn	PTA7	IO48	I	3.3V	*²
13	TXD0	PTD0	IO0	O	3.3V	*²
14	RXD0	PTD1	IO1	I	3.3V	*²
15	RTS0 / TXD2	PTD2	IO2	O	3.3V	*²
16	CTS0 / RXD2	PTD3	IO3	I	3.3V	*²
17	TXD1	PTB4	IO4	O	3.3V	*1
18	RXD1	PTB5	IO5	I	3.3V	*1
19	HDPA	USB1_DP	-	I/Odiff	-	onboard Pull-Down 15k*⁶
20	HDMA	USB1_DM	-	I/Odiff	-	onboard Pull-Down 15k*⁶
21	DDP	USB0_DP	-	I/Odiff	-	
22	DDM	USB0_DM	-	I/Odiff	-	
23	USB DEVICE VBUS	USB0_VBUS_DETECT	IO6	I	5.0V	
24	USB PWR	PTE6	IO7	O	3.3V	
25	GND			PWR	GND	

Pin	Signal	CPU Pad	GPIO Number	I/O	Voltage	Remarks
26	SPI MISO	PTB20	IO8	I/O	3.3V	*1
27	SPI MOSI	PTB21	IO9	I/O	3.3V	*1
28	SPI SPCK	PTB22	IO10	I/O	3.3V	*1
29	SPI PCS0	PTB19	IO11	I/O	3.3V	*1
30	CAN0_TX I2C0_SDA	PTB15	IO49	I/O	3.3V	*1*2
31	CAN0_RX I2C0_SCL	PTB14	IO50	I/O	3.3V	*1*2
32	I2C1_SDA CAN1_TX	PTB17	IO12	I/O	3.3V	*2*7
33	I2C1_SCL CAN1_RX	PTB16	IO13	I/O	3.3V	*2*7
34	SD DAT0	PTA26	IO14	I/O	3.3V	*1*2
35	SD DAT1	PTA27	IO15	I/O	3.3V	*1*2
36	SD DAT2	PTA28	IO16	I/O	3.3V	*1*2
37	SD DAT3	PTA29	IO17	I/O	3.3V	*1*2
38	SD CLK	PTA24	IO18	I/O	3.3V	
39	SD CMD	PTA25	IO19	I/O	3.3V	
40	IRQ0	PTB26	IO20	I/O	3.3V	*2
41	PWM / ETHLED1	- / PTB8	IO21	O	3.3V	
42	GND			PWR	GND	
43	LCD0	PTE8	IO22	I/O	3.3V	*3R3
44	LCD1	PTE9	IO23	I/O	3.3V	*3R4
45	LCD2	PTE10	IO24	I/O	3.3V	*3R5
46	LCD3	PTE11	IO25	I/O	3.3V	*3R6
47	LCD4	PTE12	IO26	I/O	3.3V	*3R7
48	LCD5	PTE15	IO27	I/O	3.3V	*3G2
49	LCD6	PTE16	IO28	I/O	3.3V	*3G3
50	LCD7	PTE17	IO29	I/O	3.3V	*3G4
51	LCD8	PTE18	IO30	I/O	3.3V	*3G5
52	LCD9	PTE19	IO31	I/O	3.3V	*3G6
53	LCD10	PTE20	IO32	I/O	3.3V	*3G7
54	LCD11	PTE24	IO33	I/O	3.3V	*3B3
55	LCD12	PTE25	IO34	I/O	3.3V	*3B4
56	LCD13	PTE26	IO35	I/O	3.3V	*3B5
57	LCD14	PTE27	IO36	I/O	3.3V	*3B6
58	LCD15	PTE28	IO37	I/O	3.3V	*3B7
59	LCDCLK	PTE2	IO38	I/O	3.3V	*3
60	LCDDEN	PTE4	IO39	I/O	3.3V	*3

Pin	Signal	CPU Pad	GPIO Number	I/O	Voltage	Remarks
61	GND			PWR		GND
62	GND			PWR		GND
63	LCD16	PTE0 / PTE23	IO40	I/O	3.3V	LCD-LINE*1*3
64	LCD17	PTE1 / PTE7	IO41	I/O	3.3V	LCD-FRAME*1*3
65	LCDCC (PWM)	PTB0	IO42	I/O	3.3V	VEEK*2
66	LCDPOWn	PTE3	IO43	I/O	3.3V	LCD Power on (low active) *2
67	CFLPOWn	PTC29	IO44	I/O	3.3V	Backlight Power on (low active) *2
68	LCDENA	PTB3	IO45	I/O	3.3V	LCD Enable (not used on TFT)*2
69	RTS1 / I2S_DIN	PTB6 / PTA18	IO46	I/O	3.3V	*2*4
70	ETHLED0	-	-	O	3.3V	
71	TSPX	-	-	I	-	Touch X+
72	GND			PWR		GND
73	GND			PWR		GND
74	TSMX	-	-	I	-	Touch X-
75	TSPY	-	-	I	-	Touch Y+
76	TSMY	-	-	I	-	Touch Y-
77	LOUT / I2S_LRCLK / LAN1_TX-	- / PTA19 / -	-	O	-	Line Out Left / I2S LRCLK / Ethernet1 TX- *4*5
78	ROUT / I2S_DOUT / LAN1_RX-	- / PTA22 / -	-	I/O	-	Line Out Right / I2S DOUT / Ethernet1 RX- *4*5
79	LIN / I2S_SYS_MCLK / LAN1_TX+	- / PTB11 / -	-	I/O	-	Line In Left / I2S SYS MCLK / Ethernet1 TX+ *4*5
80	RIN / I2S_SCLK / LAN1_RX+	- / PTA16 / -	-	I/O	-	Line In Right / I2S SCLK / Ethernet1 RX+ *4*5

Table 2: B2B connector

*1: These IO-Pins are active signals during boot. Don't drive during boot process.

*2: These IO-Pins can be reconfigured as GPIO.

*3: If display is not used all these IO-Pins can be reconfigure as GPIO together.

*4: These pins have optional connections/features. See Chapter x.xx for the pin connections.

*5: These pins have optional connections/features. See Chapter x.xx for the pin connections.

*6: Mounted on HW. Some additional PU/PD can be switched on by software. Please refer SW manual or ask our support team.

*7: From HW Revision 1.20 on.

4 Interfaces

4.1 USB Host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

With the USB_PWR signal you could switch on the USB power on your current limiting IC. The usb.org webpage provides “High Speed USB Platform Design Guidelines“ with highly recommended information’s for a proper working USB design.

If the USB port is not used please leave open.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	20	USB_H1_DN	USB1_DM	I/O		90 Ohm differential pair; Preferred for host
J1	19	USB_H1_DP	USB1_DP	I/O		
J1	24	USB_H1_PWRn	PTE6	O	3.3V	Power enable

Table 3: USB Host Interface

4.2 USB OTG

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

The USB_OTG_VBUS signal does detect a connected host by detecting the voltage. This signal is 5V tolerant and needs a level above 4.5V. Do not use a voltage divider.

If the USB device port is not used please leave open.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	23	USB_OTG_VBUS	USB0_VBUS_DETECT	I	5.0V	Input; USB Phy voltage supply
J1	21	USB_OTG_DP	USB0_DP	I/O		90 Ohm differential pair
J1	22	USB_OTG_DN	USB0_DM	I/O		

Table 4: USB OTG Interface

4.3 SD Card Interface A

This interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

Pullups are integrated on the module. Card detection and write protection are not supported by the PicoCOM standard.

Unused signals should be left unconnected.

Signals can be optional used as GPIO.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J2	60	SDHC_CDn	PTA7	I	3.3V	Active low card detect
J2	62	SD CMD	PTA25	I/O	3.3V	Command/Response, onboard pull-up 100k
J2	64	SD CLK	PTA24	O	3.3V	
J2	66	SD DATA0	PTA26	I/O	3.3V	onboard pull-up 100k
J2	68	SD DATA1	PTA27	I/O	3.3V	
J2	70	SD DATA2	PTA28	I/O	3.3V	
J2	72	SD DATA3	PTA29	I/O	3.3V	

Table 5: SD Card Interface A

4.4 SPI

The module support HS SPI (Serial Peripheral Interface). All signals are 3.3V compliant. Devices on baseboard with other voltage need a level shifter.

Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	SM*1	MM*1	Voltage	Description
J1	29	SPI_A_SS0	PTB19	I	O	3.3V	
J1	26	SPI_A_MISO	PTB20	O	I	3.3V	
J1	27	SPI_A_MOSI	PTB21	I	O	3.3V	
J1	28	SPI_A_SCLK	PTB22	I	O	3.3V	

*1: SM: Slave Mode, MM: Master Mode

Table 6: SPI Interface

4.5 CAN

PicoCOMA5 provides up-to two CAN interfaces. One is compatible with the PicoCOM standard. The second shares pins with the I2C interface. The Vybrid SoC is used for the CAN function. PicoCOMA5 provide the CAN bus transmit and receive 3.3V TTL signal without any termination.

Needs a 3.3V transceiver like SN65HVD230 to the CAN bus.

Signals can be optional used as GPIO or I2C.Signals don't have pull-ups on module.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

	Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	30	CAN0_TX	PTB15	O	3.3V	
J1	31	CAN0_RX	PTB14	I	3.3V	
J1	32	CAN1_TX	PTB17	O	3.3V	
J1	33	CAN1_RX	PTB16	I	3.3V	

Table 7: CAN Interface

4.6 I2C

The module supports 2x I2C interfaces as I2C master.

Devices on baseboard with other voltage need a level shifter.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

Signals can be optional used as GPIO.

	Pin	Alternative Pin	Signal	CPU Pad	I/O	Voltage	Description
J1	30	53	I2C0_SDA	PTB15	I/O	3.3V	
J1	31	52	I2C0_SCL	PTB14	O	3.3V	
J1	32	58	I2C1_SDA	PTB17	I/O	3.3V	
J1	33	57	I2C1_SCL	PTB16	O	3.3V	

Table 8: I2C A and I2C B Interface

Note: I2C0 and I2C1 can only be used on one pair of pins at the same time (identical hardware block). There is no compatibility to other PicoCOM using this alternative function.

For all I2C Pins, there are no Pull-Ups on PicoCOM Module.

4.7 Serial ports

The module provides a maximum of three different serial ports with 3.3V TTL signals. These signals are not 5V compliant. Please use a transceiver with 3.3V power supply.

If you don't need the serial port this pins can be used optional as GPIOs.

	Pin	Signal	UART	CPU Pad	I/O	Voltage	Description
J1	14	UART0_RXD	SCI2	PTD1	I	3.3V	Reserved for debug, onboard Pull-Up 100k
J1	13	UART0_TXD	SCI2	PTD0	O	3.3V	Reserved for debug
J1	69	UART1_RTS	SCI1	PTB6	O	3.3V	
J1	11	UART1_CTS	SCI1	PTB7	I	3.3V	
J1	18	UART1_RXD	SCI1	PTB5	I	3.3V	onboard Pull-Up 100k
J1	17	UART1_TXD	SCI1	PTB4	O	3.3V	
J1	16	UART2_RXD	SCI3 (SCI2_CTS)	PTD3	I	3.3V	onboard Pull-Up 100k
J1	15	UART2_TXD	SCI1 (SCI2_RTS)	PTD2	O	3.3V	

Table 9: UART 0/1/2 Interface

UART	FIFO depth
SCI1	16-entry transmit and 16-entry receive
SCI2	8-entry transmit and 8-entry receive
SCI3	8-entry transmit and 8-entry receive

Table 10: UART FIFO depth

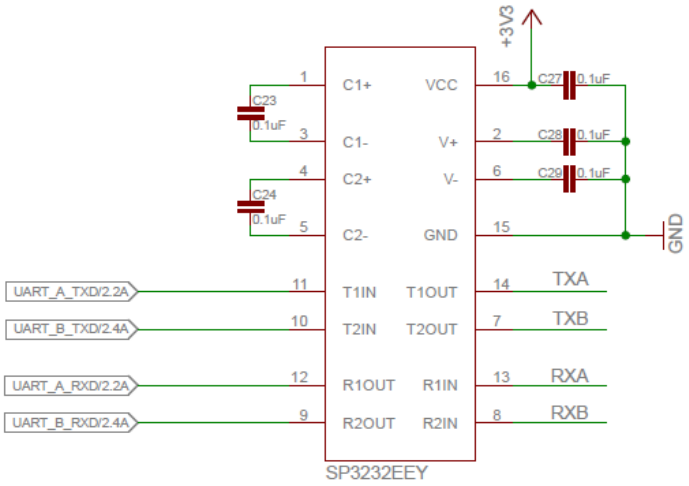

Figure 4: UART transceiver example

4.8 Ethernet0

PHY TI DP83848J is mounted on the module.

Ethernet TX+/- and LAN RX+/- are 100 ±20% Ohm differential pairs to a 1:1/1:1 transformer. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm).

The transformer midpoint should be connected to the 3.3V power supply.

LED signal is able to drive a 3.3V powered LED with 5mA directly to GND.

If Ethernet is not used please leave signals unconnected.

	Pin	Signal	Function	I/O	Voltage	Description
J1	1	LAN0_TX-	Ethernet 0 TX-	I/Odiff	-	1st PHY Differential data line
J1	2	LAN0_RX-	Ethernet 0 RX-	I/Odiff	-	
J1	3	LAN0_TX+	Ethernet 0 TX+	I/Odiff	-	1st PHY Differential data line
J1	4	LAN0_RX+	Ethernet 0 RX+	I/Odiff	-	
J1	70	ETHLED0	LINKLED	O	3.3V	1st PHY LINK LED, ON at LINK

Table 11: LAN A Interface

4.9 Ethernet1

Ethernet 1 is only a mounting option. It is only available if Audio is not used.

PHY TI DP83848J is mounted on the module.

Ethernet TX+/- and LAN RX+/- are 100 ±20% Ohm differential pairs to a 1:1/1:1 transformer. We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm).

The transformer midpoint should be connected to the 3.3V power supply.

LED signal is able to drive a 3.3V powered LED with 5mA directly to GND.

If Ethernet is not used please leave signals unconnected.

	Pin	Signal	Function	I/O	Voltage	Description
J1	1	LAN1_TX-	Ethernet 1 TX-	I/Odiff	-	2nd PHY Differential data line
J1	2	LAN1_RX-	Ethernet 1 RX-	I/Odiff	-	
J1	3	LAN1_TX+	Ethernet 1 TX+	I/Odiff	-	2nd PHY Differential data line
J1	4	LAN1_RX+	Ethernet 1 RX+	I/Odiff	-	
J1	70	ETHLED0	LINKLED	O	3.3V	2nd PHY LINK LED, ON at LINK

Table 12: LAN A Interface

4.10 Audio

The PicoCOMA5 module can support audio interface either directly via I2S signals or with an onboard audio codec IC. The audio codec NXP SGTL5000 can be mounted on the module optionally. In this case the module can also support only 1x Ethernet.

The onboard audio codec does support a stereo analog input and a stereo analog output for 1Vpp audio signals.

This signals needs serial capacitors.

ESD and EMV protection is required on baseboard.

For mounting option with I2S codec on baseboard please ask our technical support.

	Pin	Signal	I/O	Voltage	Description
J1	77	AUDIO_LOUT_L	O		Line Out Left / I2S LRCLK / Ethernet1 TX-
J1	78	AUDIO_LOUT_R	O		Line Out Right / I2S DOUT / Ethernet1 RX-
J1	79	AUDIO_LIN_L	I		Line In Left / I2S SYS MCLK / Ethernet1 TX+
J1	80	AUDIO_LIN_R	I		Line In Right / I2S SCLK / Ethernet1 RX+

Table 13: Audio Interface (with Codec)

	Pin	Signal	I/O	Voltage	Description
J1	69	I2S_DIN	I	3.3V	
J1	77	I2S LRCLK	O	3.3V	Line Out Left / I2S LRCLK / Ethernet1 TX-
J1	78	I2S DOUT	O	3.3V	Line Out Right / I2S DOUT / Ethernet1 RX-
J1	79	I2S SYS MCLK	O	3.3V	Line In Left / I2S SYS MCLK / Ethernet1 TX+
J1	80	I2S SCLK	O	3.3V	Line In Right / I2S SCLK / Ethernet1 RX+

Table 14: Audio I2S Interface (without Codec)

4.11 Digital RGB LCD Interface

All signals are working with 3.3V logic level.

	Pin	Signal	18 bit (without HSYNC/VSYNC)	18 bit (with HSYNC/VSYNC)	**15 bit**	16 bit
J1	43	LCD0	R1	R1	R0(LSB)	R0(LSB)
J1	44	LCD1	R2	R2	R1	R1
J1	45	LCD2	R3	R3	R2	R2
J1	46	LCD3	R4	R4	R3	R3
J1	47	LCD4	R5(MSK)	R5(MSB), R0(LSB)	R4(MSB)	R4(MSB)
J1	48	LCD5	G0(LSB)	G0(LSB)	G0(LSB)	---
J1	49	LCD6	G1	G1	G1	G0(LSB)
J1	50	LCD7	G2	G2	G2	G1
J1	51	LCD8	G3	G3	G3	G2
J1	52	LCD9	G4	G4	G4	G3
J1	53	LCD10	G5(MSB)	G5(MSB)	G5(MSB)	G4(MSB)
J1	54	LCD11	B1	B1	B0(LSB)	B0(LSB)
J1	55	LCD12	B2	B2	B1	B1
J1	56	LCD13	B3	B3	B2	B2
J1	57	LCD14	B4	B4	B3	B3
J1	58	LCD15	B5(MSB)	B5(MSB), B0(LSB)	B4(MSB)	B4(MSB)
J1	59	LCDCLK	DCLK			
J1	63	LCD16	B0(LSB)	HSYNC	HSYNC	HSYNC
J1	64	LCD17	R0(LSB)	VSYNC	VSYNC	VSYNC
J1	60	LCDDEN	DE	DE	DE	DE
J1	68	LCDENA	---	---	---	---
J1	65	LCDCC	PWM Backlight			
J1	66	LCDPOWn	LCD Power On (active low)			
J1	67	CFLPOWn	Backlight Power On (active low)			

Table 15: LCD Interface

Note: Most displays support HSYNC/VSYNC or DE mode. Please be sure just connect only useful signals at same time. The 18bit w/o HSYNC/VSYNC mode needs a special configuration made by software. Please refer the SW manual for this configuration.

4.12 Touch Interface

The integrated resistive touch controller will support 4 wire analog resistive touch panels without any additional circuit.

	Pin	Signal	I/O	Voltage	Description
J1	71	TSPX	I		Touch X+
J1	74	TSMX	I		Touch X-
J1	75	TSPY	I		Touch Y+
J1	76	TSMY	I		Touch Y-

Table 16: Touch Interface

4.13 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pull-ups or pull-downs are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on one of the GPIO contacts. Also a higher voltage as the announced IO power is not allowed.

4.14 Power and Power Control Contacts

	Pin	Signal	I/O	Description
J1	5,6	V33	PWR	Main Power supply input please refer chapter 0 Electrical characteristic
J1	7, 8	GND	PWR	Main Power supply Ground input
J1	9	VBAT	PWR	RTC battery input; tie to 3.0V please refer chapter 0 Electrical characteristic
J1	51	USB_OTG_VBUS	I	USB Phy voltage input; 5V
J1	10	nRES	I	Power on reset input; 10k PU; 1.8V* (3.3V on Rev. 1.00)

Table 17: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

RESETIN is a Reset Input for the module. Will just reset the CPU. Button or OC/OD output will restart the CPU. On power fail VIN has to be switched off and on to avoid latch up effects. We recommend to pull low this pin with a VCC voltage supervisor on power up with the powergood signal from power supply or using a voltage supervisor.

The GND contacts which are given in the table above are the power ground contacts for V33_VIN. For a better EMC performance it is highly recommended to connect all GND contacts to GND on the carrier board (not just the power ground contacts).

5 Flash

PicoCOMA5 can be shipped with SLC NAND Flash. By default NXP Vybrid are configured so that PicoCOMA5 boots from the assembled flash memory.

Please contact support for other boot options.

5.1 NAND Flash

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system

6 RTC

There is a NXP PCF8563TS/5 or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

7 Electrical characteristic

7.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IOs	-0.3	OVDD*+0.3	V
Voltage on any IO with V33_VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA

Table 18: Absolute Maximum Ratings

7.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
V33_VIN	Module main power		3.15	3.45	V
VBAT	RTC power		2.0	3.6	V
USB_DEVICE_VBUS	USB supply voltage		4.5	5.5	V
V_{ih}	High Level Input Voltage		0.7* V33_VIN	V33_VIN	V
V_{il}	Low Level Input Voltage		0	0.3* V33_VIN	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	V33_VIN -0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA
I_{VBAT}	Current consumption VBAT			0.25[*1]	µA
R_{DVR}	Output driver impedance	3.3V	[*2]	150	Ω

Table 19: DC Electrical Characteristics

[*1] Low current: typical 0.25 µA at VDD = 3.0 V and Tamb = 25 °C

[*2] Some IO pins are able to drive stronger by software configuration. Stronger driving does increase EMC radiation. Please refer software manual to increase or decrease impedance or ask our support.

8 Thermal Specification

Operating Ranges	Min	Typ.	Max	Unit
Consumer Range Environment Temperature	0		+70	°C
Industrial Range Environment Temperature	-25		+85	°C

Note 1: Maximum CPU junction is 105°C. Cooling is need in this case. See also: *Power consumption and cooling*

Note 2: Life expectancy of the CPU is shortened by high temperatures.

9 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

10 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

11 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

12 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **4 Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **1Watt** to **1.5Watt**. Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

13 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

14 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

15 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

16 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 5: Matrix Code Sticker

17 Appendix

Important Notice

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