Hardware Documentation

efus™A9 / efus™A9r2

Version 130
(2022-03-09)

Elektronik Systeme

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About This Document

This document describes how to use the efus™A9 and efus™A9r2 modules with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Important Note!

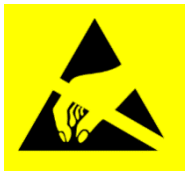
The latest PCB version for efusA9 is Version 1.21, for efusA9r2 is Version 1.00.

The only difference between these two modules is their Gbit Ethernet PHY's.

efus™A9 → Qualcomm Atheros AR8035

efus™A9r2 → Realtek RTL8211F/D

ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
12.03.14	001	All		-	Initial Version	DB
25.03.14	002	All			Mechanic, signal description	KW
25.04.14	003	All	M	3.1	Remove I2C_C from GPIO capability	KW
10.07.14	003	All	M	*	Changed to new company CI	JG
11.07.14	003	All	M	1	Changed block diagram design	JG
11.07.14	003	All	A	6, 6.2, 6.4	Add information for NAND, SPI-Flash and I2C-EEPROM	HF
15.07.14	004	All	A	6.5	LVDS EMC protection	HF
30.07.14	005	All	A	3.1 7.1	Add comment for CAM_MCLK Add common mode choke part number	KW KW
23.03.15	006	All	M	*	Some typos corrected	HF
13.07.15	007	All	M	8 3.1 4.10	Add TDP correct parallel camera signals (mounting option) add different camera pinouts and description	KW
05.08.15	008	All	M	3.1 **Error! Reference source not found.**	Correct USB_DEV_PWR_ON to low active signal by default CPU functionality	KW
07.10.15	009	All	M	3.1	Correct signal name pin 187	KW
08.10.15	010	All	M	5	Correct JAE connector order number	KW
08.01.16	011	All	M	**Error! Reference source not found.**	Correct signal description I2C_A	KW
04.03.16	100	All	A	6.1.1	Added note about data retention of SLC NAND flash	HF
04.03.16	100	All	A	6.2	Added information about eMMC flash memory.	HF
03.01.17	100	All	A	5, 8 5 9, 14, 0, 16	Add max. current for VLCD, add 5V feature Add missing I2C on LVDS connector Add Packaging, Matrix Code Sticker, ROHS and Reach Statement, Storing conditions	KW
26.03.18	110	All	M A	4, 4.6, 4.10 0, 9, 10, 11	Correct LAN LEDs, make camera If more clear Add RTC, Review service, ESC/ EMI, second source rules	KW
18.09.18	110	All	A	7	Extend thermal specification	JG
24.10.19	120	All	M	0	Add part of schematic to show internal connection of VBAT to RTC	HF
26.03.20	121	All	M	3.1	Correct signal name pin 154	MW
07.03.22	130	All	A,M	All	New F&S documentation template New Hardware efusA9r2 with an alternative Ethernet controller	MD

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

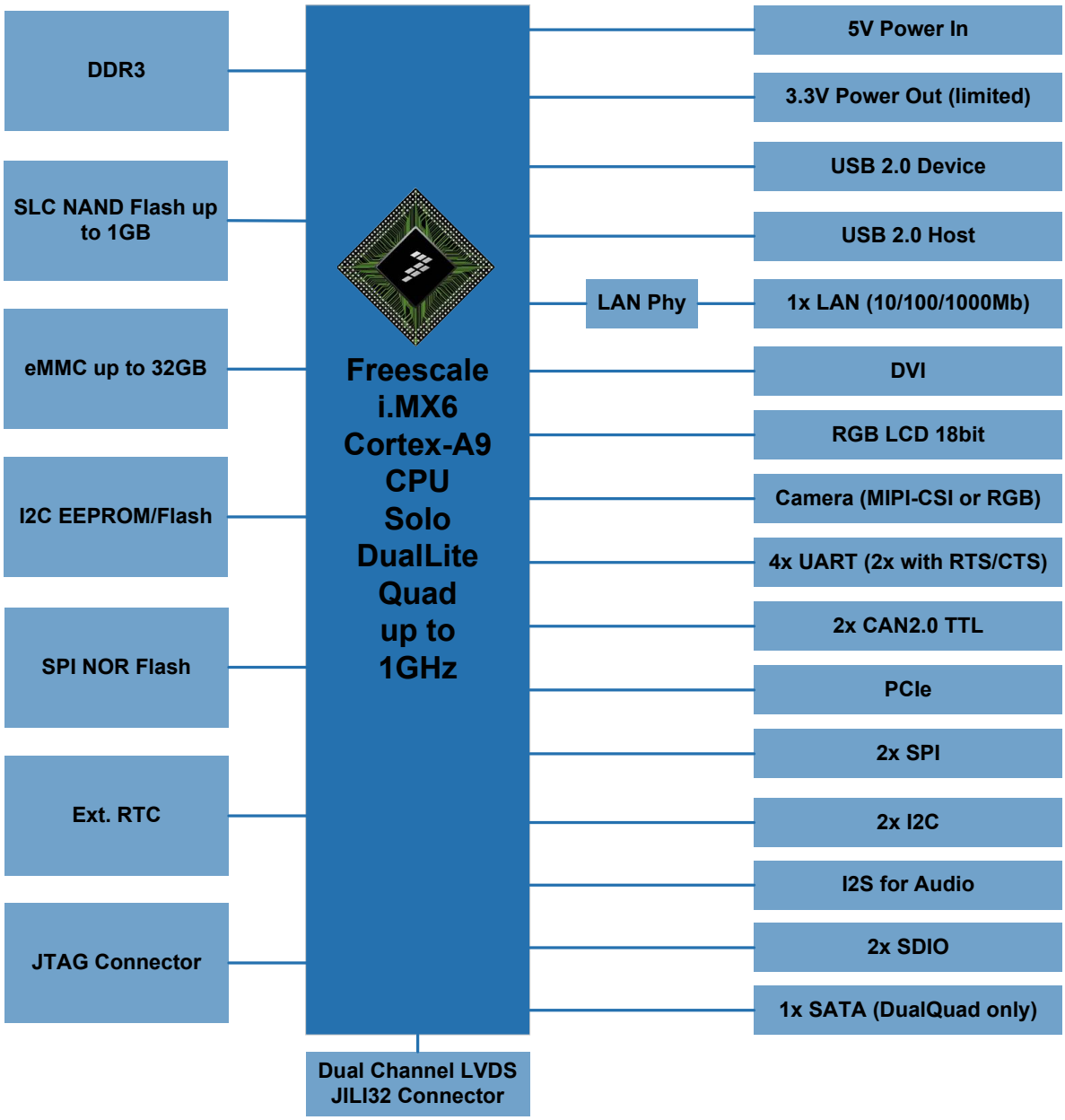


Figure 1: Block Diagram

2 Mechanical dimension

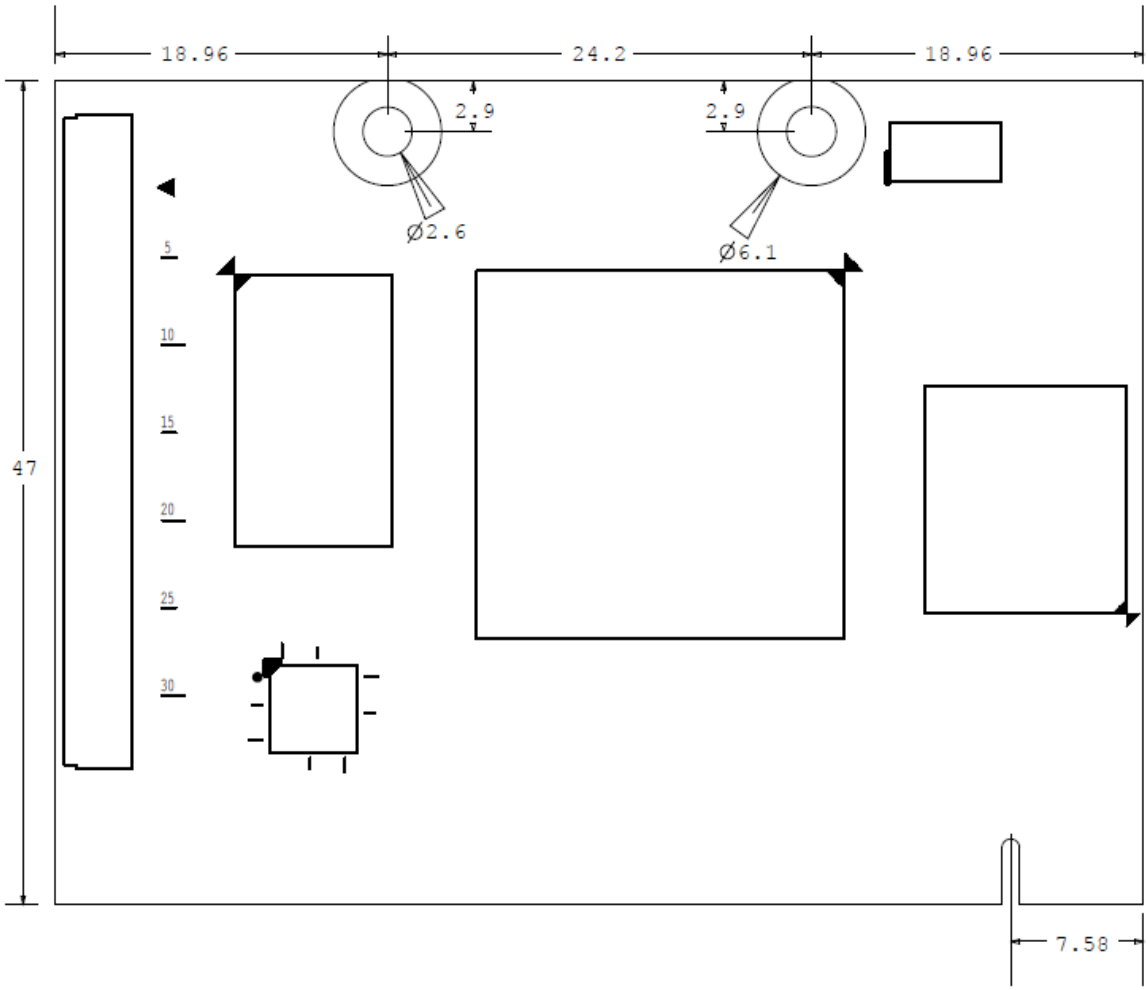


Figure 2: Mechanical Dimensions [mm]

Dimensions	Description
Size	62.1mm x 47mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	4.65mm
Height of the parts on the bottom side	0.9mm
Weight	14g

3 Interface and signal description

3.1 Goldfinger connector

See also efus start interface documentation for more information.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
1	+5V		PWR I	5.0V	Power Supply Input
2	+5V		PWR I	5.0V	Power Supply Input
3	+5V		PWR I	5.0V	Power Supply Input
4	+5V		PWR I	5.0V	Power Supply Input
5	+5V		PWR I	5.0V	Power Supply Input
6	+5V		PWR I	5.0V	Power Supply Input
7	GND		PWR	GND	
8	GND		PWR	GND	
9	VBAT		PWR I	3.0V	RTC Battery Input 2.2 < VBAT < 3.45V
10	V33OUT/V33-ENABLE		PWR O	3.3V	3.3V/100mA out, use as enable for main board 3.3V if more current is required
11	ACOK	USB_OTG_CHD_B	I	3.3V	USB OTG charge detect, future use
12	!RESET_IN		I	3.3V	100k Pull-up to 3.3V, drive with OC/OD*
13	I0OUT_ADC_IN	N.C.	X	X	Not connected
14	!RESET_OUT	ENET_RXD1	O	3.3V	4.7k pull-down to 3.3V, active low reset for baseboard logic
15	RXD_C_TTL	CSI_DAT11	I	3.3V	
16	SD_A_WP	DI0_PIN4	I	3.3V	4.7k pull up to 3.3V
17	TXD_C_TTL	CSI_DAT10	O	3.3V	
18	SD_A_CD	GPIO_1	I	3.3V	4.7k pull up to 3.3V
19	RTS_C_TTL	EIM_D19	O	3.3V	
20	SD_A_DAT2	SD1_DAT2	I/O	3.3V	
21	CTS_C_TTL	EIM_D20	I	3.3V	
22	SD_A_DAT3	SD1_DAT3	I/O	3.3V	
23	NC		X	X	No Connection
24	SD_A_CMD	SD1_CMD	O	3.3V	10k pull up to 3.3V

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
25	PWMA	SD4_DAT2	O	3.3V	
26	SD_A_VCC	SD1_VCC	PWR O	3.3V	3.3V out for SD-Card A
27	GND		PWR	GND	
28	SD_A_CLK	SD1_CLK	O	3.3V	
29	CAN_A_TX	KEY_COL4	O	3.3V	
30	GND		PWR	GND	
31	CAN_A_RX	KEY_ROW4	I	3.3V	
32	SD_A_DAT0	SD1_DAT0	I/O	3.3V	
33	GND		PWR	GND	
34	SD_A_DAT1	SD1_DAT1	I/O	3.3V	
35	CAN_B_TX	KEY_COL2	O	3.3V	
36	N.C.		X	X	Not connected
37	CAN_B_RX	KEY_ROW2	I	3.3V	
38	N.C.		X	X	Not connected
39	GND		PWR	GND	
40	N.C.		X	X	Not connected
41	MPCIE_CTX_P	PCIE_TXP	O	1.2V/2.5V	
42	N.C.		X	X	Not connected
43	MPCIE_CTX_N	PCIE_TXM	O	1.2V/2.5V	
44	N.C.		X	X	Not connected
45	GND		PWR	GND	
46	GND		PWR	GND	
47	MPCIE_CRX_P	PCIE_RXP	I	1.2V/2.5V	
48	EXT_PROG	BOOT_MODE0	I	3.3V	Boot select
49	MPCIE_CRX_N	PCIE_RXM	I	1.2V/2.5V	
50	SPI_B_MISO	EIM_D17	I	3.3V	
51	GND		PWR	GND	
52	SPI_B_MOSI	EIM_D18	O	3.3V	
53	MPCIE_CLK_P	CLK1_P	O	1.2V/2.5V	
54	SPI_B_SPCK	EIM_D16	O	3.3V	
55	MPCIE_CLK_N	CLK1_N	O	1.2V/2.5V	
56	SPI_B_CS1	EIM_D24	O	3.3V	
57	GND		PWR	GND	

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
58	SPI_B_CS2	EIM_D25	O	3.3V	
59	MPCIE_PERST	NANDF_CS1	O	3.3V	
60	SPI_B_IRQ1	GPIO_5	I/O	3.3V	100k pull up to 3.3V
61	MPCIE_WAKE	NANDF_CS3	I	3.3V	
62	SPI_B_IRQ2	GPIO_6	I/O	3.3V	100k pull up to 3.3V
63	GND		PWR	GND	
64	GND		PWR	GND	
65	SD_B_DAT2	SD2_DAT2	I/O	3.3V	
66	SPI_A_MISO	EIM_OE	I	3.3V	
67	SD_B_DAT3	SD2_DAT3	I/O	3.3V	
68	SPI_A_MOSI	EIM_CS1	O	3.3V	
69	SD_B_CMD	SD2_CMD	O	3.3V	10k pull up to 3.3V
70	SPI_A_SPCK	EIM_CS0	O	3.3V	
71	SD_B_VCC	SD2_VCC	PWR O	3.3V	3.3V out for SD-Card B
72	SPI_A_CS1	EIM_SS0	O	3.3V	
73	SD_B_CLK	SD2_CLK	O	3.3V	
74	SPI_A_CS2	EIM_LBA	O	3.3V	
75	GND		PWR	GND	
76	SPI_A_IRQ1	GPIO_7	I/O	3.3V	100k pull up to 3.3V
77	SD_B_DAT0	SD2_DAT0	I/O	3.3V	
78	SPI_A_IRQ2	GPIO_8	I/O	3.3V	100k pull up to 3.3V
79	SD_B_DAT1	SD2_DAT1	I/O	3.3V	
80	GND		PWR	GND	
81	SD_B_WP	GPIO_2	I	3.3V	4.7k pull up to 3.3V
82	I2C_B_DAT	GPIO_16	I/O	3.3V	4.7k pull up to 3.3V
83	SD_B_CD	GPIO_4	I	3.3V	4.7k pull up to 3.3V
84	I2C_B_CLK	GPIO_3	I	3.3V	4.7k pull up to 3.3V
85	GND		PWR	GND	
86	I2C_B_IRQ	SD4_DAT4	O	3.3V	100k pull up to 3.3V
87	BL_CTRL	SD4_DAT1	O	3.3V	PWM Backlight dimming
88	I2C_B_RST	SD4_DAT5	O	3.3V	100k pull up to 3.3V
89	VCFL_ON	SD4_DAT0	O	3.3V	4.7k pull down, Backlight enable
90	GND		PWR	GND	

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
91	GND		PWR	GND	
92	RXD_A_TTL	KEY_ROW0	I	3.3V	Debug, 100k pull up to 3.3V
93	LCD_CLK	DI0_DISP_CLK	O	3.3V	
94	TXD_A_TTL	KEY_COL0	O	3.3V	Debug
95	GND		PWR	GND	
96	RXD_D_TTL	KEY_ROW1	I	3.3V	
97	LCD_HSYNC	DI0_PIN2	O	3.3V	
98	TXD_D_TTL	KEY_COL1	O	3.3V	
99	LCD_VSYNC	DI0_PIN3	O	3.3V	
100	GND		PWR	GND	
101	GND		PWR	GND	
102	RXD_B_TTL	EIM_D27	I	3.3V	
103	LCD_R0	DISP0_DATA0	O	3.3V	
104	TXD_B_TTL	EIM_D26	O	3.3V	
105	LCD_R1	DISP0_DATA1	O	3.3V	
106	RTS_B_TTL	EIM_D28	O	3.3V	
107	LCD_R2	DISP0_DATA2	O	3.3V	
108	CTS_B_TTL	EIM_D29	I	3.3V	
109	LCD_R3	DISP0_DATA3	O	3.3V	
110	GND		PWR	GND	
111	LCD_R4	DISP0_DATA4	O	3.3V	
112	I2S_MCLK	GPIO_0	O	3.3V	
113	LCD_R5	DISP0_DATA5	O	3.3V	
114	GND		PWR	GND	
115	GND		PWR	GND	
116	I2S_LRCLK	DISP0_DAT22	O	3.3V	
117	LCD_G0	DISP0_DATA6	O	3.3V	
118	GND		PWR	GND	
119	LCD_G1	DISP0_DATA7	O	3.3V	
120	I2S_SCLK	DISP0_DAT20	O	3.3V	
121	LCD_G2	DISP0_DATA8	O	3.3V	
122	GND		PWR	GND	
123	LCD_G3	DISP0_DATA9	O	3.3V	

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
124	I2S_DOUT	DISP0_DAT23	I	3.3V	
125	LCD_G4	DISP0_DATA10	O	3.3V	
126	I2S_DIN	DISP0_DAT21	O	3.3V	
127	LCD_G5	DISP0_DATA11	O	3.3V	
128	GND		PWR	GND	
129	GND		PWR	GND	
130	I2C_C_DAT	CSI0_DAT8	I/O	3.3V	4.7k pull up to 3.3V
131	LCD_B0	DISP0_DATA12	O	3.3V	
132	I2C_C_CLK	CSI0_DAT9	I/O	3.3V	4.7k pull up to 3.3V
133	LCD_B1	DISP0_DATA13	O	3.3V	
134	DVI_DDC_VOUT	-	O	3.3V	3.3V output for ESD protection
135	LCD_B2	DISP0_DATA14	O	3.3V	
136	GND		PWR	GND	
137	LCD_B3	DISP0_DATA15	O	3.3V	
138	DVI_DATA2_P	HDMI_D2P	O	1.2V/2.5V	
139	LCD_B4	DISP0_DATA16	O	3.3V	
140	DVI_DATA2_N	HDMI_D2M	O	1.2V/2.5V	
141	LCD_B5	DISP0_DATA17	O	3.3V	
142	DVI_DATA1_P	HDMI_D1P	O	1.2V/2.5V	
143	GND		PWR	GND	
144	DVI_DATA1_N	HDMI_D1M	O	1.2V/2.5V	
145	LCD_DE	DI0_PIN15	O	3.3V	
146	DVI_DATA0_P	HDMI_D0P	O	1.2V/2.5V	
147	GND		PWR	GND	
148	DVI_DATA0_N	HDMI_D0M	O	1.2V/2.5V	
149	VLCD_ON	SD4_DAT3	O	3.3V	4.7k pull down
150	DVI_CLK_P	HDMI_CLKP	O	1.2V/2.5V	
151	I2C_A_DAT	KEY_ROW3	I/O	3.3V	4.7k pull up to 3.3V
152	DVI_CLK_N	HDMI_CLKM	O	1.2V/2.5V	
153	I2C_A_IRQ	ENET_TXD0	I	3.3V	100k pull up to 3.3V
154	LVDS/DSI _DATA3_P				
155	I2C_A_CLK	KEY_COL3	O	3.3V	4.7k pull up to 3.3V
156	DVI_DDCCEC	EIM_A25	I/O	3.3V	

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
157	I2C_A_RST	ENET_TXD1	O	3.3V	100k pull up to 3.3V
158	DVI_HPD	HDMI_HPD	I	1.2V/2.5V	
159	GND		PWR	GND	
160	GND		PWR	GND	
161	CAMINT_YDATA0/D0_N	CSI0_DAT10/ CSI_D0M	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
162	ETH_B_D4-	N.C.	X	X	Not connected
163	CAMINT_YDATA1/D0_P	CSI0_DAT11/ CSI_D0P	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
164	ETH_B_D4+	N.C.	X	X	Not connected
165	CAMINT_YDATA4/D1_N	CSI0_DAT12/ CSI_D1M	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
166	ETH_B_LED_ACT	N.C.	X	X	Not connected
167	CAMINT_YDATA3/D1_P	CSI0_DAT13/ CSI_D1P	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
168	ETH_B_D3-	N.C.	X	X	Not connected
169	CAMINT_YDATA5/D2_N	CSI0_DAT14/ CSI_D2M	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
170	ETH_B_D3+	N.C.	X	X	Not connected
171	CAMINT_YDATA2/D2_P	CSI0_DAT15/ CSI_D2P	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
172	GND		PWR	GND	
173	CAMINT_YDATA6/D3_N	CSI0_DAT16/ CSI_D3M	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
174	ETH_B_D2-	N.C.	X	X	Not connected
175	CAMINT_PCLK/D3_P	CSI0_PIXCLK/ CSI_D3P	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
176	ETH_B_D2+	N.C.	X	X	Not connected
177	CAMINT_YDATA7/CLK_N	CSI0_DAT17/ CSI_CLK0M	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
178	ETH_B_LED_LINK	N.C.	X	X	Not connected
179	CAMINT_YDATA8/CLK_P	CSI0_DAT18/ CSI_CLK0P	I	2.8V/2.5V	Parallel Camera / MIPI-CSI
180	ETH_B_D1-	N.C.	X	X	Not connected
181	GND		PWR	GND	
182	ETH_B_D1+	N.C.	X	X	Not connected
183	CAMINT_MCLK	NANDF_CS2	O	3.3V	Parallel and MIPI CSI mounting option Same signal source as I2S_MCLK; we recommend oscillator on baseboard as MCLK source for camera
184	GND		PWR	GND	
185	GND		PWR	GND	
186	ETH_CTREF	N.C.	X	X	Not connected

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
187	CAMINT_YDATA9	CSI0_DAT19	I	2.8V	Parallel Camera option
188	ETH_A_D4_N	-	I/O	1.8V	
189	CAMINT_VCAM	-	PWR O	2.8V/3.3V	2.8V for parallel camera 3.3V for MIPI-CSI option
190	ETH_A_D4_P	-	I/O	1.8V	
191	CAMINT_HREF	CSI0_MCLK	I	2.8V	Parallel Camera option
192	ETH_A_LED_ACT	-	O	3.3V	
193	CAMINT_PWDN	CSI0_DAT6	O	2.8V	Parallel Camera option
194	ETH_A_D3_N	-	I/O	1.8V	
195	CAMINT_VSYNC	CSI0_VSYNC	I	2.8V	Parallel Camera option
196	ETH_A_D3_P	-	I/O	1.8V	
197	I2C_C_CAMRST	CSI0_DAT5	O	2.8V	
198	ETH_A_VLEDOUT	-	PWR O	3.3V	
199	GND		PWR	GND	
200	ETH_A_D2_N	-	I/O	1.8V	
201	SATA_RX_P	SATA_RXP	I	1.2V/2.5V	
202	ETH_A_D2_P	-	I/O	1.8V	
203	SATA_RX_N	SATA_RXM	I	1.2V/2.5V	
204	ETH_A_LED_LINK	-	O	3.3V	
205	SATA_TX_N	SATA_TXM	O	1.2V/2.5V	
206	ETH_A_D1_N	-	I/O	1.8V	
207	SATA_TX_P	SATA_TXP	O	1.2V/2.5V	
208	ETH_A_D1_P	-	I/O	1.8V	
209	GND		PWR	GND	
210	GND		PWR	GND	
211	CAM_A_IN	N.C.	X	X	Not connected
212	USB_PWRON	EIM_D31	I	3.3V	
213	CAM_A_GND	N.C.	X	X	Not connected
214	USB_A_N	USB_H1_DN	I/O	3.3V	
215	GND		PWR	GND	
216	USB_A_P	USB_H1_DP	I/O	3.3V	
217	USB_DEV_VBUS	USB_OTG_VBUS	O	5V	4.6 … 5.2V does detect conected USB device
218	GND		PWR	GND	

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Remarks
219	USB_DEV_PWR_ONn	EIM_D22	I/O	3.3V	
220	USB_A_SSRX_N	N.C.	X	X	Not connected
221	USB_DEV_OC	EIM_D21	I	3.3V	
222	USB_A_SSRX_P	N.C.	X	X	Not connected
223	USB_DEV_ID	ENET_RX_ER	I	3.3V	100k pull up to 3.3V
224	GND		PWR	GND	
225	USB_DEV_N	USB_OTG_DN	I/O	3.3V	
226	USB_A_SSTX_N	N.C.	X	X	Not connected
227	USB_DEV_P	USB_OTG_DP	I/O	3.3V	
228	USB_A_SSTX_P	N.C.	X	X	Not connected
229	GND		PWR	GND	
230	GND		PWR	GND	
231	MOUNTINGHOLE_1	N.C.	X	X	Mounting holes
232	MOUNTINGHOLE_2	N.C.	X	X	Mounting holes

Table 1: Goldfinger Pinout

4 Interfaces

4.1 USB Interface (Host & Device)

efus™A9 and efus™A9r2 modules provide 1x USB2.0 Host only and 1x USBOTG2.0 connections.

The 90 Ohm differential pair of USB signals do not need any termination. For external ports EMV and ESD protection is required nearby the USB connector on the base board. If the USB port is not used please leave open.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
212	USB_PWRON	EIM_D31		3.3V	High active USB port power on signal
214	USB_A_N	USB_H1_DN	I/O	3.3V	Differential USB Signals – 90Ohm
216	USB_A_P	USB_H1_DP	I/O	3.3V	
217	USB_DEV_VBUS	USB_OTG_VBUS	O	5V	4.6 … 5.2V does detect connected USB device Connect with pin 1 on USB device connector
219	USB_DEV_PWR_ONn	EIM_D22	I/O	3.3V	Low active USB port power on signal
221	USB_DEV_OC	EIM_D21	I	3.3V	Overcurrent Input signal
223	USB_DEV_ID	ENET_RX_ER	I	3.3V	Used in OTG mode only 100k pull-up to 3.3V
225	USB_DEV_N	USB_OTG_DN	I/O	3.3V	Differential USB Signals – 90Ohm
227	USB_DEV_P	USB_OTG_DP	I/O	3.3V	

Table 2: USB Interface –Host & Device

4.2 HDMI & DVI

The module allows connecting a single channel DVI monitor without any transmitter chip. The signals should be routed with 100 ohm ±15% differential lines. The length difference between a differential pair should be limited to 5 mils maximum. Each pair should be length-matched to within ± 20 mils of any other signal pair.

If interface is not used, please leave unconnected.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
130	I2C_C_DAT	CSI0_DAT8	I/O	3.3V	DDC DAT input Shared with internal peripherals
132	I2C_C_CLK	CSI0_DAT9	I	3.3V	DDC CLK input Shared with internal peripherals
134	DVI_DDC_VOUT	-	O	3.3V	3.3V output for ESD protection device
138	DVI_DATA2_P	HDMI_D2P	O	1.2V/2.5V	DVI Data Lane2+
140	DVI_DATA2_N	HDMI_D2M	O	1.2V/2.5V	DVI Data Lane2-
142	DVI_DATA1_P	HDMI_D1P	O	1.2V/2.5V	DVI Data Lane1+
144	DVI_DATA1_N	HDMI_D1M	O	1.2V/2.5V	DVI Data Lane1-
146	DVI_DATA0_P	HDMI_D0P	O	1.2V/2.5V	DVI Data Lane0+
148	DVI_DATA0_N	HDMI_D0M	O	1.2V/2.5V	DVI Data Lane0-
150	DVI_CLK_P	HDMI_CLKP	O	1.2V/2.5V	DVI Clock Lane+
152	DVI_CLK_N	HDMI_CLKM	O	1.2V/2.5V	DVI Clock Lane-
156	DVI_DDCCEC	EIM_A25	I/O	3.3V	CEC signal
158	DVI_HPD	HDMI_HPD	I	1.2V/2.5V	Hotplug detect input; 3.3V tolerant 47k pull up to 3.3V

Table 3: HDMI&DVI Interface

4.3 SD/MMC card

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

Unused signals should be left unconnected.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
16	SD_A_WP	DI0_PIN4	I	3.3V	SD card A write protect input 4.7k pull up to 3.3V
18	SD_A_CD	GPIO_1	I	3.3V	SD card A card low active detect input 4.7k pull up to 3.3V
20	SD_A_DAT2	SD1_DAT2	I/O	3.3V	SD card A data signal
22	SD_A_DAT3	SD1_DAT3	I/O	3.3V	SD card A data signal
24	SD_A_CMD	SD1_CMD	O	3.3V	SD card A command signal
26	SD_A_VCC	SD1_VCC	PWR O	3.3V	SD card A power out
28	SD_A_CLK	SD1_CLK	O	3.3V	SD card A clock signal
32	SD_A_DAT0	SD1_DAT0	I/O	3.3V	SD card A data signal
34	SD_A_DAT1	SD1_DAT1	I/O	3.3V	SD card A data signal
81	SD_B_WP	GPIO_2	I	3.3V	SD card B write protect input 4.7k pull up to 3.3V
83	SD_B_CD	GPIO_4	I	3.3V	SD card B card low active detect input 4.7k pull up to 3.3V
65	SD_B_DAT2	SD2_DAT2	I/O	3.3V	SD card B data signal
67	SD_B_DAT3	SD2_DAT3	I/O	3.3V	SD card B data signal
69	SD_B_CMD	SD2_CMD	O	3.3V	SD card B command signal
71	SD_B_VCC	SD2_VCC	PWR O	3.3V	SD card B power out
73	SD_B_CLK	SD2_CLK	O	3.3V	SD card B clock signal
77	SD_B_DAT0	SD2_DAT0	I/O	3.3V	SD card B data signal
79	SD_B_DAT1	SD2_DAT1	I/O	3.3V	SD card B data signal

Table 4: SD/MMC Card

4.4 Serial Interfaces

On efus™A9 and efus™A9r2 boards it is allowed for the users to use these serial interfaces, which are given below. All of these serial Interfaces are 3.3V compliant.

UART: 2 x UART with RTS/CTS and 2 x UART without RTS/CTS

I2C: 3 x I2C

SPI: 2 x SPI

CAN: 2 x CAN (no termination needed, TTL Level) – an external transceiver is needed for the CAN FD interface.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
UART_A (UART4)*[1]					
92	RXD_A_TTL	KEY_ROW0	I	3.3V	Data receive, Debug interface, 100k pull-up
94	TXD_A_TTL	KEY_COL0	O	3.3V	Data transmit, Debug interface
UART_B (UART2)					
102	RXD_B_TTL	EIM_D27	I	3.3V	Data receive; no pull up on board
104	TXD_B_TTL	EIM_D26	O	3.3V	Data transmit
106	RTS_B_TTL	EIM_D28	O	3.3V	Request to send
108	CTS_B_TTL	EIM_D29	I	3.3V	Clear to send
UART_C (UART1)					
15	RXD_C_TTL*[2]	CSI_DAT11	I	3.3V	Data receive; no pull up on board
17	TXD_C_TTL*[2]	CSI_DAT10	O	3.3V	Data transmit
19	RTS_C_TTL	EIM_D19	O	3.3V	Request to send
21	CTS_C_TTL	EIM_D20	I	3.3V	Clear to send
UART_D (UART5)					
96	RXD_D_TTL	KEY_ROW1	I	3.3V	Data receive; no pull up on board
98	TXD_D_TTL	KEY_COL1	O	3.3V	Data transmit

*[1] It is recommended to use UART_A for debugging and service only.
*[2] Optional with parallel camera interface, cannot be used at the same time

Table 5: Serial Interfaces – UART

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
I2C_A*[1] (I2C2)					

151	I2C_A_DAT	KEY_ROW3	I/O	3.3V	Data signal; 4.7k pull up to 3.3V
153	I2C_A_IRQ	ENET_TXD0	I	3.3V	Interrupt input; 100k pull up to 3.3V
155	I2C_A_CLK	KEY_COL3	O	3.3V	Clock signal; 4.7k pull up to 3.3V
157	I2C_A_RST	ENET_TXD1	O	3.3V	Reset output; 100k pull up to 3.3V
I2C_B (I2C3)					
82	I2C_B_DAT	GPIO_16	I/O	3.3V	Data signal; 4.7k pull up to 3.3V
84	I2C_B_CLK	GPIO_3	I	3.3V	Clock signal; 4.7k pull up to 3.3V
86	I2C_B_IRQ	SD4_DAT4	O	3.3V	Interrupt input; 100k pull up to 3.3V
88	I2C_B_RST	SD4_DAT5	O	3.3V	Reset output; 100k pull up to 3.3V
I2C_C*[2] (I2C1)					
130	I2C_C_DAT	CSI0_DAT8	I/O	3.3V	Data signal; 10k pull up to 3.3V
132	I2C_C_CLK	CSI0_DAT9	O	3.3V	Clock signal; 10k pull up to 3.3V

*[1] I2C_A is reserved for display and touch controller
*[2] I2C_C is reserved for DVI DDC, sound codec programming, mPCIe SMB and camera programming, the port is also shared with RTC and EEPROM on module. It is not recommended to use for other functions

Table 6: Serial Interfaces – I2C

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
SPI_A (ECSPI2)					
66	SPI_A_MISO	EIM_OE	I	3.3V	SPI0 Master In Slave Out (Data In)
68	SPI_A_MOSI	EIM_CS1	O	3.3V	SPI0 Master Out Slave In (Data Out)
70	SPI_A_SPCK	EIM_CS0	O	3.3V	SPI0 Serial Peripheral Clock
72	SPI_A_CS1	EIM_SS0	O	3.3V	SPI0 Chip Select 1 (Slave Select 0)
74	SPI_A_CS2	EIM_LBA	O	3.3V	SPI0 Chip Select 2 (Slave Select 1)
76	SPI_A_IRQ1	GPIO_7	I/O	3.3V	SPI0 Interrupt Flag 1 ;100k pull up to 3.3V
78	SPI_A_IRQ2	GPIO_8	I/O	3.3V	SPI0 Interrupt Flag 2; 100k pull up to 3.3V
SPI_B (ECSPI1)					
50	SPI_B_MISO	EIM_D17	I	3.3V	SPI3 Master In Slave Out (Data In)
52	SPI_B_MOSI	EIM_D18	O	3.3V	SPI3 Master Out Slave In (Data Out)
54	SPI_B_SPCK	EIM_D16	O	3.3V	SPI3 Serial Peripheral Clock
56	SPI_B_CS1	EIM_D24	O	3.3V	SPI3 Chip Select 1 (Slave Select 0)
58	SPI_B_CS2	EIM_D25	O	3.3V	SPI3 Chip Select 2 (Slave Select 1)
60	SPI_B_IRQ1	GPIO_5	I/O	3.3V	SPI3 Interrupt Flag 1; 100k pull up to 3.3V
62	SPI_B_IRQ2	GPIO_6	I/O	3.3V	SPI3 Interrupt Flag 2; 100k pull up to 3.3V

Table 7: Serial Interfaces – SPI

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
CAN_A (CAN1)					
29	CAN_A_TX	KEY_COL4	O	3.3V	CAN port A TX out
31	CAN_A_RX	KEY_ROW4	I	3.3V	CAN port A RX in
CAN_B (CAN2)					
35	CAN_B_TX	KEY_COL2	O	3.3V	CAN port B TX out
37	CAN_B_RX	KEY_ROW2	I	3.3V	CAN port B RX in

Table 8: Serial Interfaces – CAN

4.5 Digital Audio Interface (I2S)

The module supports an external I2S audio codec.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
112	I2S_MCLK	GPIO_0	O	3.3V	I2S master clock for external codec (I2S_MCLK on CPU)
116	I2S_LRCLK	DISP0_DAT22	O	3.3V	I2S frame clock for external codec (I2S_TXFS on CPU)
120	I2S_SCLK	DISP0_DAT20	O	3.3V	I2S bit clock for external codec (I2S_TXC on CPU)
124	I2S_DOUT	DISP0_DAT23	I	3.3V	I2S data output for external codec (I2S_RXD on CPU)
126	I2S_DIN	DISP0_DAT21	O	3.3V	I2S data input for external codec (I2S_TXD on CPU)
130	I2C_C_DAT*[1]	CSI0_DAT8	I/O	3.3V	I2C Serial Data control signal (shared)
132	I2C_C_CLK*[1]	CSI0_DAT9	O	3.3V	I2C Serial Clock control signal (shared)

*[1] I2C_C can be used for the external audio codec

Table 9: Digital Audio Interface (I2S) Pinout

4.6 Ethernet

The module supports a single 10/100/1000 Mbit LAN interface.

efus™A9 → Qualcomm Atheros AR8035 Gbit Ethernet PHY

efus™A9r2 → Realtek RTL8211F/D Gbit Ethernet PHY

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
186	ETH_CTREF	N.C.	X	X	Not Connected
188	ETH_A_D4_N		I/O	1.8V	Ethernet A Data Lane4-
190	ETH_A_D4_P		I/O	1.8V	Ethernet A Data Lane4+
192	ETH_A_LED_ACT		O	3.3V	ACT LED cathode output, serial R needed
194	ETH_A_D3_N		I/O	1.8V	Ethernet A Data Lane3-
196	ETH_A_D3_P		I/O	1.8V	Ethernet A Data Lane3+
198	ETH_A_VLEDOUT		PWR O	3.3V	3.3V out for LAN LEDs anode
200	ETH_A_D2_N		I/O	1.8V	Ethernet A Data Lane2-
202	ETH_A_D2_P		I/O	1.8V	Ethernet A Data Lane2+
204	ETH_A_LED_LINK		O	3.3V	LINK LED cathode output, serial R needed
206	ETH_A_D1_N		I/O	1.8V	Ethernet A Data Lane1-
208	ETH_A_D1_P		I/O	1.8V	Ethernet A Data Lane1+

Table 10: Ethernet Pinout

4.7 PCIe

A single lane PCI Express port (Gen 2.0) is supported.

Please following design rules from PCI-SIG on your design.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
41	MPCIE_CTX_P	PCIE_TXP	O	1.2V/2.5V	PCIe Data Transmit+
43	MPCIE_CTX_N	PCIE_TXM	O	1.2V/2.5V	PCIe Data Transmit-
47	MPCIE_CRX_P	PCIE_RXP	I	1.2V/2.5V	PCIe Data Receive+
49	MPCIE_CRX_N	PCIE_RXM	I	1.2V/2.5V	PCIe Data Receive-
53	MPCIE_CLK_P	CLK1_P	O	1.2V/2.5V	PCIe Clock+
55	MPCIE_CLK_N	CLK1_N	O	1.2V/2.5V	PCIe Clock-
59	MPCIE_PERST	NANDF_CS1	O	3.3V	PCIe reset output
61	MPCIE_WAKE	NANDF_CS3	I	3.3V	PCIe wake input

Table 11: PCIe Pinout

4.8 SATA

A single SATA device can be connected on the SATA interface. Leave signals unconnected if not used.

SATA interface is not available on modules that based on i.MX6 Solo and i.MX6 Dual Lite.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
201	SATA_RX_P	SATA_RXP	I	1.2V/2.5V	SATA Data Receive+
203	SATA_RX_N	SATA_RXM	I	1.2V/2.5V	SATA Data Receive-
205	SATA_TX_N	SATA_TXM	O	1.2V/2.5V	SATA Data Transmit+
207	SATA_TX_P	SATA_TXP	O	1.2V/2.5V	SATA Data Transmit-

Table 12: SATA Pinout

4.9 RGB LCD

Since the high speed RGB signals have 3.3V TTL voltage level, high EMI radiation might be generated. Signals must be routed as short as possible and a shielding is highly recommended in order to prevent potential EMC problems.

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
87	BL_CTRL	SD4_DAT1	O	3.3V	3.3V TTL PWM output for Backlight dimming
89	VCFL_ON	SD4_DAT0	O	3.3V	4.7k pull down, high active Backlight on
93	LCD_CLK	DI0_DISP_CLK	O	3.3V	RGB LCD clock
97	LCD_HSYNC	DI0_PIN2	O	3.3V	RGB LCD HSYNC
99	LCD_VSYNC	DI0_PIN3	O	3.3V	RGB LCD VSYNC
103	LCD_R0	DISP0_DATA0	O	3.3V	Red0
105	LCD_R1	DISP0_DATA1	O	3.3V	Red1
107	LCD_R2	DISP0_DATA2	O	3.3V	Red2
109	LCD_R3	DISP0_DATA3	O	3.3V	Red3
111	LCD_R4	DISP0_DATA4	O	3.3V	Red4
113	LCD_R5	DISP0_DATA5	O	3.3V	Red5
117	LCD_G0	DISP0_DATA6	O	3.3V	Green0
119	LCD_G1	DISP0_DATA7	O	3.3V	Green1
121	LCD_G2	DISP0_DATA8	O	3.3V	Green2
123	LCD_G3	DISP0_DATA9	O	3.3V	Green3
125	LCD_G4	DISP0_DATA10	O	3.3V	Green4
127	LCD_G5	DISP0_DATA11	O	3.3V	Green5
131	LCD_B0	DISP0_DATA12	O	3.3V	Blue0
133	LCD_B1	DISP0_DATA13	O	3.3V	Blue1
135	LCD_B2	DISP0_DATA14	O	3.3V	Blue2
137	LCD_B3	DISP0_DATA15	O	3.3V	Blue3
139	LCD_B4	DISP0_DATA16	O	3.3V	Blue4
141	LCD_B5	DISP0_DATA17	O	3.3V	Blue5
145	LCD_DE	DI0_PIN15	O	3.3V	Data enable
149	VLCD_ON	SD4_DAT3	O	3.3V	4.7k pull down, high active LCD power on

Table 13: RGB LCD Pinout

4.10 Camera

CSI Camera (default mounting option on most standard variants)

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
161	D0_N	CSI_D0M	I	2.5V	MIPI CSI Data0-
163	D0_P	CSI_D0P	I	2.5V	MIPI CSI Data0+
165	D1_N	CSI_D1M	I	2.5V	MIPI CSI Data1-
167	D1_P	CSI_D1P	I	2.5V	MIPI CSI Data1+
169	D2_N	CSI_D2M	I	2.5V	MIPI CSI Data2-
171	D2_P	CSI_D2P	I	2.5V	MIPI CSI Data2+
173	D3_N	CSI_D3M	I	2.5V	MIPI CSI Data3-
175	D3_P	CSI_D3P	I	2.5V	MIPI CSI Data3+
177	CLK_N	CSI_CLK0M	I	2.5V	MIPI CSI Clock-
179	CLK_P	CSI_CLK0P	I	2.5V	MIPI CSI Clock+
183	CAM_MCLK	NANDF_CS2	O	3.3V	we recommend oscillator on baseboard as MCLK source for camera
189	CAM_VCAM		PWR O	3.3V	Camera interface voltage out (3.3V)
193	CAM_PWDN	CSI0_DAT6	O	3.3V	High active powerdown signal
197	CAMRST	CSI0_DAT5	O	3.3V	High active reset signal
130	I2C_C_DAT	CSI0_DAT8	I/O	3.3V	I2C Serial Data (shared)
132	I2C_C_CLK	CSI0_DAT9	O	3.3V	I2C Serial Clock (shared)

Table 14: MIPI-CSI Pinout

Parallel camera (mounting option, please refer your ordered product version or ask for customized variant)

Note: Due to an HW failure, this pinout is just working starting from the HW Version 1.2 on efusA9 modules! On efusA9r2 modules there are no problems!

J1 Pin	Signal Name	CPU Pad	I/O	Voltage	Description
161	CAM_YDATA0*[1]	CSI0_DAT10	I	2.8V	Parallel camera interface Data0
163	CAM_YDATA1*[1]	CSI0_DAT11	I	2.8V	Parallel camera interface Data1
165	CAM_YDATA4	CSI0_DAT12	I	2.8V	Parallel camera interface Data4
167	CAM_YDATA3	CSI0_DAT13	I	2.8V	Parallel camera interface Data3
169	CAM_YDATA5	CSI0_DAT14	I	2.8V	Parallel camera interface Data5
171	CAM_YDATA2	CSI0_DAT15	I	2.8V	Parallel camera interface Data2
173	CAM_YDATA6	CSI0_DAT16	I	2.8V	Parallel camera interface Data6
175	CAM_PCLK	CSI0_PIXCLK	I	2.8V	Parallel camera interface Clock
177	CAM_YDATA7	CSI0_DAT17	I	2.8V	Parallel camera interface Data7
179	CAM_YDATA8	CSI0_DAT18	I	2.8V	Parallel camera interface Data8
187	CAM_YDATA9	CSI0_DAT19	I	2.8V	Parallel camera interface Data9
183	CAM_MCLK	NANDF_CS2	O	3.3V	we recommend oscillator on baseboard as MCLK source for camera
189	CAM_VCAM		PWR O	2.8V	Camera interface voltage out (2.8V)
191	CAM_HREF	CSI0_MCLK	I	2.8V	Parallel camera interface HREF
195	CAM_VSYNC	CSI0_VSYNC	I	2.8V	Parallel camera interface VSYNC
193	CAM_PWDN	CSI0_DAT6	O	2.8V	High active power down signal
197	CAMRST	CSI0_DAT5	O	2.8V	High active reset signal
130	I2C_C_DAT	CSI0_DAT8	I/O	3.3V	I2C Serial Data (shared)
132	I2C_C_CLK	CSI0_DAT9	O	3.3V	I2C Serial Clock (shared)

[1] These signals are shared with UART_C and cannot be used at the same time. In case of using UART_C, just the 8 bits (YDATA [2:9]) of the parallel camera interface are available. In that case the LSB (least significant bits) of the camera must be left unconnected

Table 15: Parallel Camera Interface Pinout

4.11 Power and Power Control Pins & Other GPIOs

J1 Pin	Signal Name	I/O	Voltage	Description
1…6	+5V	PWR I		VCC in, 5V +/-5%
9	VBAT	PWR I		RTC battery input. Leave open if not used
10	V33-Enable	PWR O		3.3V/100mA Vout use as enable for main board 3.3V if more current is required
11	ACOK	I	3.3V	USB OTG charge detect, for future usage
12	!RESET_IN	I	3.3V	3.3V 100k pull-up on module drives with OC/OD*[1] to GND. Leave open if not used.
14	!RESET_OUT	O	3.3V	4.7k pull down, active low reset for baseboard logic
25	PWM_A	O	3.3V	3.3V TTL level PWM output
	GND	PWR	GND	GND, connect all GND pins to GND plane

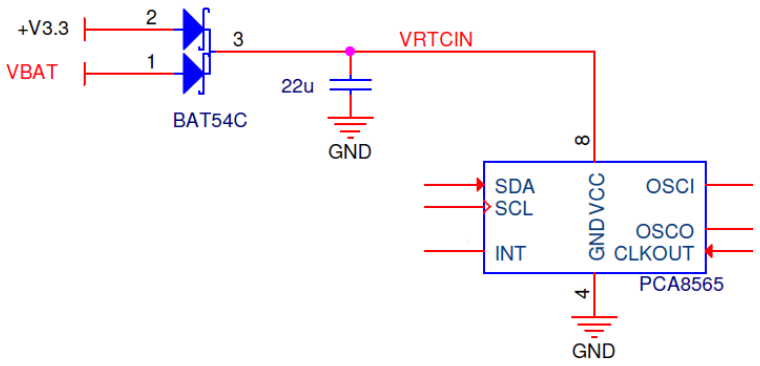
*[1] *OC/OD: Open Collector/Open Drain*

Table 16: Miscellaneous Pins

4.12 RTC

There is a NXP PCF8565 or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day.

Between VBAT and RTC is a diode to prevent current flow into an externally connected lithium cell.



5 LVDS-connector

J2	Signal Name	I/O	Voltage	Description
1	LVDS0_DATA0-	O	2.5V	LVDS0 Data Lane0-
2	LVDS0_DATA0+	O	2.5V	LVDS0 Data Lane0+
3	LVDS0_DATA1-	O	2.5V	LVDS0 Data Lane1-
4	LVDS0_DATA1+	O	2.5V	LVDS0 Data Lane1+
5	LVDS0_DATA2-	O	2.5V	LVDS0 Data Lane2-
6	LVDS0_DATA2+	O	2.5V	LVDS0 Data Lane2+
7	GND	PWR		
8	LVDS0_CLK-	O	2.5V	LVDS0 Clock Lane-
9	LVDS0_CLK+	O	2.5V	LVDS0 Clock Lane+
10	LVDS0_DATA3-	O	2.5V	LVDS0 Data Lane3-
11	LVDS0_DATA3+	O	2.5V	LVDS0 Data Lane3+
12	LVDS1_DATA0-	O	2.5V	LVDS1 Data Lane0-
13	LVDS1_DATA0+	O	2.5V	LVDS1 Data Lane0+
14	GND	PWR		
15	LVDS1_DATA1-	O	2.5V	LVDS1 Data Lane1-
16	LVDS1_DATA1+	O	2.5V	LVDS1 Data Lane1+
17	GND	PWR	2.5V	
18	LVDS1_DATA2-	O	2.5V	LVDS1 Data Lane2-
19	LVDS1_DATA2+	O	2.5V	LVDS1 Data Lane2+
20	LVDS1_CLK-	O	2.5V	LVDS1 Clock Lane-
21	LVDS1_CLK+	O	2.5V	LVDS1 Clock Lane+
22	LVDS1_DATA3-	O	2.5V	LVDS1 Data Lane3-
23	LVDS1_DATA3+	O	2.5V	LVDS1 Data Lane3+
24	GND	PWR		
25	I2C_C_DAT	I/O	3.3V	4.7k pull up onboard
26	VLCDON	O	3.3V	
27	I2C_C_CLK	O	3.3V	4.7k pull up onboard
28	VLCD	PWR O	3.3V/5V	Can be switched between 3.3V and 5V
29	VLCD	PWR O	3.3V/5V	Can be switched between 3.3V and 5V
30	VLCD	PWR O	3.3V/5V	Can be switched between 3.3V and 5V

Table 17: LVDS Connector Pinout

6 Memory Elements

6.1 NAND Flash

By default, boot mode of efusA9 is configured for NAND boot.

efusA9 implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored twice in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S to be robust against power failures

6.1.1 NAND Flash Data Retention

The NAND Flash is based on “single level cell” (SLC) technology. This technology is ten times more robust compared to “multi level cell” (MLC) technology. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6.2 eMMC Flash

This component is optional and not mounted in all configurations. Please contact sales to get more information.

6.2.1 eMMC Flash Data Retention

The eMMC Flash is based on “multi level cell” (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6.3 SPI NOR Flash

This device can be used for booting. Means you can store boot-loader and boot from this memory. Because selection of boot-medium is done with eFuse during manufacturing you have to order the efusA9 with the desired boot mode.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

6.4 I2C EEPROM

This component is optional and not mounted in all configurations. Please contact sales to get more information.RTC

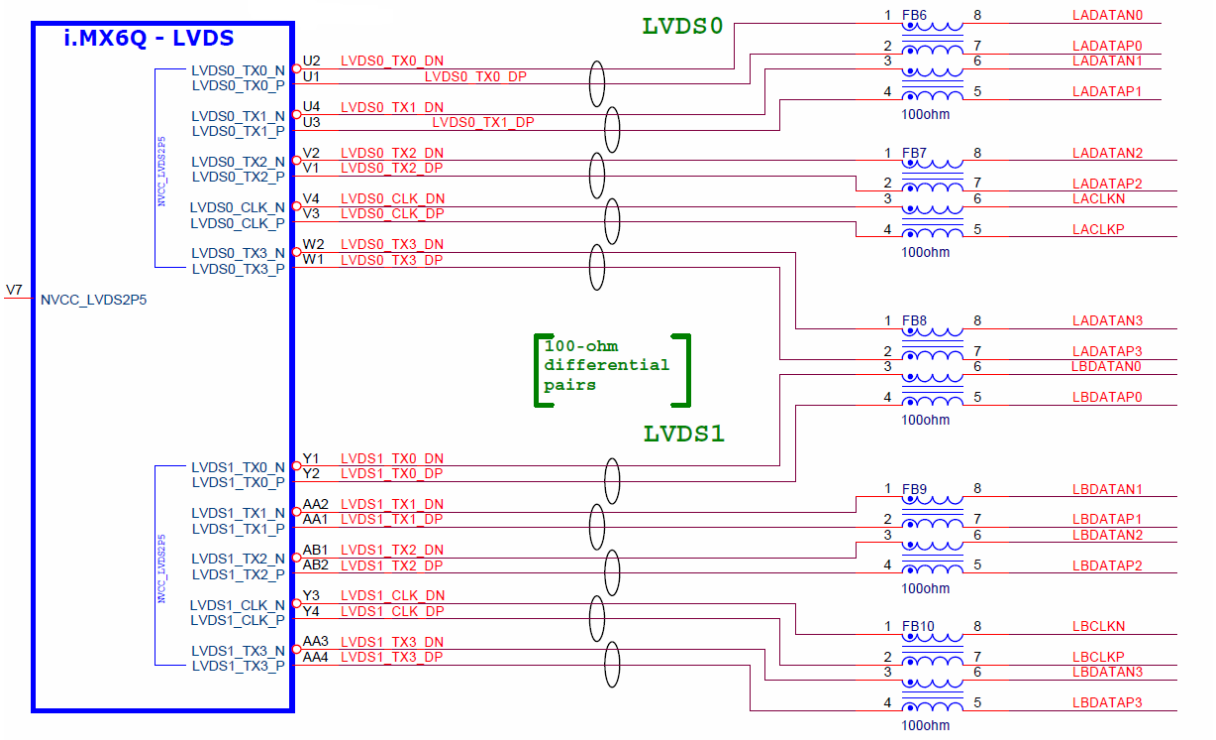
The dual channel LVDS display port can be direct connected to 2 LVDS 18 or 24 bit single channel or dual channel display.

Connector type: *JILI30 JAE FI-X30SSLA Connector or compatible*

VLCD can be switched between 3.3V and 5V depends on the LVDS display. 5V option is only available on efusA9 HW revision 1.21 or newer. All of the efusA9r2 modules have this option.

6.5 LVDS EMC protection

The following schematic shows the internal connection of LVDS signals between connector and CPU. The common mode chokes are TDK MCZ2010CH240L4T, Panasonic EXC-28CG240U or equivalent parts.



7 Thermal Specification

The described Embedded Module is a high performance computing system, which makes it necessary to develop a cooling concept. A general statement for such a cooling solution is not possible, because it depends on many factors like housing, power consumption, heat spreader, airflow and many others.

In order to keep the lifetime of the system as long as possible, the following points should be part of the cooling concept:

- The heat production of the module highly depends on the usage of CPU and GPU and therefore from customers software application.
  To reduce heat, the CPU offers a “Dynamic Voltage and Frequency Scaling” (DVFS), as well as “Thermal throttling” by an integrated temperature sensor. The integrated sensor measures the temperature of the CPU die and lowers CPU clock or shut down CPU if needed.
  DVFS lowers CPU clock and voltage in accordance with the performance needed from the application.
  For optimal use of DVFS, modify your software to only use peak performance for short times.
- The housing has big influence on the heat dissipation. There are many points to analyze:
  - Is there the option of dissipating heat to the housing?
  - Is there a possibility that the air can circulates in the housing?
  - Is an active cooling possible?
- The surrounding temperatures has a big effect to the temperature of the system.
- Be aware that an insufficient cooling will result in malfunction, a reduced lifetime or destruction.

The following table shows nominal thermal specification of the module:

	Min	Typ.	Max	Unit
Consumer Range Environmental Temperature	0		+70	°C
Consumer Range CPU Junction Temperature	-40		+105	°C
Industrial Range Environmental Temperature (I)	-20		+85	°C
Industrial Range CPU Junction Temperature (I)	-40		+125	°C
Junction to Package Top (ΨJT)		2		°C/W

Table 18: RGB LCD Pinout

Note 1: Maximum junction temperature of the CPU is 105°C/125°C. In this case cooling is a necessity and highly recommended. See also: Power Consumption and Cooling

Note 2: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN13273 (https://www.nxp.com/docs/en/application-note/AN13273.pdf)

8 Electrical characteristic

8.1 Absolute maximum ratings

Description	Min	Max	Unit
I/O Voltage range for 3.3V IO pins	-0.3	3.6	V
Maximum output current VLCD		500.0	mA
Maximum output current V33-Enable		100.0	mA

Table 19: Absolute maximum ratings

8.2 DC electrical characteristics for 3.3V IO pins

Parameter	Description	Min.	Typ.	Max.	Unit
VIN	efus™A9/r2 input supply voltage	4.5	5.0	5.5	V
I_{IN}	Input Current			1.0	A
VBAT	RTC Power Supply	2.2	3.0	3.45	V
P_{VBAT}	Power Consumption @25°C		3.0	10	µA
USB_DEV_VBUS	USB supply voltage	4.6	5.0	5.2	V
I_{VBUS}	USB supply current		100		mA
V_{ih}	High Level Input Voltage	2.43		3.43	V
V_{il}	Low Level Input Voltage	0		0.94	V
V_{oh}	High Level Output Voltage (I_{oh}=0.1mA)	2.98			V
V_{ol}	Low Level Output Voltage (I_{oh}=0.1mA)			0.15	V
I_o	Output current IOs		5.0		mA

Table 20: DC electrical characteristics

9 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

10 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

11 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

12 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **10 Watt**. This values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **5.5W (iMX6 Solo) to 7W (iMX6 Dual Lite with eMMC)** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

13 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

14 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

15 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
efus™ modules are shipped in trays. One tray can hold 10 boards. An empty tray is used as top cover.

16 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: matrix code sticker

17 Appendix

Important Notice

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