

# NetDCUA5 GPIO Reference Card

V1.0

23.02.2014

## Pin Layout for Board Rev. 1.10

### I/O-Connector J5

J5	Function	Device	GPIO	Mode	/sys/class/gpio/gpio#	SKIT
1	EINT	GPIO	PTB18	IO	40	J15_1
2	ROW7	KEYBD	PTA12	IO	5	J15_2
3	ROW6	KEYBD	PTA11	IO	4	J15_3
4	ROW5	KEYBD	PTA10	IO	3	J15_4
5	ROW4	KEYBD	PTA9	IO	2	J15_5
6	ROW3	KEYBD	PTA8	IO	1	J15_6
7	ROW2	KEYBD	PTD26	IO	68	J15_7
8	ROW1	KEYBD	PTD25	IO	69	J15_8
9	ROW0	KEYBD	PTD24	IO	70	J15_9
10	SPI_MISO / COL8 / I2C_SDA	SPI / KEYBD / I2C	PTB20 / PTB20 / PTD27	IO / IO / IO	42 / 42 / 67	J15_10
11	SPI_MOSI / COL9 / I2C_SCL	SPI / KEYBD / I2C	PTB21 / PTB21 / PTD28	IO / IO / IO	43 / 43 / 66	J15_11
12	UART_B_RXD <sup>(2)</sup>	UART	PTD1	I (IO)	80	J1F_B_2
13	SPI_CS0 / COL10	SPI / KEYBD	PTB19	IO / IO	41	J15_13
14	UART_B_TXD <sup>(1)</sup>	UART	PTD0	O (IO)	79	J1F_B_3
15	SPI_CLK / COL11	SPI / KEYBD	PTB22	IO / IO	44	J15_15
16	GND					J15_16
17	COL7	KEYBD	PTD31	IO	63	J15_17
18	COL6	KEYBD	PTD30	IO	64	J15_18
19	COL5	KEYBD	PTD29	IO	65	J15_19
20	COL4	KEYBD	PTD6	IO	85	J15_20
21	COL3	KEYBD	PTD5	IO	84	J15_21
22	COL2	KEYBD	PTD4	IO	83	J15_22
23	COL1	KEYBD	PTD3	IO	82	J15_23
24	COL0	KEYBD	PTD2	IO	81	J15_24
25	V5					J15_25
26	V3.3					J15_26

- (1) If the RS232 level shifter is mounted, this pin can theoretically be used as General Purpose Output only and carries RS232 level then; if the level shifter is not mounted, it can be Input and Output and uses 3.3V level
- (2) If the RS232 level shifter is mounted, this pin can theoretically be used as General Purpose Input only and expects RS232 level then; if the level shifter is not mounted, it can be Input and Output and uses 3.3V level

### Power/Serial Connector

J1	Function	Device	GPIO	Mode	/sys/class/gpio/gpio#	SKIT
1	ETH_A_RX+	ETH				J1B_3
2	ETH_A_RX-	ETH				J1B_5
3	UART_A RTS <sup>(1)</sup>	UART	PTB6	O (IO)	28	J1F_A_7
4	UART_A_RXD <sup>(2)</sup>	UART	PTB5	I (IO)	27	J1F_A_2
5	UART_A_CTS <sup>(2)</sup>	UART	PTB7	I (IO)	29	J1F_A_8
6	UART_A_TXD <sup>(1)</sup>	UART	PTB4	O (IO)	26	J1F_A_3
7	ETH_A_TX+	ETH				J1B_1
8	ETH_A_TX-	ETH				J1B_2
9	V5 (output)					
10	GND					
11	CAN_A_TX <sup>(3)</sup>	CAN	PTB15	IO	37	J1D_3/4
12	CAN_A_RX <sup>(3)</sup>	CAN	PTB14	IO	36	J1D_3/4
13	CAN_B_TX <sup>(3)</sup>	CAN	PTB17	IO	39	J1E_3/4
14	CAN_B_RX <sup>(3)</sup>	CAN	PTB16	IO	38	J1E_3/4
15	ETH_B_RX+	ETH				J1C_3
16	ETH_B_RX-	ETH				J1C_5
17	ETH_B_TX+	ETH				J1C_1
18	ETH_B_TX-	ETH				J1C_2
19	VCFL (input)					J1A_1
20	-					
21	V5 (input)					J1A_2
22	V5 (input)					J1A_2
23	VBAT (input)					J1A_3
24	-					
25	GND					J1A_4
26	GND					J1A_4

- (1) If the RS232 level shifter is mounted, this pin can theoretically be used as General Purpose Output only and carries RS232 level then; if the level shifter is not mounted, it can be Input and Output and uses 3.3V level
- (2) If the RS232 level shifter is mounted, this pin can theoretically be used as General Purpose Input only and expects RS232 level then; if the level shifter is not mounted, it can be Input and Output and uses 3.3V level
- (3) Pin has internal level shifter and uses 5V level!