

# Hardware Documentation

## *armStone™ A5* *for HW Revision 1.20*

Version 008  
(2021-08-20)



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Systeme**

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# About This Document

This document describes how to use the [armStone™ A5](#) board with mechanical and electrical information. The latest version of this document can be found at:

<http://www.fs-net.de>.

## ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

## History

Date	V	Platform	A,M,R	Chapter	Description	Au
06.02.2013	001	All			Initial Version	DB
14.02.2013	002	All	M		Minor changes	DB
25.07.2013	003	All	M		Change battery current	DB
21.08.2013	004	All	A		Added connector chapter	DB
02.05.2014	005	All	M		Naming of connector	HF
15.08.2014	005	All	M	*	Changed to New Company CI	JG
18.08.2014	006	All	M		Add current consumption	KW
25.09.2019	007	All	M	4.5	Correction in LVDS Connector Pin layout table	MD
19.08.2021	008	All	M	*	Update to HW Revision 1.20; Change to new Layout	MW

V Version

A,M,R Added, Modified, Removed

Au Author

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# 1 Block Diagram

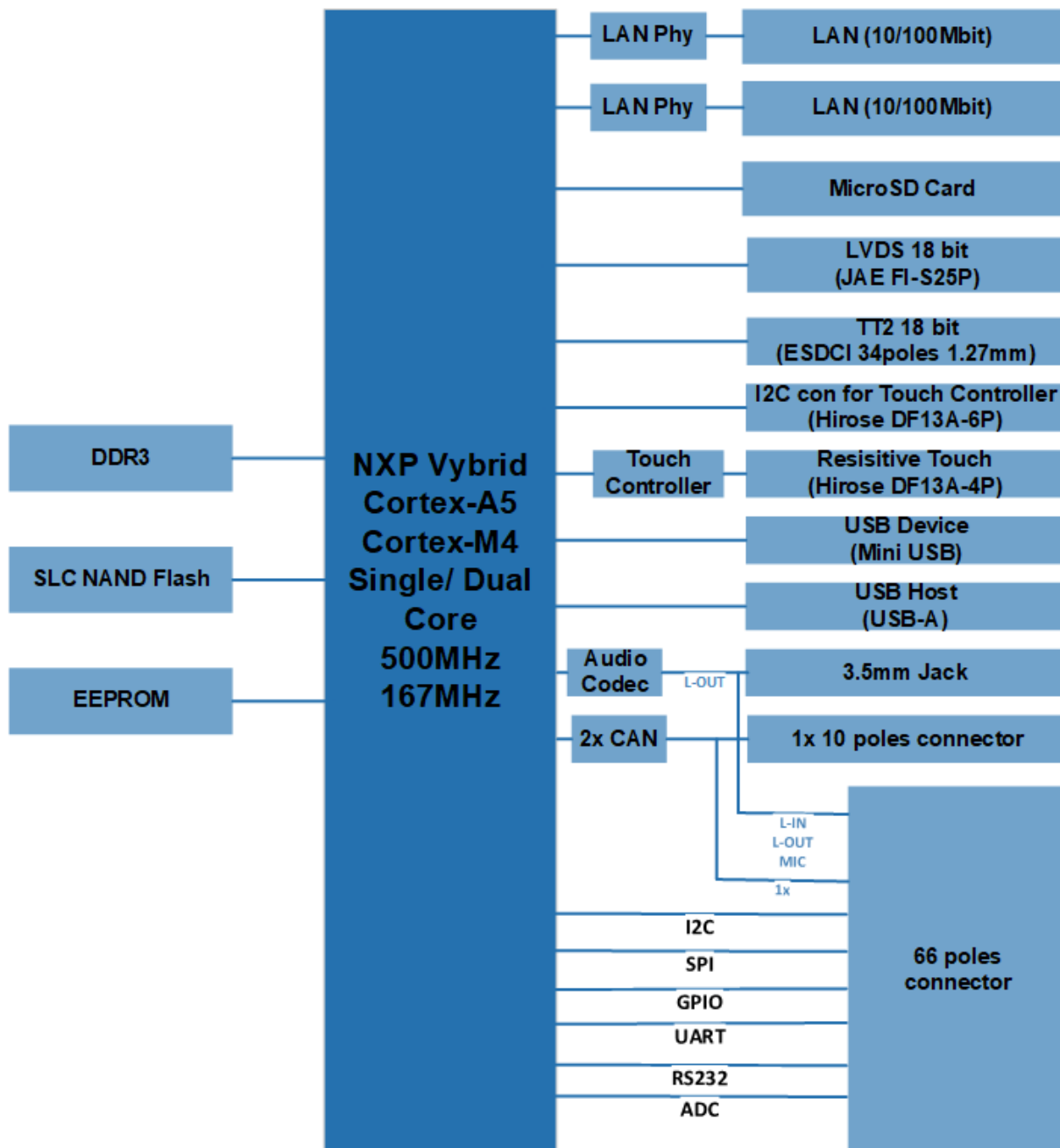


Figure 1: Block Diagram

## 2 Mechanical Dimension

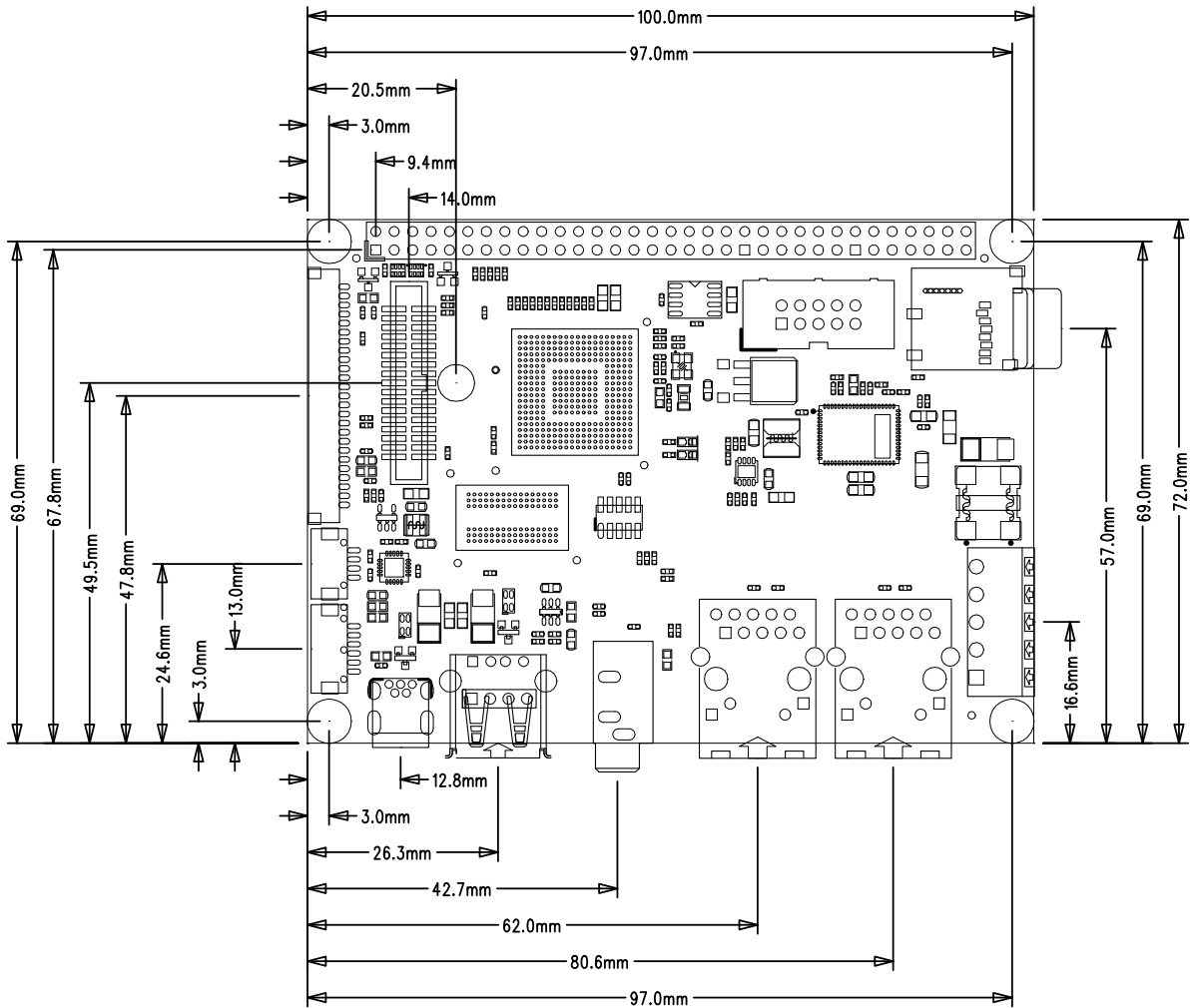


Figure 2: Mechanical Dimension Top

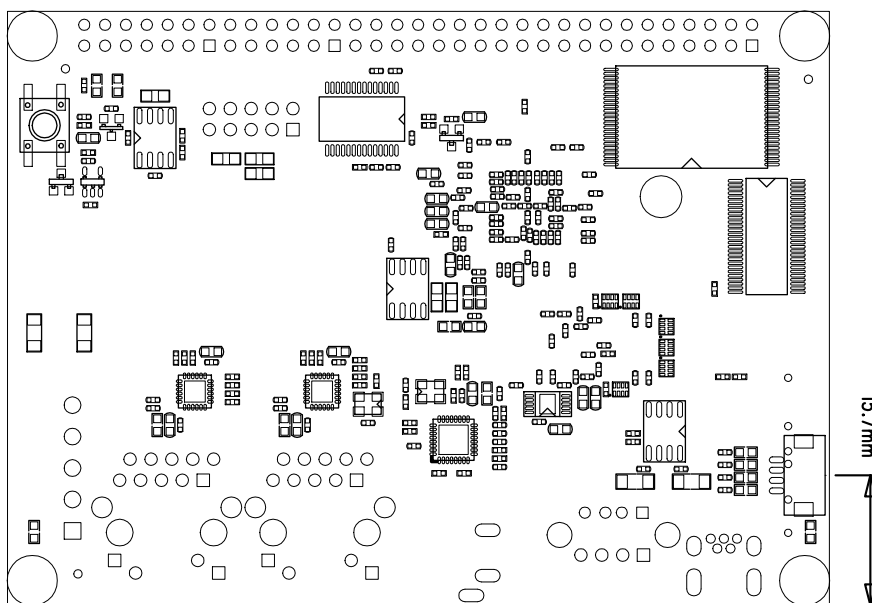


Figure 3: Mechanical Dimension Bottom

Dimensions	Description
Size	100mm x 72mm
PCB Thickness	1.5mm ± 0.1mm
Height of the parts on the top side	14mm
Height of the parts on the bottom side	3mm
Weight	55gr.

*Table 1: Mechanical Dimensions*

3D Step model available, please contact [support@fs-net.de](mailto:support@fs-net.de)

# 2.1 Connectors Layout

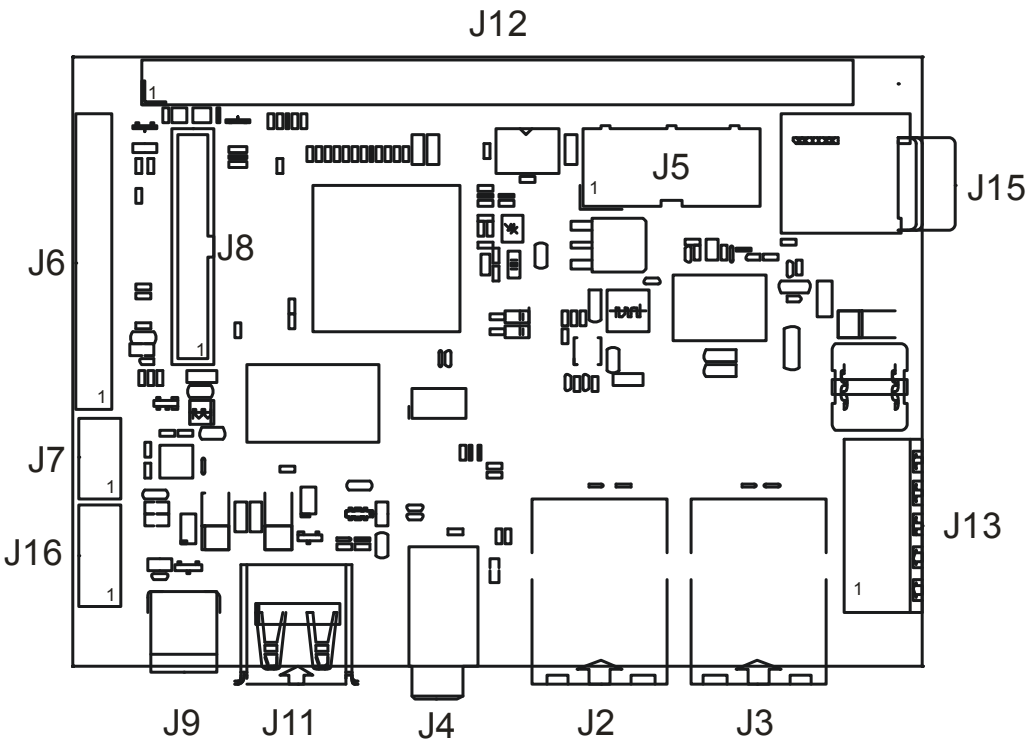


Figure 4: Connector Layout Top

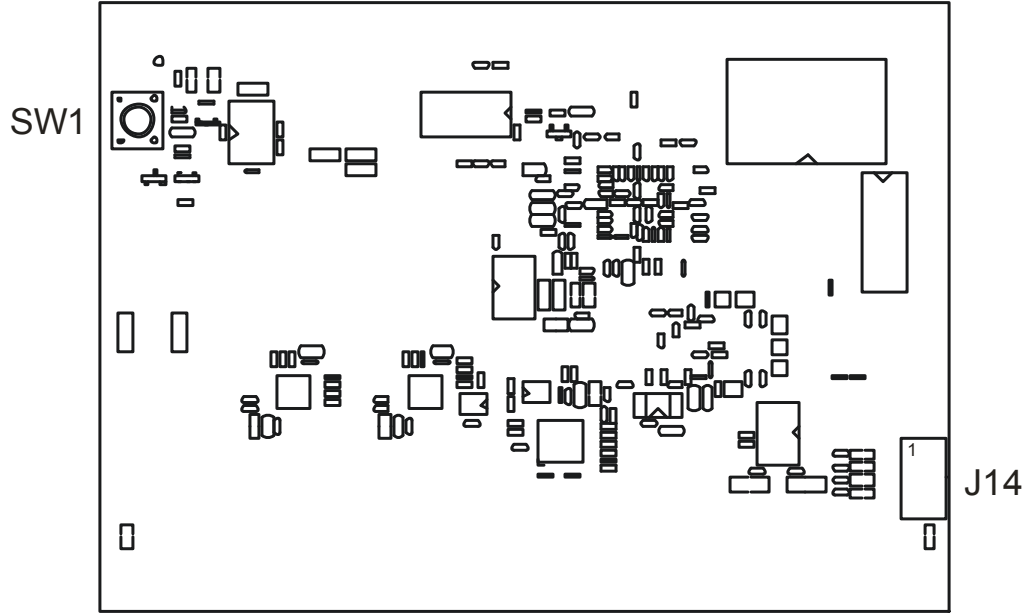


Figure 5: Connector Layout Bottom



	Description	PCB Side	Pin Number	Part Type
<b>J2</b>	Ethernet 100MBit RJ45 With Integrated Magnetics	Top	12	Würth Elektronik 74990100211
<b>J3</b>	Ethernet 100MBit RJ45 With Integrated Magnetics	Top	12	Würth Elektronik 74990100211
<b>J4</b>	Audio Connector	Top	3	CUI Inc SJ1-3533NG
<b>J5</b>	CAN Connector	Top	10	FCI 75869-501
<b>J6</b>	LVDS-Connector	Top	25	JAE FI-S25P-HFE
<b>J7</b>	Backlight Connector	Top	4	Hirose DF13-4P-1.25H(20)
<b>J8</b>	TFT RGB Connector	Top	34	Nexus 1171V34BR00
<b>J9</b>	USB-Device Connector	Top	5	Nexus 3854RJBY
<b>J11</b>	USB-Host Type-A Connector	Top	8	Würth Elektronik 61400416021
<b>J12</b>	Feature Connector, 2.54mm Pitch Connector	Top	66	
<b>J13</b>	Power Connector	Top	5	Würth Elektronik 691322310005
<b>J14</b>	Resistive Touch Connector	Bottom	4	Hirose DF13-4P-1.25H(20)
<b>J15</b>	MicroSD Slot	Top	-	Molex 512811294
<b>J16</b>	I2C Touch Connector	Top	6	Hirose DF13-6P-1.25H(20)
<b>SW 1</b>	Reset Button	Bottom	-	Panasonic EVQQ2201W

Table 2: Connectors Layout

## 3 Interface and Signal Description

### 3.1 Power Supply

The armStone board has per default a 5 way connector with 3,81mm pitch for an external DC power supply. The connector is compatible to F&S power supply [ADP-NT24V2](#) (IN 13-36V, OUT 5V+12V)

Connector Base Board: Würth WR-TBL Series 322 – 5- pins

Matching Connector: Würth WR-TBL Series 2109.

J13 Pin	Signal Name	I/O	Remarks
1	NC		
2	VBAT_IN	PWR	Voltage: 2.2V-3.45V (*Optional for external RTC voltage supply)
3	+V5.0_IN	PWR	Voltage: 4.5V-5.5V
4	GND_IN	PWR	
5	+V3.3	OUT	3.3V power output for external logic, max. current 50mA

*Table 3: Power J15 Connector Pin Layout*

If an external 3.3V power supply is used for external logic, we recommend to use the “VCC Out 3.3V” as enable signal for this power supply to avoid backdrive leak current through IO pins.

## 4 Interfaces

### 4.1 USB Host

The single USB Host connector does support USB2.0 connection with high speed up to 480Mbit/s and also full and low speed devices.

The power on the 5V line is equipped with a resettable fuse with 500mA. The USB signals are routed as 90 Ohm differential pairs. ESD and EMV protection is included in PCB design.

J11 Pin	Signal	I/O	Voltage	Description
1	USB_Host_PWR	O	5,0V	Output voltage, switched by USB Switch
2	USB_Host_DN	I/O		90 Ohm differential pair
3	USB_Host_DP	I/O		
4	GND	PWR		

Table 4: USB Host Interface (Type-A Connector)

### 4.2 USB Device

The USB Device Port is realised on a Mini USB connector without OTG functionally.

The USB signals are routed as 90 Ohm differential pairs. ESD and EMV protection is included in PCB design.

J9 Pin	Signal	I/O	Voltage	Description
1	USB1_VBUS	PWR	5V	Input
2	USB1_DP	I/O		90 Ohm differential pair
3	USB1_DN	I/O		
4	NC	-	-	Not Connected
5	GND	PWR		

Table 5: USB Device Interface

### 4.3 Micro SD / Micro SIM card

To access a Micro SD there is a holder on the armStone.

The microSD push-push connector supports the SD Standard Host Specification Version 2.0 standard.

Connector type: Molex: 512811294

J9 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	SDHC_DATA2	PTA28	I/O	3.3V	
2	SDHC_DATA3	PTA29	I/O	3.3V	
3	SDHC_CMD	PTA25	O	3.3V	10k Pull-Up
4	VDD_SD		PWR	3.3V	Enabled if SD is insert
5	SDHC_CLK	PTA24	O	3.3V	
6	GND		PWR		
7	SDHC_DATA0	PTA26	I/O	3.3V	
8	SDHC_DATA1	PTA27	I/O	3.3V	
9	SDHC_CDn	PTA7	I	3.3V	Cad insert = Low

Table 6: SD Card Interface A

## 4.4 Ethernet Interface

The board supports two 10/100 Mbit LAN interfaces. Two 10/100 Megabit PHY Micrel KSZ8081 is mounted on the board.

J2 Pin	Signal	Function	I/O	Description
1	ETH0_TX_P		I/O	
2	ETH0_TX_N		I/O	
3	ETH0_RX_P		I/O	
4	GND via 100nF			
5	GND via 100nF			
6	ETH0_RX_N		I/O	
7	NC			
8	GND		PWR	
9	3.3V via 300Ω		PWR	
10	LED0		O	LED Signal of Ethernet Phy
11	NC			
12	NC			

Table 7: Ethernet Interface

J3 Pin	Signal	Function	I/O	Description
1	ETH1_TX_P		I/O	
2	ETH1_TX_N		I/O	
3	ETH1_RX_P		I/O	
4	GND via 100nF			
5	GND via 100nF			
6	ETH1_RX_N		I/O	
7	NC			
8	GND		PWR	
9	3.3V via 300Ω		PWR	
10	LED0		O	LED Signal of Ethernet Phy
11	NC			
12	NC			

Table 8: Ethernet Interface

## 4.5 TTL RGB Interface

Connector is a 1.27mm pitch shrouded header for 1.27mm pitch IDC connector.

All signals have 3.3V level.

**Note: the RGB display signals are used with a transceiver behind for the LVDS interface too. So only a LVDS or a RGB display is usable.**

J8 Pin	Signal	I/O	Voltage	Description
1	+V3.3	PWR	3.3V	
2	+V5.0	PWR	5.0V	
3	GND	PWR		
4	LCD_CLK	O	3.3V	
5	LCD_HSYNC	O	3.3V	
6	LCD_VSYNC	O	3.3V	
7	GND	PWR		
8	LCD_R0	O	3.3V	
9	LCD_R1	O	3.3V	
10	LCD_R2	O	3.3V	
11	LCD_R3	O	3.3V	
12	LCD_R4	O	3.3V	
13	LCD_R5	O		
14	GND	PWR		
15	LCD_G0	O	3.3V	
16	LCD_G1	O	3.3V	
17	LCD_G2	O	3.3V	
18	LCD_G3	O	3.3V	
19	LCD_G4	O	3.3V	
20	LCD_G5	O		
21	GND	PWR		
22	LCD_B0	O	3.3V	
23	LCD_B1	O	3.3V	
24	LCD_B2	O	3.3V	
25	LCD_B3	O	3.3V	
26	LCD_B4	O	3.3V	
27	LCD_B5	O	3.3V	
28	GND	PWR		
29	LCD_DE	O	3.3V	
30	VLCD	PWR	3.3V	3.3V switched
31	VLCD	PWR	3.3V	3.3V switched
32	I2C_DAT	I/O	3.3V	2,2k pull-up; Shared with on-board touch and I2C Connector
33	I2C_IRQ	I	3.3V	
34	I2C_CLK	O	3.3V	2,2k pull-up; Shared with on-board touch and I2C Connector

## 4.6 LVDS Interface

The single channel LVDS display port can be direct connected to a LVDS 18 bit display.

The VLCD voltage is 3.3V and can be switched. The current limit is 1.2 A.

Connector is a JAE FI-S25P-HFE. Matching connector on display cable is a crimp connector FI-S25S housing and a cable with FI-C3-A1-15000 crimp contacts.

This connector is used because a wide range of displays does have a JAE FI-S series connector (with different pinouts) and it's easy to handle identical crimp contacts for the cable manufacturer.

The LVDS signals are generated by a RGB to LVDS Bridge.

Unused signals should be left unconnected.

**Note: the display signals are the RGB signals with a LVDS transceiver behind. So only a LVDS or a RGB display is usable.**

J6 Pin	Signal	I/O	Voltage	Description
1	LVDS_A_D0-	O		
2	LVDS_A_D0+	O		
3	LVDS_A_D1-	O		
4	LVDS_A_D1+	O		
5	LVDS_A_D2-	O		
6	LVDS_A_D2+	O		
7	GND	PWR		
8	LVDS_A_CLK-	O		
9	LVDS_A_CLK+	O		
10	LVDS_A_D3-	O		
11	LVDS_A_D3+	O		
12	LVDS_B_D0-	O		
13	LVDS_B_D0+	O		
14	GND	PWR		
15	LVDS_B_D1-	O		
16	LVDS_B_D1+	O		
17	GND	PWR		
18	LVDS_B_D2-	O		
19	LVDS_B_D2+	O		
20	LVDS_B_CLK-	O		
21	LVDS_B_CLK+	O		
22	LVDS_B_D3-	O		
23	LVDS_B_D3+	O		
24	GND	PWR		
25	I2C_SDA	I/O	3,3V	Connect to I2C2_SDA with 4.7k $\Omega$ Pull Up
26	I2C_IRQ / VLCDON	I / O	3,3V	Connect to SAI3_MCLK
27	I2C_SCL	O	3,3V	Connect to I2C2_SCL with 4.7k $\Omega$ Pull Up
28	VLCD	PWR		3,3V or 5V Output switched by VLCDON
29	VLCD	PWR		
30	VLCD	PWR		

Table 9: LVDS Interface



## 4.7 I2C Touch Interface

To connect a capacitive Touchpanel via I<sup>2</sup>C, the SBC offers the I<sup>2</sup>C Signals on a 6-pin connector.

Connector type: Hirose DF13-6P-1.25H

Unused signals should be left unconnected.

J16 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	3.3V		PWR		Maximal 50mA Output
2	I2C3_SDA	PTA31	I/O	3.3V	2.2k $\Omega$ Pull Up; Shared with TTL RGB Connector
3	I2C3_SCL	PTA30	O	3.3V	2.2k $\Omega$ Pull Up; Shared with TTL RGB Connector
4	I2C3_RST	PTE21	O	3.3V	
5	I2C3_IRQ	PTE22	I	3.3V	Shared with TTL RGB Connector
6	GND		PWR		

Table 10: I2C Touch Interface

## 4.8 Resistive Touch Interface

The integrated resistive touch controller will support 4 wire analog resistive touch panels.

The connector is a Hirose 4 pin connector, model no. DF13A-4P-1.25H, mounted on the armStoneA5 module. Pin 1 is marked on PCB.

Connector type: Hirose DF13-6P-1.25H

Unused signals should be left unconnected.

J14 Pin	Signal	Description
1	XP	Touch X+
2	YP	Touch Y+
3	XN	Touch X-
4	YN	Touch Y-

Table 11: Resistive Touch Interface

## 4.9 Backlight Interface

To control the LCD voltage and Backlight, the SBC offers a 4-pin connector with the control pins.

Connector type: Hirose DF13-4P-1.25H

J7 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	VLCD_ON	PTE3	O	3.3V	Display on/off
2	BL_ON	PTC29	O	3.3V	Backlight on/off
3	BL_PWM	PTB0	O	3.3V	Backlight Brightness
4	GND		PWR		

Table 12: Backlight Interface

### 4.9.1 Solution with a single cable with 3 connectors

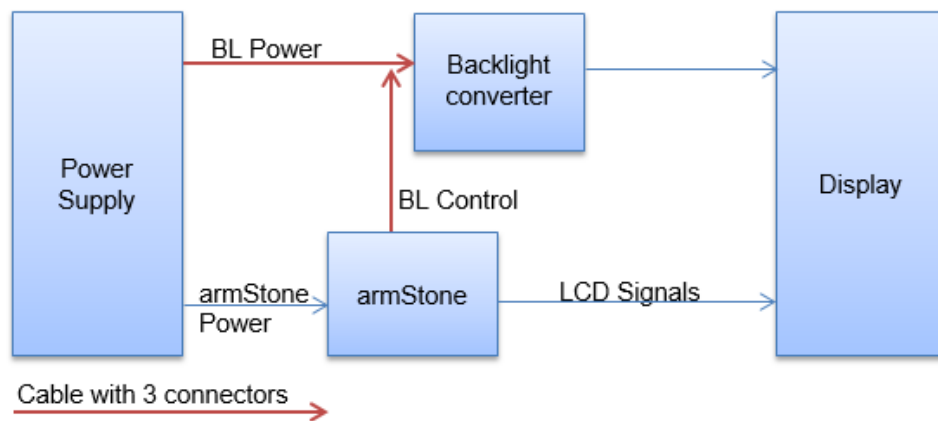


Figure 6: Backlight connection with single cable

**4.9.2 Solution with 2 cable with 2 connectors each**

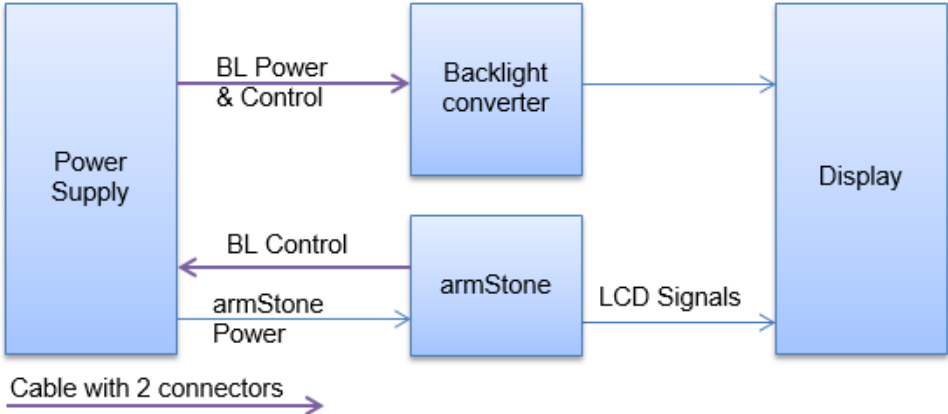


Figure 7: Backlight connection with 2 cable

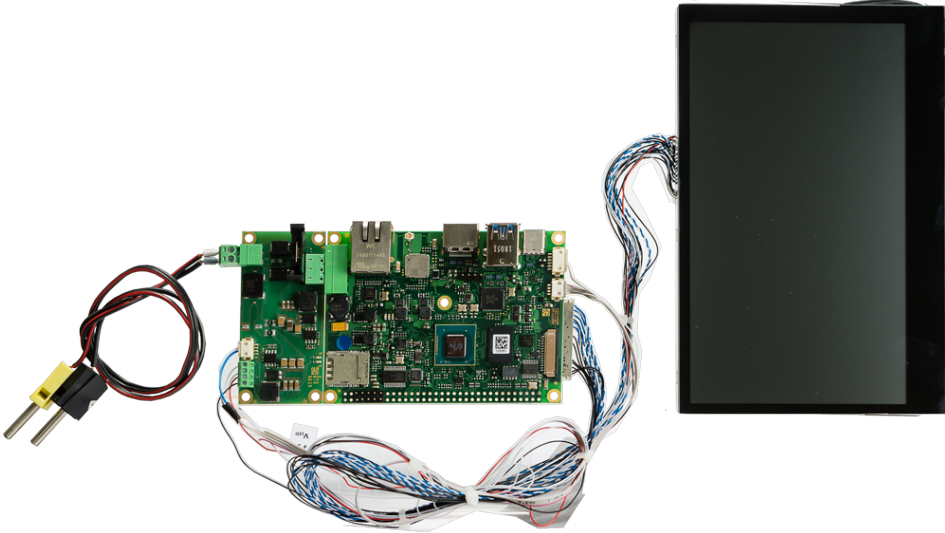


Figure 8: Backlight connection with 2 cable

## 4.10 CAN Interface

This connector is a 2.54mm pitch shrouded header.

J5 Pin	Signal	I/O	Voltage	Description
1	+V3.3 / +V5.0	PWR	3.3V / 5.0V	Mounting option
2	GND	PWR		
3	CAN1L	I/O		CAN1 Low
4	CAN1H	I/O		CAN1 High
5	GND	PWR		
6	NC			
7	NC			
8	+V3.3 / +V5.0	PWR	3.3V / 5.0V	Mounting option
9	NC			
10	NC			

Table 13: CAN Interface

## 4.11 Audio Interface

A 3.5mm Stereo phone jack provides audio line-out. The signals are shared with the audio signals on the Feature connector.

## 4.12 GPIO

GPIOs are free programmable. All GPIOs can trigger an interrupt. Pullups or pulldowns are configurable by software, but they are not available at board start-up. On a non-powered board it's not allowed to have a voltage on GPIO pins. Also a higher voltage as the announced IO power is not allowed.

## 4.13 Feature Connector

The SBC supports an I2C interface as I2C master. Devices on baseboard with other voltage need a level shifter. It's the preferred I2C for touch controller.

For more chip selects, interrupts and other signals use GPIOs and modify the driver.

J12 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	VCC3.3	-	PWR	3.3V	
2	VCC5	-	PWR	5.0V	
3	XGPIO0 / COL0	PTD2	I/O	3.3V	4.7k $\Omega$ Pull Up
4	XGPIO1 / COL1	PTD3	I/O	3.3V	4.7k $\Omega$ Pull Up
5	XGPIO2 / COL2	PTD4	I/O	3.3V	4.7k $\Omega$ Pull Up
6	XGPIO3 / COL3	PTD5	I/O	3.3V	4.7k $\Omega$ Pull Up
7	XGPIO4 / COL4	PTD6	I/O	3.3V	4.7k $\Omega$ Pull Up
8	XGPIO5 / COL5	PTD29	I/O	3.3V	4.7k $\Omega$ Pull Up
9	XGPIO6 / COL6	PTD30	I/O	3.3V	4.7k $\Omega$ Pull Up
10	XGPIO7 / COL7	PTD31	I/O	3.3V	4.7k $\Omega$ Pull Up
11	GND	-	PWR		
12	XGPIO8 / SPI_CLK	PTB22	I/O	3.3V	4.7k $\Omega$ Pull Up
13	XGPIO9 / TXD2	PTD0	I/O	3.3V	- / 4.7k $\Omega$ Pull Up for SAI1_RXD6
14	XGPIO10 / SPI_CS	PTB19	I/O	3.3V	4.7k $\Omega$ Pull Up
15	XGPIO11 / RXD2	PTD1	I/O	3.3V	100k $\Omega$ Pull Up / 4.7k $\Omega$ Pull Up for SAI1_RXD7
16	XGPIO12 / I2C_CLK / SPI_MOSI	PTB21	I/O	3.3V	4.7k $\Omega$ Pull Up for SAI3_RXC
17	XGPIO13 / I2C_DAT/ SPI_MISO	PTB20	I/O	3.3V	4.7k $\Omega$ Pull Up for SAI3_RXD
18	XGPIO14 / ROW0 / TXD1	PTD24	I/O	3.3V	
19	XGPIO15 / ROW1	PTD25	I/O	3.3V	4.7k $\Omega$ Pull Up
20	XGPIO16 / ROW2 / RXD1	PTD26	I/O	3.3V	100k $\Omega$ Pull Up
21	XGPIO17 / ROW3	PTA8	I/O	3.3V	4.7k $\Omega$ Pull Up
22	XGPIO18 / ROW4	PTA9	I/O	3.3V	4.7k $\Omega$ Pull Up
23	XGPIO19 / ROW5	PTA10	I/O	3.3V	4.7k $\Omega$ Pull Up
24	XGPIO29 / ROW6	PTA11	I/O	3.3V	4.7k $\Omega$ Pull Up
25	XGPIO21 / ROW7	PTA12	I/O	3.3V	4.7k $\Omega$ Pull Up

26	KBINT	PTB23	I/O	3.3V	4.7k $\Omega$ Pull Up
27	GND	-	PWR		
28	XGPIO22 / PWMOUT0	PTB1	I/O	3.3V	4.7k $\Omega$ Pull Up
29	XGPIO23 / ADC_IN0	ADC0SE8	I/O	3.3V	ADC from ADS1015 / 4.7k $\Omega$ Pull Up for I2C3_SDA
30	XGPIO24 / PWMOUT1	PTB8	I/O	3.3V	4.7k $\Omega$ Pull Up
31	XGPIO25 / ADC_IN1	ADC0SE9	I/O	3.3V	ADC from ADS1015 / 4.7k $\Omega$ Pull Up for I2C3_SCL
32	XGPIO26 / PWMOUT2	PTB9	I/O	3.3V	4.7k $\Omega$ Pull Up
33	XGPIO27 / ADC_IN2	ADC1SE8	I/O	3.3V	ADC from ADS1015/ 4.7k $\Omega$ Pull Up for SAI3_TXD
34	Backlight On	PTC29	O	3.3V	4.7k $\Omega$ Pull Down
35	XGPIO28 / ADC_IN3	ADC1SE9	I/O	3.3V	ADC from ADS1015/ 4.7k $\Omega$ Pull Up for SAI3_RXFS
36	RXD3 (RS232)	-	I/O		100k $\Omega$ Pull Up
37	GND	-	PWR		
38	TXD3 (RS232)	-	I/O		
39	VCC3.3	-	PWR		
40	VCC5	-	PWR		
41	MIC1 (Audio pin 1)	-	I		From SGTL5000
42	GND	-	PWR		
43	Not connected	-	-		
44	LINEIN_R	-	I		From SGTL5000
45	LINEOUT_R	-	O		From SGTL5000
46	GND	-	PWR		
47	GND	-	PWR		
48	LINEIN_L	-	I		From SGTL5000
49	LINEOUT_L	-	O		From SGTL5000
50	GND	-	PWR		
51	RESETBTN	-	I		Leave open if not used
52	VCC3.3	-	PWR		
53	Not connected	-	-		
54	Not connected	-	-		

<b>55</b>	RXD1 (RS232)	-	I		From UART2_RXD via SP3243
<b>56</b>	RTS1 (RS232)	-	O		From UART4_RXD via SP3243
<b>57</b>	TXD1 (RS232)	-	O		From UART2_TXD via SP3243
<b>58</b>	CTS1 (RS232)	-	I		From UART4_TXD via SP3243
<b>59</b>	Not connected	-	-		
<b>60</b>	Not connected	-	-		
<b>61</b>	GND	-	PWR		
<b>62</b>	VCC5 (COM keypin)	-	PWR		
<b>63</b>	CAN1RX / CAN1L	PTB14	I/O		From MCP2515 optional with CAN transceiver
<b>64</b>	CAN1TX / CAN1H	PTB15	I/O		From MCP2515 optional with CAN transceiver
<b>65</b>	BOOTSEL	-	I		Connect with Pin 66 to set SBC into Bootmode; Leave unconnected if unused
<b>66</b>	VCC3.3	-	PWR		

*Table 14: Feature Connector*

### 4.13.1 Audio

The feature connector provides Stereo Line in, Stereo Line out and microphone.

### 4.13.2 RS232 COM port

A 9 pin double row connector is mounted in pin 53...61. That allows to attach a standard 9pin to DSUB9 adapter cable for debug output of bootloader and kernel with TX, RX, RTS and CTS to a terminal.

Pin 1 of this adapter should connect on pin 53 of the 66 pin connector. Pin 62 is the key pin and should be removed.

On pin 36 & 38 is a second RS232 COM port (RXD2/TXD2).

### 4.13.3 TTL COM port

There is additional serial port with 3.3V TTL level (RXD1/TXD1).

### 4.13.4 SPI

The module supports a HS SPI (Serial Peripheral Interface) with 2 chip selects. Signals are 3.3V compliant and have 4.7k pull-ups on module.

### 4.13.5 I2C

The module supports an I2C interface as I2C master. Signals are 3.3V compliant and have 4.7k pull-ups on module.

### 4.13.6 ADC In

4 ADC inputs (ADC\_IN0...3)

- Resolution: 12-bit
- Differential Nonlinearity Error:  $\pm 1.0$  LSB (Max.)
- Integral Nonlinearity Error:  $\pm 4.0$  LSB (Max.)
- Maximum Conversion Rate: 0.5 MSPS
- Analog Input Range: 0 ~ 3.3V
- On-chip sample-and-hold function

### 4.13.7 PWM out

3 programmable PWM outputs (PWMOUT0...2) with 3.3V level in 16.1kHz up to 33 MHz frequency range

### 4.13.8 Matrix keyboard

8x8 keyboard matrix (ROW0...7, COL0...1) with 3.3V level. The ROW signals have 4.7k pull-ups on module.



## 4.14 JTAG

J1 Pin	Signal	CPU Pad	I/O	Voltage	Description
1	3.3V		PWR		
2	JTAG_TMS	PTA11		3,3V	
3	GND		PWR		
4	JTAG_TCK	PTA8		3,3V	
5	GND		PWR		
6	JTAG_TDO	PTA10		3,3V	
7	NC				
8	JTAG_TDI	PTA9		3,3V	
9	GND		PWR		
10	RESETn	RESET		3,3V	

*Table 15: JTAG Interface*

- For debug only
- Leave unconnected, if you don't use JTAG
- Don't put them in a JTAG chain, because different power sequence and power level could kill the CPU

## 5 Power and Power Control Pins

J15 Pin	J16 Pin	Signal	I/O	Description
3	3, 4, 5, 6	VIN (+V5S)	I	Main Power supply input please refer chapter ADP-NT24V2
4	7, 8, 9, 10	GND	I	Main Power supply Ground input
2	1, 2	VDD_VBAT	I	RTC battery input; tie to 3.0V please refer chapter ADP-NT24V2
5	-	3.3V	O	20mA output from on board DCDC powered from VIN

Table 16: Power and Power Control

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory. It's possible to use a supercap instead.

3.3V is the 3.3V power supply of the board generated form PMIC and powered from VIN. Use as enable for baseboard power regulators.

# 6 Flash

## 6.1 NAND Flash

By default, boot mode is configured for NAND boot.

The board implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S or TFAT to be robust against power failures

## 7 ADP-NT24V2

To power the armStoneA9 with 7,5-36V F&S provide a power supply Adapter: ADP-NT24V2:

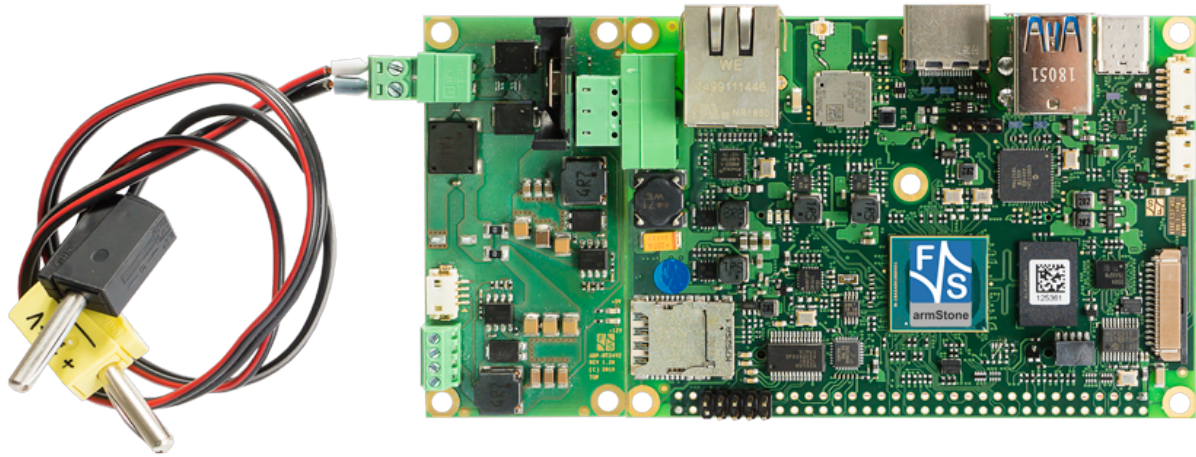


Figure 9: ADP-NT24V2

The extension board is designed to plug it into the power Connector of the armStone.

For more information check the F&S website:

<https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/>

## 8 Electrical characteristic

### 8.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 85°C		0.6	µA
Maximum output current 3.3V		20	mA

Table 17: Absolute Maximum Ratings

### 8.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VIN	Baord main power		4.5	5.5	V
VBAT	RTC power		1.8	3.5	V
OVDD	On board 3.3V DCDC		3.15	3.45	V

$V_{ih}$	High Level Input Voltage		$0.7 \cdot OVDD$	$OVDD$	V
$V_{il}$	Low Level Input Voltage		0	$0.3 \cdot OVDD$	V
$V_{oh}$	High Level Output Voltage	$I_{oh}=0.1mA$	$OVDD-0,15$		V
$V_{ol}$	Low Level Output Voltage	$I_{ol}=0.1mA$		0.15	V
$I_o$	Output current IOs	3.3V		5	mA
$I_{VBAT}$	Current consumption VBAT			0.22	$\mu A$

*Table 18: DC Electrical Characteristics*

*OVDD = power on pin 3.3V from on board DCDC*

## 9 Thermal Specification

	Min	Typ	Max	Unit
Operating temperature	0		+70 <sup>1</sup>	°C
Operating temperature ("I") <sup>2</sup>	-40		+85 <sup>1</sup>	°C
Junction temperature NXP Vybrid	-40		+105	°C

<sup>1</sup> Depending on cooling solution. See also: [Power consumption and cooling](#)

## 10 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to [support@fs-net.de](mailto:support@fs-net.de).

## 11 ESD and EMI implementing on COM

Like all other SBC's at the market there is no ESD protection on any signal out from the SBC. ESD protection has to be placed as near as possible to the ESD source - this is every connector with external access. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the board supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decreases your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

## 12 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

## 13 Power consumption and cooling

Depending on your product version you will have different temperature range and power consumption of the board.

The operating temperature can be measured on the mounting holes on top of the board and **shouldn't exceed the maximum operating temperature of the board (85°C)**.

The maximum power consumption of the board could be **7.5 Watt**. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depending on your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **2** and **6 Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

**Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.**

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- [fischerelektronik.de/web\\_fisch...eKataloge/Heatsinks/#/18/](http://fischerelektronik.de/web_fisch...eKataloge/Heatsinks/#/18/)
- [http://www.eetimes.com/document.asp?doc\\_id=1276748](http://www.eetimes.com/document.asp?doc_id=1276748)
- [http://www.eetimes.com/document.asp?doc\\_id=1276750](http://www.eetimes.com/document.asp?doc_id=1276750)

## 14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months  
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months  
For longer storage we recommend vacuum dry packs.

## 15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

## 16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.  
The boards are shipped in cartons. One carton can hold 30 boards.

## 17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here <https://www.fs-net.de/en/support/serial-number-info-and-rma/> to get information on shipping date and type of board.



Figure 10: Matrix Code Sticker



# 18 Appendix

## Important Notice

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