Hardware Documentation

efus™A7UL
HW Revision 1.20

Version 102
(2021-09-06)

Elektronik Systeme

Untere Waldplätze 23
D-70569 Stuttgart
Phone: +49(0)711-123722-0
Fax: +49(0)711-123722-99

About This Document

This document describes how to use the efus™A7UL board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
12.08.2015	001	All		-	Initial Version	TM
07.03.2016	002	All	M	3.1, 4**Error! Reference source not found.**	Correct Interface and Signal description	TM
04.03.2016	002	All	A	6.1.1	Added note about data retention of SLC NAND flash	HF
04.03.2016	002	All	A	6.2	Added information about eMMC flash memory.	HF
16.06.2016	003	All	A	4.12	Added Chapter Camera	TM
15.08.2016	004	All	M	4.10	Add 24-Bit LCD interface description	TM
15.12.2016	005	All	A	some	Add comments for non-working features	KW
13.11.2017	006	All	A		ESD warning	HF
12.03.2018	100	All	A M	4.9 5.2 5.4 8; 0; 10 13 3.1 5.5 7	Make CTREF more clear, add ETH_B as an option Add some eMMC specification RTC added Review service, general ESD and EMV statement, second source rule and packaging added Add columns for options and revisions, correct some Pullups and pulldowns, add LVDS option WLAN option updated Add some electrical values	KW
12.12.2018	100	All	A	5.5	Added QDID	JG
30.04.2020	101	All	A	1;4;11	Added 18 bit LVDS interface	HF
18.08.2021	102	All	A		Add chapter Power consumption and cooling / Change to new Layout	HF / MW

V	Version
A, M, R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block Diagram

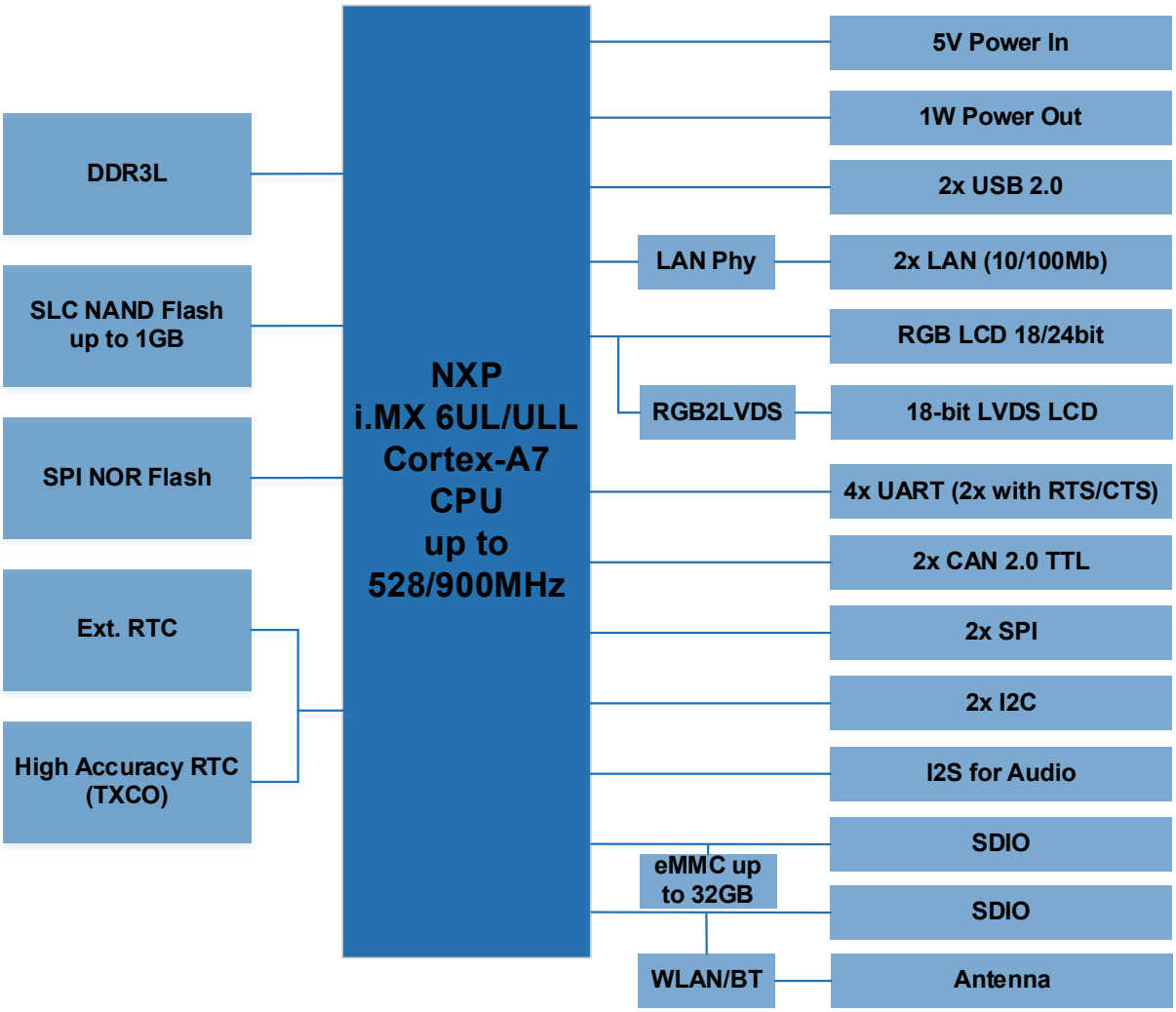

Figure 1: efusA7UL block diagram

2 Mechanical Dimensions

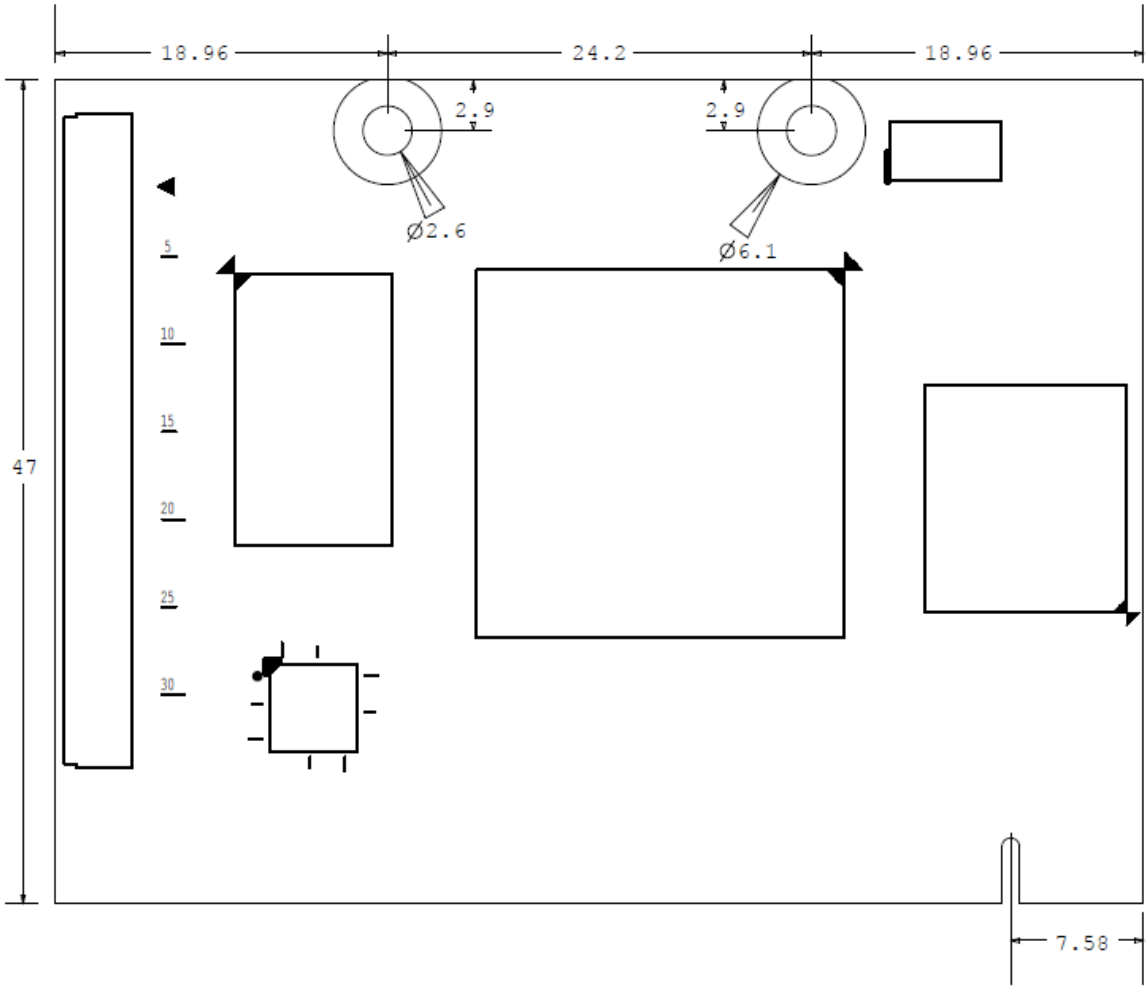

Figure 2: Mechanical Dimensions [mm]

Dimensions	Description
Size	62.1mm x 47mm
PCB Thickness	1.2mm ± 0.1mm
Height of the parts on the top side	5mm
Height of the parts on the bottom side	2mm
Weight	13gr

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Interface and Signal Description

3.1 B2B Connector (J3)

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
1	+5V	V5.0	PWR I	5.0V	Power Supply Input
2	+5V	V5.0	PWR I	5.0V	Power Supply Input
3	+5V	V5.0	PWR I	5.0V	Power Supply Input
4	+5V	V5.0	PWR I	5.0V	Power Supply Input
5	+5V	V5.0	PWR I	5.0V	Power Supply Input
6	+5V	V5.0	PWR I	5.0V	Power Supply Input
7	GND	GND	PWR	GND	
8	GND	GND	PWR	GND	
9	VBAT	VBAT	PWR I	3.0V	2.2 < VBAT < 3.45V
10	V33OUT/V33-ENABLE	V3.3	PWR O	3.3V	Max. 20mA output
11	ACOK	NC	X	X	
12	!RESET_IN	RESET_IN	I		100k PU on 3.3V
13	I0OUT_ADC_IN	NC	X	X	
14	!RESET_OUT	NC	O	3.3V	NC; only supported on boards with WLAN mounted: 10k PU, active low reset for baseboard logic *1*3
15	RXD_C_TTL	CSI_DATA01 / LCD_ENABLE	I	3.3V	*1*2
16	SD_A_WP / NC	UART1_CTS	I	3.3V	*1*2
17	TXD_C_TTL	CSI_DATA00 / LCD_CLK	O	3.3V	*1*2
18	SD_A_CD / NC	UART1_RTS	I	3.3V	*1*2
19	RTS_C_TTL	CSI_DATA03 / LCD_HSYNC	I	3.3V	*1*2*3
20	SD_A_DAT2 / NC	SD1_DAT2	I/O	3.3V	*1*2
21	CTS_C_TTL	CSI_DATA02 / LCD_VSYNC	I	3.3V	*1*2*3
22	SD_A_DAT3 / NC	SD1_DAT3	I/O	3.3V	*1*2
23	NC				
24	SD_A_CMD / NC	SD1_CMD	O	3.3V	10k PullUp *1*2
25	PWM_A	GPIO1_IO05	O		

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
26	SD_A_VCC		PWR	3.3V	3.3V out for SD-Card A
27	GND		PWR		
28	SD_A_CLK / NC	SD1_CLK	O	3.3V	*1*2
29	CAN_A_TX	UART3_CTS	O	3.3V	
30	GND		PWR		
31	CAN_A_RX	UART3_RTS	I	3.3V	
32	SD_A_DAT0 / NC	SD1_DAT0	I/O	3.3V	*1*2
33	GND		PWR		
34	SD_A_DAT1 / NC	SD1_DAT1	I/O	3.3V	*1*2
35	CAN_B_TX	UART2_CTS	O	3.3V	
36	NC				
37	CAN_B_RX	UART2_RTS	I	3.3V	
38	NC				
39	GND		PWR		
40	NC				
41	NC				
42	NC				
43	NC				
44	NC				
45	GND		PWR		
46	GND		PWR		
47	NC				
48	EXT_PROG		I		
49	NC				
50	SPI_B_MISO	UART5_RX_DATA	I	3.3V	
51	GND		PWR		
52	SPI_B_MOSI	UART5_TX_DATA	O	3.3V	
53	NC				
54	SPI_B_SPCK	UART4_TX_DATA	O	3.3V	
55	NC				
56	SPI_B_CS1	UART4_RX_DATA	O	3.3V	
57	GND		PWR		
58	NC				

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
59	NC				
60	SPI_B_IRQ1	SNVS_TAMPER7	I	3.3V	100k PullUp
61	NC				
62	NC				
63	GND		PWR		
64	GND		PWR		
65	SD_B_DAT2 / NC	LCD_DATA22	I/O	3.3V	*1*4
66	SPI_A_MISO	CSI_DATA07	I	3.3V	
67	SD_B_DAT3 / NC	LCD_DATA23	I/O	3.3V	*1*4
68	SPI_A_MOSI	CSI_DATA06	O	3.3V	
69	SD_B_CMD / NC	LCD_DATA18	O	3.3V	*1*4
70	SPI_A_SPCK	CSI_DATA074	O	3.3V	
71	SD_B_VCC		PWR	3.3V	3.3V out for SD-Card B
72	SPI_A_CS1	CSI_DATA075	O	3.3V	
73	SD_B_CLK / NC	LCD_DATA19	O	3.3V	*1*4
74	NC				
75	GND		PWR		
76	SPI_A_IRQ1	SNVS_TAMPER6	I	3.3V	100k Pull-Up
77	SD_B_DAT0 / NC	LCD_DATA20	I/O	3.3V	*1*4
78	NC				
79	SD_B_DAT1 / NC	LCD_DATA21	I/O	3.3V	*1*4
80	GND		PWR		
81	NC (SD_B_WP)	UART1_CTS	I	3.3V	Only available if WLAN is mounted *1*4
82	I2C_B_DAT	CSI_VSYNC	I/O	3.3V	4k7 PullUp
83	NC (SD_B_CD)	UART1_RTS	I	3.3V	Only available if WLAN is mounted *1*4
84	I2C_B_CLK	CSI_HSYNC	O	3.3V	4k7 PullUp
85	GND		PWR		
86	I2C_B_IRQ	SNVS_TAMPER1	I	3.3V	100k PullUp
87	BL_CTRL	GPIO1_IO08	O	3.3V	PWM Backlight dimming
88	I2C_B_RST	SNVS_TAMPER3	O	3.3V	100k PullUp
89	VCFL_ON	SNVS_TAMPER5	O	3.3V	Backlight On
90	GND		PWR		
91	GND		PWR		

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
92	RXD_A_TTL	UART1_RX_DATA	I	3.3V	Debug, 100k pull-up
93	LCD_CLK	LCD_CLK	O	3.3V	
94	TXD_A_TTL	UART1_TX_DATA	O	3.3V	Debug
95	GND		PWR		
96	RXD_D_TTL	CSI_PIXCLK	I	3.3V	
97	LCD_HSYNC	LCD_HSYNC	O	3.3V	
98	TXD_D_TTL	CSI_MCLK	O	3.3V	
99	LCD_VSYNC	LCD_VSYNC	O	3.3V	
100	GND		PWR		
101	GND		PWR		
102	RXD_B_TTL	UART2_RX_DATA	I	3.3V	
103	LCD_R0	LCD_DATA00	O	3.3V	
104	TXD_B_TTL	UART2_TX_DATA	O	3.3V	
105	LCD_R1	LCD_DATA01	O	3.3V	
106	RTS_B_TTL	UART3_TX_DATA	O	3.3V	*3
107	LCD_R2	LCD_DATA02	O	3.3V	
108	CTS_B_TTL	UART3_RX_DATA	I	3.3V	*3
109	LCD_R3	LCD_DATA03	O	3.3V	
110	GND		PWR		
111	LCD_R4	LCD_DATA04	O	3.3V	
112	I2S_MCLK	JTAG_TMS	O	3.3V	
113	LCD_R5	LCD_DATA05	O	3.3V	
114	GND		PWR		
115	GND		PWR		
116	I2S_LRCLK	JTAG_TDO	O	3.3V	
117	LCD_G0	LCD_DATA06	O	3.3V	
118	GND		PWR		
119	LCD_G1	LCD_DATA07	O	3.3V	
120	I2S_SCLK	JTAG_TDI	O	3.3V	
121	LCD_G2	LCD_DATA08	O	3.3V	
122	GND		PWR		
123	LCD_G3	LCD_DATA09	O	3.3V	
124	I2S_DOUT	JTAG_TCK	I	3.3V	*3

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
125	LCD_G4	LCD_DATA10	O	3.3V	
126	I2S_DIN	JTAG_nTRST	O	3.3V	*3
127	LCD_G5	LCD_DATA11	O	3.3V	
128	GND		PWR		
129	GND		PWR		
130	I2C_C_DAT	SNVS_TAMPER8	I/O	3.3V	4k7 PullUp
131	LCD_B0	LCD_DATA12	O	3.3V	
132	I2C_C_CLK	SNVS_TAMPER9	O	3.3V	4k7 PullUp
133	LCD_B1	LCD_DATA13	O	3.3V	
134	NC				
135	LCD_B2	LCD_DATA14	O	3.3V	
136	GND		PWR		
137	LCD_B3	LCD_DATA15	O	3.3V	
138	NC/ LVDS_TX2_DP		I/Odiff		*1
139	LCD_B4	LCD_DATA16	O	3.3V	
140	NC/ LVDS_TX2_DN		I/Odiff		*1
141	LCD_B5	LCD_DATA17	O	3.3V	
142	NC/ LVDS_TX1_DP		I/Odiff		*1
143	GND		PWR		
144	NC/ LVDS_TX1_DN		I/Odiff		*1
145	LCD_DE	LCD_ENABLE	O	3.3V	
146	NC/ LVDS_TX0_DP		I/Odiff		*1
147	GND		PWR		
148	NC/ LVDS_TX0_DN		I/Odiff		*1
149	VLCD_ON	SNVS_TAMPER4	O	3.3V	
150	NC/ LVDS_CLK_DP		I/Odiff		*1
151	I2C_A_DAT	GPIO1_IO03	I/O	3.3V	4k7 PullUp
152	NC/ LVDS_CLK_DN		I/Odiff		*1
153	I2C_A_IRQ	SNVS_TAMPER0	I	3.3V	100k PullUp
154	GND		PWR		
155	I2C_A_CLK	GPIO1_IO02	O	3.3V	4k7 PullUp
156	NC				
157	I2C_A_RST	SNVS_TAMPER2	O	3.3V	100k PullUp

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
158	NC				
159	GND		PWR		
160	GND		PWR		
161	NC				
162	NC				
163	NC				
164	NC				
165	NC				
166	ETH_B_LED_LINK		O	3.3V	
167	NC				
168	NC				
169	NC				
170	NC				
171	NC				
172	GND		PWR		
173	NC				
174	ETH_B_D2_N		I/Odiff		*1
175	NC				
176	ETH_B_D2_P		I/Odiff		*1
177	NC				
178	NC				
179	NC				
180	ETH_B_D1_N		I/Odiff		*1
181	GND		PWR		
182	ETH_B_D1_P		I/Odiff		*1
183	NC				
184	GND		PWR		
185	GND		PWR		
186	CTREF		PWR		LAN transformer voltage, NC at this board
187	NC				
188	NC				
189	NC				
190	NC				

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
191	NC				
192	ETH_A_LED_LINK		O	3.3V	
193	NC				
194	NC				
195	NC				
196	NC				
197	NC				
198	ETH_A_VLEDOUT		PWR	3.3V	3.3V out for LAN LEDs
199	GND		PWR		
200	ETH_A_D2_N		I/Odiff		
201	NC				
202	ETH_A_D2_P		I/Odiff		
203	NC				
204	NC				
205	NC				
206	ETH_A_D1_N		I/Odiff		
207	NC				
208	ETH_A_D1_P		I/Odiff		
209	GND		PWR		
210	GND		PWR		
211	NC				
212	USB_A_PWRON		O	3.3V	10k PullUp, not switchable due pinmux capability
213	NC				
214	USB_A_N	USB_OTG2_DN	I/Odiff		
215	GND		PWR		
216	USB_A_P	USB_OTG2_DP	I/Odiff		
217	USB_DEV_VBUS		I	5.0V	10k PullDown
218	GND		GND		
219	USB_DEV_PWR_ONn	GPIO1_IO04	O	3.3V	100k PullUp
220	NC				
221	USB_DEV_OC	GPIO1_IO01	I	3.3V	
222	NC				
223	USB_DEV_ID	GPIO1_IO00	I	3.3V	

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
224	GND		PWR		
225	USB_DEV_N	USB_OTG_DN	I/Odiff		
226	NC				
227	USB_DEV_P	USB_OTG_DP	I/Odiff		
228	NC				
229	GND		PWR		
230	GND		PWR		

**1 Optional*

**2 Not available if WLAN is mounted*

**3 Comes with HW Rev. 1.20 (NC on older revisions)*

**4 Not available if eMMC is mounted*

Table 2: B2B Connector Pin Layout

4 Interfaces

4.1 Ethernet

On efus™A7UL board by standard there are 2 standard 100MBit Ethernet connections.

We recommend a connector with integrated transformer in short distance (less than 1 inch = 25.4 mm) to the module connector. The RX pair should have a 0.1 inch min. distance to TX pair to avoid crosstalk. The intra pair mismatch of each differential pair should be <10 mil (0.254mm). LED signal is able to drive a 3.3V powered LED with 5mA directly to GND. If Ethernet is not used please leave signals unconnected.

J3 Pin	Signal Name	I/O	Description
208	ETH_A_D1+	I/O	Ethernet 1 TX Lane +
206	ETH_A_D1-	I/O	Ethernet 1 TX Lane -
202	ETH_A_D2+	I/O	Ethernet 1 RX Lane +
200	ETH_A_D2-	I/O	Ethernet 1 RX Lane -
192	ETH_A_LED_ LINK	O	Ethernet 1 Led Link
198	ETH_VLEDOUT	PWR O	Ethernet LEDs Supply Voltage, serial R needed
182	ETH_B_D1+	I/O	Ethernet 2 TX Lane +
180	ETH_B_D1-	I/O	Ethernet 2 TX Lane -
176	ETH_B_D2+	Í/O	Ethernet 2 RX Lane +
174	ETH_B_D2-	I/O	Ethernet 2 RX Lane -
166	ETH_B_LED_LINK	I	Ethernet 2 Led Link
186	ETH_CTREF		Common power pin for LAN transformers, NC on this design, we recommend to connect this pin to common pin of both transformers for compatibility with boards used in future

Table 3: Ethernet Interface

4.2 WLAN and Bluetooth

Starting HW Revision 120 efusA7UL can provide a 802.11b/g/n and BT4.1 + HS “Smart Ready” BLE solution based on QCA9377 chipset with U.FL connector for an external antenna.

The “Letter of Conformity” for this RF functionality is available from our homepage.

The QDID for efusA7UL is 116846.

This component is optional and not mounted in all configurations. Please contact sales to get more information. UART_C is used for onboard Bluetooth if mounted and not available. SD_A is used for onboard WLAN if mounted and not available.

4.3 USB

efus™A7UL provides 1x USB2.0 Host only and 1x USBOTG2.0 connections. The 90 Ohm differential pair of USB signals do not need any termination. For external ports EMV and ESD protection is required nearby the USB connector on the base board. If the USB port is not used please leave open.

J3 Pin	Signal Name	CPU Pin	I/O	Description
212	USB_PWRON		I	USB2.0 Host Power On
214	USB_A_N	USB_OTG2_DN	I/O	USB2.0 Host Data Lane- (in USB2.0 Case)
216	USB_A_P	USB_OTG2_DP	Í/O	USB2.0 Host Data Lane+ (in USB2.0 Case)
217	USB_DEV_VBUS		I/O	USB OTG2.0 Supply Voltage (Input @Device Mode)
219	USB_DEV_PWR_ON	GPIO1_IO04	I	USB OTG2.0 Power On
221	USB_DEV_OC	GPIO1_IO01	O	USB OTG2.0 Over Current Output (active low)
223	USB_DEV_ID	GPIO1_IO00	O	USB OTG2.0 ID
225	USB_DEV_N	USB_OTG1_DN	I/O	USB OTG2.0 Data Lane-
227	USB_DEV_P	USB_OTG1_DP	I/O	USB OTG2.0 Data Lane+

Table 4: USB Interface

4.4 Serial Interfaces

On efus™A7UL board it is allowed for the users to use these serial interfaces, which are given below. All of these serial Interfaces are 3.3V compliant.

- UART: 2 x UART with RTS/CTS and 2 x UART without RTS/CTS
- I2C: 3 x I2C
- SPI: 2 x SPI
- CAN: 2 x CAN Bus

J3 Pin	Signal Name	CPU Pin	I/O	Description
102	RXD_B_TTL	UART2_RX_DATA	I	UART2 Receive Data
104	TXD_B_TTL	UART2_TX_DATA	O	UART2 Transmit Data
106	RTS_B_TTL	UART3_TX_DATA	O	UART2 Request to Send Signal
108	CTS_B_TTL	UART3_RX_DATA	I	UART2 Clear to Send Signal
15	RXD_C_TTL	CSI_DATA01 / LCD_ENABLE	I	UART5 Receive Data
17	TXD_C_TTL	CSI_DATA00 / LCD_CLK	O	UART5 Transmit Data
19	RTS_C_TTL	CSI_DATA03 / LCD_HSYNC	O	UART5 Request to Send Signal
21	CTS_C_TTL	CSI_DATA02 / LCD_VSYNC	I	UART5 Clear to Send Signal
92	RXD_A_TTL	UART1_RX_DATA	I	UART1 Receive Data
94	TXD_A_TTL	UART1_TX_DATA	O	UART1 Transmit Data
96	RXD_D_TTL	CSI_PIXCLK	I	UART6 Receive Data
98	TXD_D_TTL	CSI_MCLK	O	UART6 Transmit Data

Table 5: Serial Interfaces – UART

J3 Pin	Signal Name	CPU Pin	I/O	Description
29	CAN_A_TX	UART3_CTS	O	CAN1 Transmit Data
31	CAN_A_RX	UART3_RTS	I	CAN1 Receive Data
35	CAN_B_TX	UART2_CTS	O	CAN2 Transmit Data
37	CAN_B_RX	UART2_RTS	I	CAN2 Receive Data

**Can transceivers must be placed on Baseboard*

Table 6: Serial Interfaces – CAN

J3 Pin	Signal Name	CPU Pin	I/O	Description
155	I2C_A_CLK	GPIO1_IO02	O	I2C1 Clock Lane
151	I2C_A_DAT	GPIO1_IO03	I/O	I2C1 Data Lane
153	I2C_A_IRQ	SNVS_TAMPER0	I/O	I2C1 Interrupt Signal
157	I2C_A_RST	SNVS_TAMPER2	I	I2C1 Reset Signal
84	I2C_B_CLK	CSI_HSYNC	O	I2C2 Clock Lane
82	I2C_B_DAT	CSI_VSYNC	I/O	I2C2 Data Lane
86	I2C_B_IRQ	SNVS_TAMPER1	I/O	I2C2 Interrupt Signal
88	I2C_B_RST	SNVS_TAMPER3	I	I2C2 Reset Signal
132	I2C_C_CLK	SNVS_TAMPER9	O	I2C3 Clock Lane
130	I2C_C_DAT	SNVS_TAMPER8	I/O	I2C3 Data Lane

Table 7: Serial Interfaces – I2C

I2C2 output is reserved for display control and touch controller for resistive or capacitive touch.

I2C3 output is reserved for DVI DDC, sound codec programming, mPCIe SMB and camera programming. It is shared on the module with RTC I2C signals and the optional on-board I2C EEPROM. We don't recommend to use this signal for other functions.

J3 Pin	Signal Name	CPU Pin	I/O	Description
66	SPI_A_MISO	CSI_DATA07	I	SPI0 Master In Slave Out (Data In)
68	SPI_A_MOSI	CSI_DATA06	O	SPI0 Master Out Slave In (Data Out)
70	SPI_A_SPCK	CSI_DATA04	O	SPI0 Serial Peripheral Clock
72	SPI_A_CS1	CSI_DATA05	O	SPI0 Chip Select 1 (Slave Select 0)
76	SPI_A_IRQ1	SNVS_TAMPER6	I/O	SPI0 Interrupt Flag 1
50	SPI_B_MISO	UART5_RX_DATA	I	SPI3 Master In Slave Out (Data In)
52	SPI_B_MOSI	UART5_TX_DATA	O	SPI3 Master Out Slave In (Data Out)
54	SPI_B_SPCK	UART4_TX_DATA	O	SPI3 Serial Peripheral Clock
56	SPI_B_CS1	UART4_RX_DATA	O	SPI3 Chip Select 1 (Slave Select 0)
60	SPI_B_IRQ1	SNVS_TAMPER7	I/O	SPI3 Interrupt Flag 1

Table 8: Serial Interfaces – SPI

4.5 SD Card

The interface is supporting an SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org. Pullups are not integrated on the module. Unused signals should be left unconnected. SD Interface supply voltage is always 3.3V.

SD_A is only available if WLAN is not mounted.

SD_B is only available if eMMC is not mounted.

J3 Pin	Signal Name	CPU Pin	I/O	Description
32	SD_A_DAT0	SD1_DAT0	I/O	SD Card Interface Data Lane 0
34	SD_A_DAT1	SD1_DAT1	I/O	SD Card Interface Data Lane 1
20	SD_A_DAT2	SD1_DAT2	I/O	SD Card Interface Data Lane 2
22	SD_A_DAT3	SD1_DAT3	I/O	SD Card Interface Data Lane 3
24	SD_A_CMD	SD1_CMD	I	Command Signal
28	SD_A_CLK	SD1_CLK	O	Clock Signal
18	SD_A_CD	UART1_RTS	I	Card Detect Signal
16	SD_A_WP	UART1_CTS	I	Write Protect Signal
26	SD_A_VCC		PWR I	SD Card Interface Supply Voltage 3.3V
77	SD_B_DAT0	LCD_DATA20	I/O	SD Card Interface Data Lane 0
79	SD_B_DAT1	LCD_DATA21	I/O	SD Card Interface Data Lane 1
65	SD_B_DAT2	LCD_DATA22	I/O	SD Card Interface Data Lane 2
67	SD_B_DAT3	LCD_DATA23	I/O	SD Card Interface Data Lane 3
69	SD_B_CMD	LCD_DATA18	I	Command Signal
73	SD_B_CLK	LCD_DATA19	O	Clock Signal
83	SD_B_CD	UART1_RTS	I	Card Detect Signal
81	SD_B_WP	UART1_CTS	I	Write Protect Signal
71	SD_B_VCC		PWR I	SD Card Interface Supply Voltage 3.3V

Table 9: SD Card Interface

4.6 Audio

efus™A7UL board supports SAI Interface (Serial Audio Interface) which is including industry-standard codecs. There are no external audio codecs on this board.

Only supported with HW Rev 1.20 and higher.

J3 Pin	Signal Name	CPU Pin	I/O	Description
126	I2S_DIN	JTAG_nTRST	I	I2S Data In
124	I2S_DOUT	JTAG_TCK	O	I2S Data Out
116	I2S_LRCLK	JTAG_TDO	O	I2S Frame Clock
112	I2S_MCLK	JTAG_TMS	O	I2S System Master Clock
120	I2S_SCLK	JTAG_TDI	O	I2S Bit Clock

Table 10: Audio Interface

4.7 RGB LCD 18bit

Because all signals does work with 3.3V TTL level and high speed, high EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary.

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
87	BL_CTRL	GPIO1_IO08	O	3.3V	3.3V TTL PWM output for Backlight dimming
89	VCFL_ON	SNVS_TAMPER5	O	3.3V	high active Backlight on
93	LCD_CLK	LCD_CLK	O	3.3V	
97	LCD_HSYNC	LCD_HSYNC	O	3.3V	
99	LCD_VSYNC	LCD_VSYNC	O	3.3V	
103	LCD_R0	LCD_DATA00	O	3.3V	
105	LCD_R1	LCD_DATA01	O	3.3V	
107	LCD_R2	LCD_DATA02	O	3.3V	
109	LCD_R3	LCD_DATA03	O	3.3V	
111	LCD_R4	LCD_DATA04	O	3.3V	
113	LCD_R5	LCD_DATA05	O	3.3V	
117	LCD_G0	LCD_DATA06	O	3.3V	
119	LCD_G1	LCD_DATA07	O	3.3V	
121	LCD_G2	LCD_DATA08	O	3.3V	
123	LCD_G3	LCD_DATA09	O	3.3V	
125	LCD_G4	LCD_DATA10	O	3.3V	
127	LCD_G5	LCD_DATA11	O	3.3V	
131	LCD_B0	LCD_DATA12	O	3.3V	
133	LCD_B1	LCD_DATA13	O	3.3V	
135	LCD_B2	LCD_DATA14	O	3.3V	
137	LCD_B3	LCD_DATA15	O	3.3V	
139	LCD_B4	LCD_DATA16	O	3.3V	
141	LCD_B5	LCD_DATA17	O	3.3V	
145	LCD_DE	LCD_ENABLE	O	3.3V	
149	VLCD_ON	SNVS_TAMPER4	O	3.3V	high active LCD power on

Table 11: B2B Connector RGB 18bit Signals Pin Layout

4.8 RGB LCD 24 bit

Because all signals does work with 3.3V TTL level and high speed, high EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary.

efus™A7UL supports a 24-bit LCD interface. SD Card interface B (SD_B) is not available in this mode and only possible if eMMC is not mounted. Needs special SW Support.

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
87	BL_CTRL	GPIO1_IO08	O	3.3V	3.3V TTL PWM output for Backlight dimming
89	VCFL_ON	SNVS_TAMPER5	O	3.3V	high active Backlight on
93	LCD_CLK	LCD_CLK	O	3.3V	
97	LCD_HSYNC	LCD_HSYNC	O	3.3V	
99	LCD_VSYNC	LCD_VSYNC	O	3.3V	
103	LCD_R0	LCD_DATA00	O	3.3V	
105	LCD_R1	LCD_DATA01	O	3.3V	
107	LCD_R2	LCD_DATA02	O	3.3V	
109	LCD_R3	LCD_DATA03	O	3.3V	
111	LCD_R4	LCD_DATA04	O	3.3V	
113	LCD_R5	LCD_DATA05	O	3.3V	
117	LCD_R6	LCD_DATA06	O	3.3V	
119	LCD_R7	LCD_DATA07	O	3.3V	
121	LCD_G0	LCD_DATA08	O	3.3V	
123	LCD_G1	LCD_DATA09	O	3.3V	
125	LCD_G2	LCD_DATA10	O	3.3V	
127	LCD_G3	LCD_DATA11	O	3.3V	
131	LCD_G4	LCD_DATA12	O	3.3V	
133	LCD_G5	LCD_DATA13	O	3.3V	
135	LCD_G6	LCD_DATA14	O	3.3V	
137	LCD_G7	LCD_DATA15	O	3.3V	
139	LCD_B0	LCD_DATA16	O	3.3V	
141	LCD_B1	LCD_DATA17	O	3.3V	
69	LCD_B2	LCD_DATA18	O	3.3V	
73	LCD_B3	LCD_DATA19	O	3.3V	
77	LCD_B4	LCD_DATA20	O	3.3V	
79	LCD_B5	LCD_DATA21	O	3.3V	
65	LCD_B6	LCD_DATA22	O	3.3V	
67	LCD_B7	LCD_DATA23	O	3.3V	

J3 Pin	Signal Name	CPU Pin	I/O	Voltage	Remarks
145	LCD_DE	LCD_ENABLE	O	3.3V	
149	VLCD_ON	SNVS_TAMPER4	O	3.3V	high active LCD power on

Table 12: B2B Connector RGB 24bit Signals Pin Layout

4.9 LVDS / MIPI-DSI

efus™A7UL supports a 3x 6-bit LVDS interface. This functions is a mounting option and not available on all versions of efus™A7UL.
Because all signals are high speed, EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary.

This function is optional.

J3 Pin	Signal Name	I/O	Voltage	Remarks
146	LVDS_DATA0+	I/Odiff		Differential data line
148	LVDS_DATA0-	I/Odiff		
142	LVDS_DATA1+	I/Odiff		Differential data line
144	LVDS_DATA1-	I/Odiff		
138	LVDS_DATA2+	I/Odiff		Differential data line
140	LVDS_DATA2-	I/Odiff		
150	LVDS_CLK+	I/Odiff		Differential data line
152	LVDS_CLK-	I/Odiff		

Table 13: B2B Connector LVDS Signals Pin Layout

4.10 Parallel Camera Interface

Parallel camera signals are shared with other signals (Default Signals) and can´t be used at the same time. Needs special SW support.

J3 Pin	Signal Name	CPU Pin	I/O	Description
17	CAMINT_YDATA00	CSI_DATA00	I	
15	CAMINT_YDATA01	CSI_DATA01	I	
21	CAMINT_YDATA02	CSI_DATA02	I	
19	CAMINT_YDATA03	CSI_DATA03	I	
70	CAMINT_YDATA04	CSI_DATA04	I	
72	CAMINT_YDATA05	CSI_DATA05	I	
68	CAMINT_YDATA06	CSI_DATA06	I	
66	CAMINT_YDATA07	CSI_DATA07	I	
96	CAMINT_PIXCLK	CSI_PIXCLK	O	
98	CAMINT_MCLK	CSI_MCLK	O	Camera System Master Clock
84	CAMINT_HSYNC	CSI_VSYNC	O	Camera Horizontal Sync Signal
84	CAMINT_VSYNC	CSI_HSYNC	O	Camera Vertical Sync Signal

Table 14: Parallel Camera Interface

4.11 Power and Power Control Pins

J3 Pin	Signal Name	I/O	Voltage	Description
1…6	+5V	PWR In	5.0V	Main Power Supply Input Please refer Electrical characteristic
9	VBAT	PWR In	3V	RTC Battery Input, leave open if not used Please refer Electrical characteristic (Ch6)
10	V33OUT / V33_ENABLE	PWR O	3.3V	20mA Output from on module DCDC powered from V5.0
12	!RESET_IN	I	3.3V	Power On Reset Input
26	SD_A_VCC	O	1.8V/3.3V	SD Card Supply Voltage (VCC_LDO_SD1 | V3.3)
134	HDMI_DDC_VOUT	O	3.3V	HDMI/LVDS Supply Voltage
149	VLCD_ON	I	3.3V	LCD Enable
189	CAMINT_VCAM	O	1.8V	Camera Supply Voltage
198	ETH_VLEDOUT	O	3.3V	Ethernet LED Supply Voltage
217	USB_DEV_VBUS	PWR I/O	5.0V	USB (OTG1) Power Supply (Input for Device Mode)
	GND	PWR	GND	Connect all GND pins to a GND plane

Table 15: Power and Power Control Pins

By using a battery for VBAT you have to follow regulation rules. Please check with your test laboratory.

V33OUT/V33_ENABLE is the DCDC power supply of the module powered from V5.0. Use as enable for baseboard power regulators.

!RESET_IN is a Reset Input for the module. Will just reset the CPU.

5 RTC

There is a NXP PCF8563TS or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day. For better accuracy F&S does support a mounting option with TCO. Please ask your sales contact for pricing and minimal order quantity, if you have enhanced requirements.

6 MISC

6.1 NAND Flash

By default, boot mode of efusA7UL is configured for NAND boot.

efusA7UL implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S to be robust against power failures

6.1.1 NAND Flash Data Retention

The NAND Flash is based on “single level cell” (SLC) technology. This technology is ten times more robust compared to “multi level cell” (MLC) technology. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6.2 eMMC Flash

If mounted a eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

If eMMC is mounted SD_B is not available on goldfinger connector and the LCD interface can only run in 18bit mode.

6.2.1 eMMC Flash Data Retention

The eMMC Flash is based on “multi level cell” (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

6.3 SPI NOR Flash

This device can be used for booting. Means you can store boot-loader and boot from this memory. Because selection of boot-medium is done with eFuse you have to order the efusA7UL with the desired boot mode.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

7 Electrical characteristic

7.1 Absolute maximum ratings

Description	Min	Max	Unit
I/O Voltage range for 1.8V IO pins	-0.3	2.1	V
I/O Voltage range for 3.3V IO pins	-0.3	3.6	V
I/O Voltage range for ADC pins	-0.1	2.1	V
USB_DEV_VBUS (USB OTG2.0)	-0.3	5.5	V

Table 16: Absolute Maximum Ratings

7.2 DC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIN	efus™A7UL input supply voltage	4.5	5	5.5	V
I_{IN}	Input Current			1.0	A
VBAT	RTC Power Supply	2.2	3.0	3.45	V
P_{VBAT}	Power Consumption @85°C		0.22	0.6	µA
USB_DEV_VBUS	USB supply voltage	4.4	5.0	5.5	V
I_{VBUS}	USB supply current		100		mA
V_{ih}	High Level Input Voltage	0.7*OVDD	OVDD		V
V_{il}	Low Level Input Voltage	0	0.3*OVDD		V
I_o	Output current IOs		5.0		mA

Table 17: DC Electrical Characteristics

Thermal design power (summary all chips from datasheet)

CPU 528MHz, eMMC, 2xLAN	1.9 W
CPU 900MHz, eMMC, 2xLAN	2.1 W
CPU 900MHz, eMMC, 2xLAN, WLAN	4.6 W

Power consumption of connected devices like display, USB devices, SD card, has to be added for power calculation.

8 Thermal Specification

	Min	Typ.	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MX6ULs	0		+95	°C
Junction temperature CPU (“I”) [2]	-40		+125	°C
Junction to Top of CPU (Psi-JT)[3]		0.1		°C/W

Table 18: Thermal Specifications

Note 1: Maximum junction temperature of the CPU is 105°C. In this case cooling is a necessity and highly recommended. See also: *Power Consumption and Cooling*

Note 2: MIPI to LVDS Bridge can support only -30°C to +85°C. This component is not critical for the booting operation.

Note 3: Life expectancy of the CPU is shortened by high temperatures. Please check NXP AN5337 (https://www.nxp.com/docs/en/application-note/AN5337.pdf)

9 Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

10 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

11 Second Source Rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

12 Power Consumption and Cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **4.0 Watt** (with i.MX6UL). This values are with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **2 Watt to 4 Watt** on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

13 Storage Conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage, we recommend vacuum dry packs.

14 ROHS and REACH Statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

15 Packaging

All F&S ESD-sensitive products will shipping either in trays or in bags.
These modules ship in trays. One tray can hold 10 boards. An empty tray will be used as top cover.

16 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 3: Matrix Code Sticker

17 Appendix

Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme (“F&S”) assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

F&S reserves the right to make changes in its products or product specifications or product documentation with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

F&S makes no warranty or guarantee regarding the suitability of its products for any particular purpose, nor does F&S assume any liability arising out of the documentation or use of any product and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

Products are not designed, intended, or authorized for use as components in systems intended for applications intended to support or sustain life, or for any other application in which the failure of the product from F&S could create a situation where personal injury or death may occur. Should the Buyer purchase or use a F&S product for any such unintended or unauthorized application, the Buyer shall indemnify and hold F&S and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that F&S was negligent regarding the design or manufacture of said product.

Specifications are subject to change without notice.

Warranty Terms

Hardware Warranties

F&S guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and F&S's sole liability shall be for F&S, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Software Warranties

Software is provided "AS IS". F&S makes no warranties, either express or implied, with regard to the software object code or software source code either or with respect to any third party materials or intellectual property obtained from third parties. F&S makes no warranty that the software is useable or fit for any particular purpose. This warranty replaces all other warranties written or unwritten. F&S expressly disclaims any such warranties. In no case shall F&S be liable for any consequential damages.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN PLACE OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL F&S BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL F&S BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE PRODUCT, THE CUSTOMER APPROVES THAT THE F&S PRODUCT, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS

18 Content