Hardware Documentation

efus™A9X
for HW Revision 1.12 and 1.20 and 1.30

efus™A9Xr2
for HW Revision 1.00

Version 260
(2022-10-20)

Elektronik Systeme

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About This Document

This document describes how to use the efus™ start interface board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

Important Note!

The latest PCB version for efusA9X is Version 1.30, for efusA9Xr2 is Version 1.00.

The only difference between these two modules is their Gbit Ethernet PHY's.

efus™A9X → Qualcomm Atheros AR8035

efus™A9Xr2 → Realtek RTL8211F/D

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
02.09.15	0.1	All		-	Initial Version	KW
08.10.15	0.2	All	M	0	Correct JAE connector order number	KW
18.12.15	0.3	All	M,A	4.9	Add second LAN	KW
15.06.16	0.4	All	R	4.4	Remove HDMI	DB
29.08.16	1.0	All	A R A M M A M A A A R A	7 4.12 4.6 2 4.4 11, 15 3.1 5.2 0 4.7 4 4.13	Add missing description pin 25..27, add max. current Remove unsupported MIPI-CSI Add LVDS connector as device on I2C_C Specify height of parts Change WIFI/ SD_A to eMMC/ SD_A for HW 1.20 Add storage, REACH and ROHS statement Correct some PU Add eMMC Add WLAN/ BT Add additional UART options Remove SATA Add	KW
06.09.16	1.0	All	A	17, 0	Added information on ESD Requirements, Packaging and Matrix Code Sticker	JG
19.10.16	1.1	All	A	0	Add U.FL connector option	KW
03.01.17	120	All	A	10	Add information about VLCD max. current	KW
19.10.17	220	All	A	11 0	Add second source rules Add link to the letter of conformity and some additional details	KW
26.03.18	230	All	A,M A	3.1 11, 12, 0	Add LVDS option, correct pin 187 Add RTC, Review service, ESD/ EM	KW
02.08.18	240	All	M	0	Default configuration changed to u.FL	HF
12.12.2018	240	All	A	8	Added QDID	JG
19.08.2022	250	All	A	18	Add efusA9Xr2	MW
17.10.2022	260	All	A	8	Add regulatory statement	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

Table of Contents

1 Block diagram

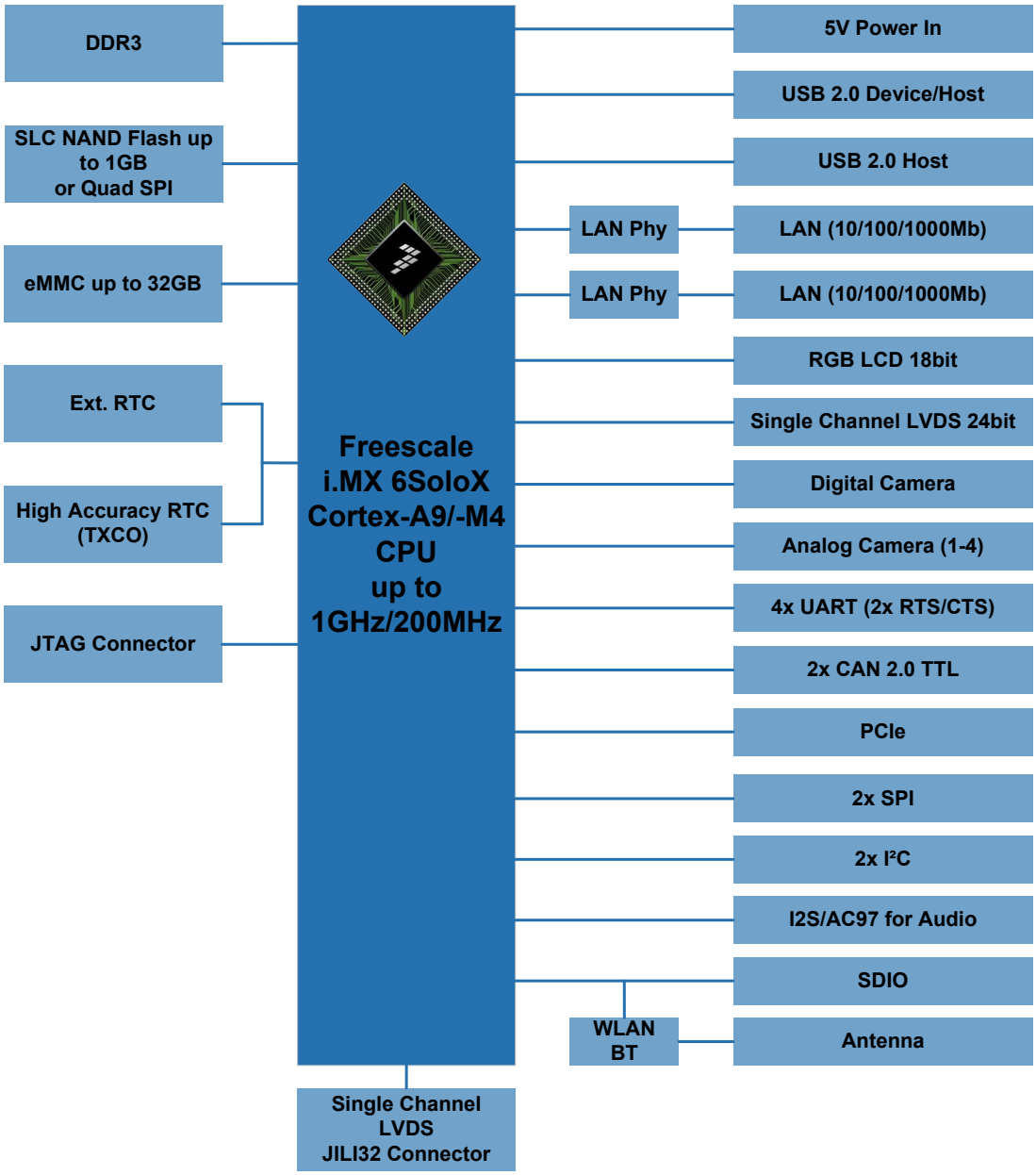


Figure 1: Block diagram

2 Mechanical dimension

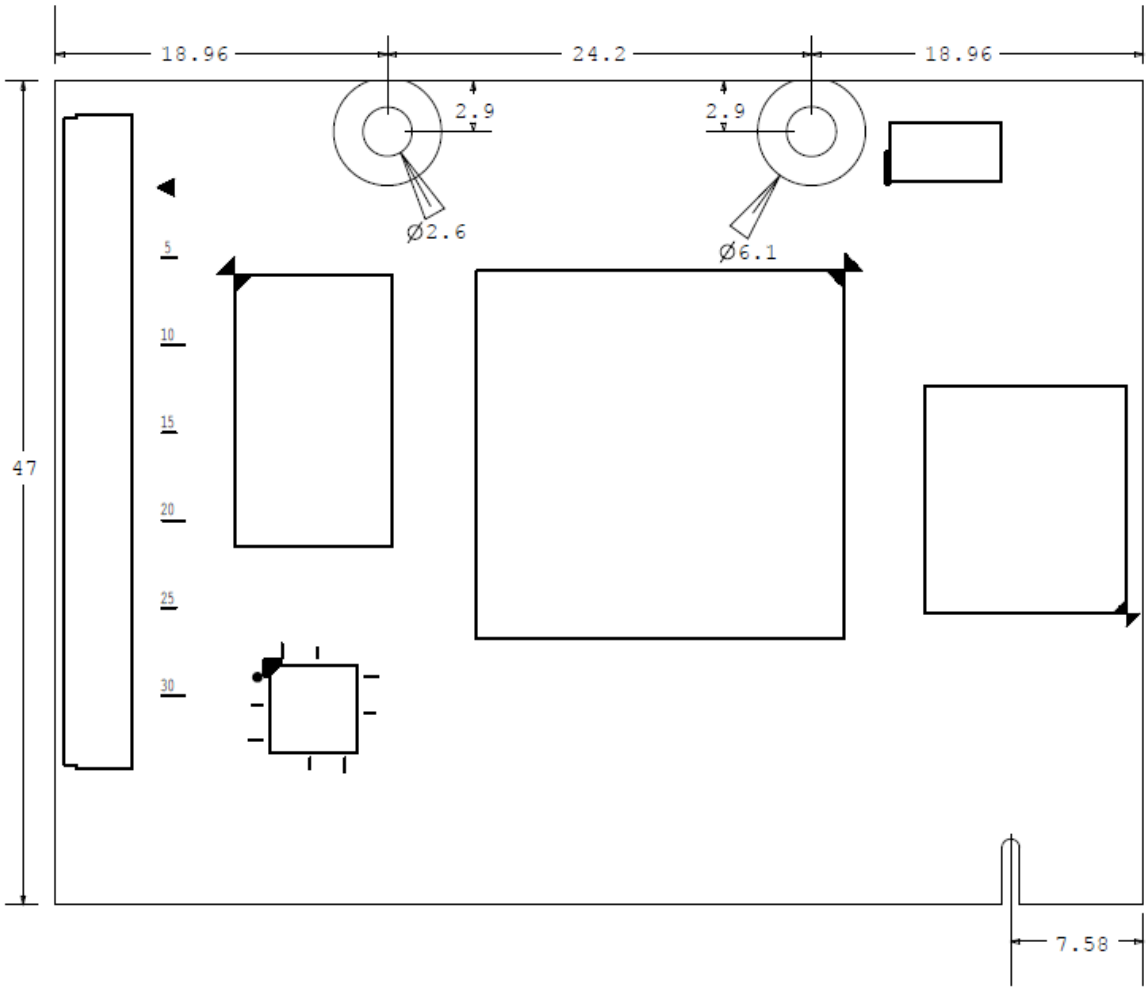


Figure 2: Mechanical dimensions

Size:	62.11mm x 47mm
PCB thickness:	1.2 ± 0.1mm
Height of the parts on the top side:	max. 4.5 mm (except Jtag connector not mounted on mass production)
Height of the parts on the bottom side:	max. 2.0 mm
Weight:	14g

3D Step model available, please contact support@fs-net.de

3 Interface and signal description

3.1 Goldfinger-connector

See also efus start interface documentation for more information.

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
1	+5V Power In	PWR		
2	+5V Power In	PWR		
3	+5V Power In	PWR		
4	+5V Power In	PWR		
5	+5V Power In	PWR		
6	+5V Power In	PWR		
7	GND	PWR		
8	GND	PWR		
9	VBAT In	PWR	RTC battery input	
10	V33-Enable	PWR/ O5	3.3V/100mA out, use as enable for main board 3.3V if more current is required	
11	NC			
12	!RESET_IN	I	3.3V pull-up, drive with OC/OD, 100k PU	
13	NC			
14	!RESET_OUT	O5	4.7k pull down, active low reset for baseboard logic Shared with MPCIE_PERST pin 59	
15	RXD_C_TTL	I*#		
16	SD_A_WP	I*#		X
17	TXD_C_TTL	O5*#		
18	SD_A_CD	I*#		X
19	RTS_C_TTL	O5*#		
20	SD_A_DAT2	I/O*#		X
21	CTS_C_TTL	I*#		
22	SD_A_DAT3	I/O*#		X
23	NC			
24	SD_A_CMD	O5*#		X
25	PWM_A	O5*		
26	SD_A_VCC	PWR	3.3V out for SD-Card A	X

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
27	GND	PWR		
28	SD_A_CLK	O5*#		X
29	CAN_A_TX	O5*		
30	GND	PWR		
31	CAN_A_RX	I*		
32	SD_A_DAT0	I/O*#		X
33	GND	PWR		
34	SD_A_DAT1	I/O *#		X
35	CAN_B_TX	O5*		
36	NC			
37	CAN_B_RX	I*		
38	NC			
39	GND	PWR		
40	NC			
41	MPCIE_CTX_P	Odiff #		
42	NC			
43	MPCIE_CTX_N	Odiff #		
44	NC			
45	GND	PWR		
46	GND	PWR		
47	MPCIE_CRX_P	Idiff #		
48	EXT_PROG			
49	MPCIE_CRX_N	Idiff #		
50	SPI_B_MISO	I*		
51	GND	PWR		
52	SPI_B_MOSI	O5*		
53	MPCIE_CLK_P	Odiff #		
54	SPI_B_SPCK	O5*		
55	MPCIE_CLK_N	Odiff #		
56	SPI_B_CS1	O5*		
57	GND	PWR		
58	SPI_B_CS2	O5*		
59	MPCIE_PERST	O5 #		

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
60	SPI_B_IRQ1	I*	100k pull-up	
61	MPCIE_WAKE	I		
62	SPI_B_IRQ2	I*	100k pull-up	
63	GND	PWR		
64	GND	PWR		
65	SD_B_DAT2	I/O*		
66	SPI_A_MISO	I*		
67	SD_B_DAT3	I/O *		
68	SPI_A_MOSI	O5*		
69	SD_B_CMD	O5*	100k pull-up	
70	SPI_A_SPCK	O5*		
71	SD_B_VCC	PWR	3.3V out for SD-Card B	
72	SPI_A_CS1	O5*		
73	SD_B_CLK	O5*		
74	SPI_A_CS2	O5*		
75	GND	PWR		
76	SPI_A_IRQ1	I*	100k pull-up	
77	SD_B_DAT0	I/O*	100k pull-up	
78	SPI_A_IRQ2	I*	100k pull-up	
79	SD_B_DAT1	I/O*		
80	GND	PWR		
81	SD_B_WP	I*		
82	I2C_B_DAT	I/O*	4.7k pull up	
83	SD_B_CD	I*		
84	I2C_B_CLK	O5*	4.7k pull up	
85	GND	PWR		
86	I2C_B_IRQ	I*	100k pull-up	
87	BL_CTRL	O5*	PWM Backlight dimming	
88	I2C_B_RST	O5*	100k pull-up	
89	VCFL_ON	O5*	Backlight on	
90	GND	PWR		
91	GND	PWR		
92	RXD_A_TTL	I*	Debug, 100k pull-up	

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
93	LCD_CLK	O5*		
94	TXD_A_TTL	O5*	Debug	
95	GND	PWR		
96	RXD_D_TTL	I*		
97	LCD_HSYNC	O5*		
98	TXD_D_TTL	O5*		
99	LCD_VSYNC	O5*		
100	GND	PWR		
101	GND	PWR		
102	RXD_B_TTL	I*		
103	LCD_R0	O5*		
104	TXD_B_TTL	O5*		
105	LCD_R1	O5*		
106	RTS_B_TTL	O5*		
107	LCD_R2	O5*		
108	CTS_B_TTL	I*		
109	LCD_R3	O5*		
110	GND	PWR		
111	LCD_R4	O5*		
112	I2S_MCLK	O5*		
113	LCD_R5	O5*		
114	GND	PWR		
115	GND	PWR		
116	I2S_LRCLK	O5*		
117	LCD_G0	O5*		
118	GND	PWR		
119	LCD_G1	O5*		
120	I2S_SCLK	O5*		
121	LCD_G2	O5*		
122	GND	PWR		
123	LCD_G3	O5*		
124	I2S_DOUT	I*		
125	LCD_G4	O5*		

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
126	I2S_DIN	O5*		
127	LCD_G5	O5*		
128	GND	PWR		
129	GND	PWR		
130	I2C_C_DAT	I/O	4.7k pull up	
131	LCD_B0	O5*		
132	I2C_C_CLK	I/O	4.7k pull up	
133	LCD_B1	O5*		
134	DVI_DDC_VOUT	PWR	3.3V output for DDC	
135	LCD_B2	O5*		
136	GND	PWR		
137	LCD_B3	O5*		
138	NC		LVDS_TX2_DP available on a special version with minimum order quantity	X
139	LCD_B4	O5*		
140	NC		LVDS_TX2_DN available on a special version with minimum order quantity	X
141	LCD_B5	O5*		
142	NC		LVDS_TX1_DP available on a special version with minimum order quantity	X
143	GND	PWR		
144	NC		LVDS_TX1_DN available on a special version with minimum order quantity	X
145	LCD_DE	O5*		
146	NC		LVDS_TX0_DP available on a special version with minimum order quantity	X
147	GND	PWR		
148	NC		LVDS_TX0_DN available on a special version with minimum order quantity	X
149	VLCD_ON	O5*		
150	NC		LVDS_CLK_DP available on a special version with minimum order quantity	X
151	I2C_A_DAT	I/O*	4.7k pull up	
152	NC		LVDS_CLK_DN available on a special version with minimum order quantity	X
153	I2C_A_IRQ	I*	100k pull up	
154	NC		LVDS_TX3_DP available on a special version with minimum order quantity	X
155	I2C_A_CLK	O5*	4.7k pull up	

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
156	NC		LVDS_TX3_DN available on a special version with minimum order quantity	
157	I2C_A_RST	O5*	100k pull up	
158	NC			
159	GND	PWR		
160	GND	PWR		
161	CAM_YDATA0	#	optional parallel camera signal	
162	ETH_B_D4_N	I/Odiff		
163	CAM_YDATA1	#	optional parallel camera signal	
164	ETH_B_D4_P	I/Odiff		
165	CAM_YDATA4	I/O(*)	parallel camera signal	
166	ETH_B_LED_ACT	O5	LINK/ACT (on with link, blinking with activity)	
167	CAM_YDATA3	I/O(*)	parallel camera signal	
168	ETH_B_D3_N	I/Odiff		
169	CAM_YDATA5	I/O(*)	parallel camera signal	
170	ETH_B_D3_P	I/Odiff		
171	CAM_YDATA2	I/O(*)	parallel camera signal	
172	GND			
173	CAM_YDATA6	I/O(*)	parallel camera signal	
174	ETH_B_D2_N	I/Odiff		
175	CAM_PCLK	I/O(*)	parallel camera signal	
176	ETH_B_D2_P	I/Odiff		
177	CAM_YDATA7	I/O(*)	parallel camera signal	
178	ETH_B_LED_LINK	PWR	LINK LED at 1GB Speed	
179	CAM_YDATA8	I/O(*)	parallel camera signal	
180	ETH_B_D1_N	I/Odiff		
181	GND	PWR		
182	ETH_B_D1_P	I/Odiff		
183	CAM_MCLK	I/O*	parallel camera signal	X
184	GND	PWR		
185	GND	PWR		
186	ETH_CTREF	PWR	NC with efusA9 Phy	
187	CAM_YDATA9	I/O(*)	parallel camera signal	
188	ETH_A_D4_N	I/Odiff		

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
189	CAM_VCAM	PWR	Camera interface voltage out (default 2.8V) Other voltages on request	
190	ETH_A_D4_P	I/Odiff		
191	CAM_HREF	I/O(*)	parallel camera signal	X
192	ETH_A_LED_ACT	O5	LINK/ACT (on with link, blinking with activity)	
193	CAM_PWDN		parallel camera signal	
194	ETH_A_D3_N	I/Odiff		
195	CAM_VSYNC	I/O(*)	parallel camera signal	
196	ETH_A_D3_P	I/Odiff		
197	I2C_C_CAMRST	I/O(*)		
198	ETH_A_VLEDOUT	PWR	3.3V out for LAN LEDs	
199	GND	PWR		
200	ETH_A_D2_N	I/Odiff		
201	NC			
202	ETH_A_D2_P	I/Odiff		
203	NC			
204	ETH_A_LED_LINK	PWR	LINK LED at 1GB Speed	
205	NC			
206	ETH_A_D1_N	I/Odiff		
207	NC			
208	ETH_A_D1_P	I/Odiff		
209	GND	PWR		
210	GND	PWR		
211	CAM_A_IN	Analog	Analog Camera In	
212	USB_A_PWRON	O5		
213	CAM_A_GND	Analog	Analog Camera Ground	
214	USB_A_N	I/Odiff		
215	GND	PWR		
216	USB_A_P	I/Odiff		
217	USB_DEV_VBUS	I	4.6 … 5.2V does detect connected USB device	
218	GND	PWR		
219	USB_DEV_PWR_ONn	O5		

J1				
Pin	**Use on base board**	**I/O**	**Remarks; onboard pullups**	**1.12-> 1.20 change**
220	NC			
221	USB_DEV_OC	I*		
222	NC			
223	USB_DEV_ID	I	100k pull up	
224	GND	PWR		
225	USB_DEV_N	I/Odiff		
226	NC			
227	USB_DEV_P	I/Odiff		
228	NC			
229	GND	PWR		
230	GND	PWR		

Table 1: 230 pin goldfinger connector

O5:	3.3V 5mA logic output
I:	3.3V logic input
Idiff, Odiff, I/Odiff:	differential signal
PWR:	Power input or output
*:	SW configurable as GPIO; 3.3V logic level
(*):	2.8V logic level, SW configurable as GPIO; driving 3.3V logic level on this pin will destroy CPU!
#:	not available in all mounting options
X at column 1.12->1.20 change:	CPU IO pin is changed for this function. Only supported with SW built for HW Rev 1.20

4 Interfaces

4.1 USB host

The 90 Ohm differential pair of USB signals doesn't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

212	USB_A_PWRON	High active USB port power on signal
214	USB_A_N	Differential USB Signal
216	USB_A_P	

4.2 USB device

The 90 Ohm differential pair of USB signals don't need any termination. For external ports ESD and EMV protection is required nearby the USB connector.

217	USB_DEV_VBUS	4.6 … 5.2V does detect connected USB device Connect with pin 1 on USB device connector
219	USB_DEV_PWR_ONn	Low active USB port power on signal Used in OTG mode only
221	USB_DEV_OC	Overcurrent Input signal
223	USB_DEV_ID	OTG ID signal input
225	USB_DEV_N	Differential USB Signal
227	USB_DEV_P	

4.3 CAN Bus

The chip does provide the CAN bus transmit and receive TTL signal without any termination.

Needs a interface chip to the CAN bus. If not used, please left signals unconnected.

29	CAN_A_TX	CAN port A TX out
31	CAN_A_RX	CAN port A RX in
35	CAN_B_TX	CAN port B TX out
37	CAN_B_RX	CAN port B RX in

4.4 SD/MMC card

The interface is supporting a SD card channel. For specification and licensing please refer the website of the SD Association http://www.sdcard.org.

Unused signals should be left unconnected.

No.	Name	Description	Onboard PU
16	SD_A_WP	SD card A write protect input	
18	SD_A_CD	SD card A card low active detect input	
20	SD_A_DAT2	SD card A data signal	
22	SD_A_DAT3	SD card A data signal	
24	SD_A_CMD	SD card A command signal	
26	SD_A_VCC	SD card A power out	
28	SD_A_CLK	SD card A clock signal	
32	SD_A_DAT0	SD card A data signal	
34	SD_A_DAT1	SD card A data signal	
81	SD_B_WP	SD card B write protect input	
83	SD_B_CD	SD card B card low active detect input	
65	SD_B_DAT2	SD card B data signal	
67	SD_B_DAT3	SD card B data signal	
69	SD_B_CMD	SD card B command signal	100k pull-up
71	SD_B_VCC	SD card B power out	
73	SD_B_CLK	SD card B clock signal	
77	SD_B_DAT0	SD card B data signal	100k pull-up
79	SD_B_DAT1	SD card B data signal	

SD_A card signals are shared with WLAN at HW Rev 1.12.
If WLAN is mounted SD_A is not available.
SD_A card signals are shared with eMMC at HW Rev 1.20 and later.
If eMMC is mounted SD_A is not available.

4.5 SPI

The module support 2 HS SPI (Serial Peripheral Interface) with 2 chip selects and 2 interrupt inputs. All signals are 3.3V compliant and do have pull-up on module. Devices on baseboard with other voltage need a level shifter.

No	Name	Description	Onboard PU
50	SPI_B_MISO	SPI port B MISO	
52	SPI_B_MOSI	SPI port B MOSI	
54	SPI_B_SPCK	SPI port B Clock	
56	SPI_B_CS1	SPI port B chip select 1 output	
58	SPI_B_CS2	SPI port B chip select 2 output	
60	SPI_B_IRQ1	SPI port B interrupt 1 input	100k
62	SPI_B_IRQ2	SPI port B interrupt 1 input	100k
66	SPI_A_MISO	SPI port A MISO	
68	SPI_A_MOSI	SPI port A MOSI	
70	SPI_A_SPCK	SPI port A Clock	
72	SPI_A_CS1	SPI port A chip select 1 output	
74	SPI_A_CS2	SPI port A chip select 2 output	
76	SPI_A_IRQ1	SPI port A interrupt 1 input	100k
78	SPI_A_IRQ2	SPI port A interrupt 1 input	100k

4.6 I2C

The module supports a I2C interface as I2C master. Signals are 3.3V compliant and do have pull-up on module. Devices on baseboard with other voltage need a level shifter.

82	I2C_B_DAT	Data signal	4k7 PU onboard
84	I2C_B_CLK	Clock signal	4k7 PU onboard
86	I2C_B_IRQ	Optional interrupt input	100k PU onboard
88	I2C_B_RST	Optional reset output	100k PU onboard

A second I2C output is reserved for display control and a touch controller for resistive or capacitive touch.

151	I2C_A_DAT	Data signal for touch controller	4k7 PU onboard
155	I2C_A_CLK	Clock signal for touch controller	4k7 PU onboard
153	I2C_A_IRQ	Interrupt input for touch controller	100k PU onboard
157	I2C_A_RST	Reset output for touch controller	100k PU onboard

A third I2C output is reserved for DVI DDC, sound codec programming, mPCIe SMB and camera programming.

It is shared on the module with RTC I2C signals, the I2C on the LVDS connector and the optional on-board I2C EEProm.

We don’t recommend to use this signal for other functions.

130	I2C_C_DAT	Data signal	4k7 PU onboard
132	I2C_C_CLK	Clock signal	4k7 PU onboard

4.7 Serial ports

92	RXD_A_TTL	UART A RX, Debug interface, 100k pull-up onboard
94	TXD_A_TTL	UART A TX, Debug interface
102	RXD_B_TTL	UART B RX
104	TXD_B_TTL	UART B TX
106	RTS_B_TTL	UART B RTS
108	CTS_B_TTL	UART B CTS
15	RXD_C_TTL *	UART C RX *n/a with on board WLAN/BT
17	TXD_C_TTL *	UART C TX * n/a with on board WLAN/BT
19	RTS_C_TTL *	UART C RTS * n/a with on board WLAN/BT
21	CTS_C_TTL *	UART C CTS * n/a with on board WLAN/BT
96	RXD_D_TTL	UART D RX
98	TXD_D_TTL	UART D TX
76	*RTS_D_TTL*	*UART D RTS (default: SPI_A_IRQ1)*
78	*CTS_D_TTL*	*UART D CTS (default: SPI_A_IRQ2)*
126	*RXD_E_TTL*	*UART E RX (default: I2S_DIN)*
86	*TXD_E_TTL*	*UART E TX (default: I2C_B_IRQ)*
153	*RTS_E_TTL*	*UART E RTS (default: I2C_A_IRQ)*
116	*CTS_E_TTL*	*UART E CTS (default: I2S_LRCLK)*
81	*RXD_F_TTL*	*UART F RX (default: SD_B_WP)*
83	*TXD_F_TTL*	*UART F TX (default: SD_B_CD)*

We recommend to use UART_A for debugging and service only.

UART_E, UART_F and UART_D control are pin sharing options and need special software support. This functionality is not available on other efus boards and is not available on F&S evaluation baseboards.

*** UART_C is used for onboard Bluetooth if WLAN/BT is mounted and not available**

4.8 I2S audio codec interface

The module supports a I2S sound codec.

112	I2S_MCLK	System master clock
116	I2S_LRCLK	I2S frame clock
120	I2S_SCLK	I2S bit clock
124	I2S_DOUT	I2S data output
126	I2S_DIN	I2S data input
130	I2C_C_DAT	Data control signal (shared)
132	I2C_C_CLK	Clock control signal (shared)

4.9 Ethernet

The module supports 2 10/100/1000 Mbit LAN interfaces.

The only difference between these two modules is their Gbit Ethernet PHY's.

efus™A9X → Qualcomm Atheros AR8035

efus™A9Xr2 → Realtek RTL8211F/D

186	ETH_CTREF	Common power pin for both LAN transformer
188	ETH_A_D4_N	Differential data line
190	ETH_A_D4_P	
192	ETH_A_LED_ACT	LINK/ACT (on with link, blinking with activity), serial R needed
194	ETH_A_D3_N	Differential data line
196	ETH_A_D3_P	
198	ETH_A_VLEDOUT	3.3V out for LAN LEDs anode, use for both LAN ports
200	ETH_A_D2_N	Differential data line
202	ETH_A_D2_P	
204	ETH_A_LED_LINK	LINK LED at 1GB Speed, serial R needed
206	ETH_A_D1_N	Differential data line
208	ETH_A_D1_P	
162	ETH_B_D4_N	Differential data line
164	ETH_B_D4_P	
166	ETH_B_LED_ACT	LINK/ACT (on with link, blinking with activity), serial R needed
168	ETH_B_D3_N	Differential data line
170	ETH_B_D3_P	
174	ETH_B_D2_N	Differential data line
176	ETH_B_D2_P	
178	ETH_B_LED_LINK	LINK LED at 1GB Speed, serial R needed
180	ETH_B_D1_N	Differential data line
182	ETH_B_D1_P	

Note: Don't use baseboard power supply for LEDs because power sequencing is needed. Efus provide LED power on goldfinger pin 198.

4.10 PCIe

A single lane PCI Express port (Gen 2.0) is supported.

Please following design rules from PCI-SIG on your design.

41	MPCIE_CTX_P	PCIe transmit differential pair
43	MPCIE_CTX_N	
47	MPCIE_CRX_P	PCIe receive differential pair
49	MPCIE_CRX_N	
53	MPCIE_CLK_P	PCIe clock differential pair
55	MPCIE_CLK_N	
59	MPCIE_PERST	PCIe Reset out
61	MPCIE_WAKE	PCIe wake input

4.11 RGB LCD

87	BL_CTRL	3.3V CMOS PWM output for Backlight dimming
89	VCFL_ON	CMOS 3.3V high active Backlight on
93	LCD_CLK	RGB LCD clock
97	LCD_HSYNC	RGB LCD HSYNC
99	LCD_VSYNC	RGB LCD VSYNC
103	LCD_R0	Red0
105	LCD_R1	Red1
107	LCD_R2	Red2
109	LCD_R3	Red3
111	LCD_R4	Red4
113	LCD_R5	Red5
117	LCD_G0	Green0
119	LCD_G1	Green1
121	LCD_G2	Green2
123	LCD_G3	Green3
125	LCD_G4	Green4
127	LCD_G5	Green5
131	LCD_B0	Blue0
133	LCD_B1	Blue1
135	LCD_B2	Blue2
137	LCD_B3	Blue3
139	LCD_B4	Blue4
141	LCD_B5	Blue5
145	LCD_DE	Data enable
149	VLCD_ON	CMOS 3.3V high active LCD power on

Because all signals does work with 3.3V TTL level and high speed, high EMI radiation will be generated. Signals should be routed as short as possible and shielding is necessary.

Please also refer the efus design guide for connecting displays with more color bits.

4.12 Parallel Camera (CSI)

Note: because an HW failure this pinout is just working HW Revision ≥1.20!

161	n.a./ CAM_YDATA0	I (2.8V) *	CPU pad QSPI1A_SS0
163	n.a./ CAM_YDATA1	I (2.8V) *	CPU pad QSPI1A_SCLK
165	CAM_YDATA4	I (2.8V)	CPU pad CSI_DATA02
167	CAM_YDATA3	I (2.8V)	CPU pad CSI_DATA01
169	CAM_YDATA5	I (2.8V)	CPU pad CSI_DATA03
171	CAM_YDATA2	I (2.8V)	CPU pad CSI_DATA00
173	CAM_YDATA6	I (2.8V)	CPU pad CSI_DATA04
175	CAM_PCLK	I (2.8V)	CPU pad CSI_PIXCLK
177	CAM_YDATA7	I (2.8V)	CPU pad CSI_DATA05
179	CAM_YDATA8	I (2.8V)	CPU pad CSI_DATA06
187	CAM_YDATA9	I (2.8V)	CPU pad CSI_DATA07
183	CAM_MCLK	O (2.8V)	CPU pad CSI_MCLK we recommend oscillator on baseboard as MCLK source for camera
189	CAM_VCAM	PWR	Camera interface voltage out (2.8V)
191	CAM_HREF	I (2.8V)	CPU pad CSI_HSYNC
195	CAM_VSYNC	I (2.8V)	CPU pad CSI_VSYNC
193	CAM_PWDN	O (2.8V)	High active powerdown signal
197	CAMRST	O (2.8V)	High active reset signal
130	I2C_C_DAT	I/O (3.3V)	Data signal, 4k7 PU onboard
132	I2C_C_CLK	O (3.3V)	Clock signal, 4k7 PU onboard

* : this signals are shared with SPI_B and are just available at a mounting option.

In case of using SPI_B just a 8bit parallel camera interface with YDATA2…9 is available.

Just leave LSBs on camera unconnected at standard mounting option.

For more information please also refer i.MX6SoloX documentation from www.nxp.com

4.13 Analog Video In

211	CAM_A_IN	Analog video input 50Ω (NTSC/ PAL)
213	CAM_A_GND	Analog Ground for Video Input
207	CAM2_A_IN *	2nd Analog video input 50Ω (NTSC/ PAL)
205	CAM3_A_IN *	3th Analog video input 50Ω (NTSC/ PAL)
201	CAM4_A_IN *	4th Analog video input 50Ω (NTSC/ PAL)

*: optional, not available on all mounting versions

4.14 MISC

10	V33-Enable	3.3V/100mA Vout, use as enable for main board 3.3V regulator if more current is required
11	ACOK	USB OTG charge detect, future use
12	!RESET_IN	3.3V 100k pull-up on module drives with OC/OD to GND. Leave open if not used.
14	!RESET_OUT	4.7k pull down, active low reset for baseboard logic
25	PWM_A	3.3V TTL level PWM output

5 Flash

5.1 NAND Flash

By default, boot mode of efusA9 is configured for NAND boot.

efusA9X implements the following to get reliable boot over long time:

- Use of SLC NAND flash memory
- Boot loader stored two times in flash memory
- Flash data protected by 32 bit ECC
- Algorithm for block refresh
- Operating system Linux uses UBI as file system
- Operating system Windows can use F3S to be robust against power failures

5.2 eMMC

If mounted a eMMC v4.41 or higher with 4GB or more is mounted from several manufacturer.

This component is optional and not mounted in all configurations. Please contact sales to get more information.
If eMMC is mounted, SD_A port is not available on goldfinger.

The eMMC Flash is based on “multi level cell” (MLC) technology. This technology has limited erase cycles and data retention depends on temperature. It is important to know, that high temperature impacts data retention of SLC or MLC flash. Independent if the device is powered or not. Please contact us, if your device is constantly in an environment where temperature is higher than 50°C.

5.3 SPI NOR Flash

This device can be used for booting. Means you can store boot-loader and boot from this memory. Because selection of boot-medium is done with eFuse you have to order the efusA9 with the desired boot mode.

This component is optional and not mounted in all configurations. Please contact sales to get more information.

5.4 I2C EEPROM

This component is optional and not mounted in all configurations. Please contact sales to get more information.

6 Power

+5V Power In	VCC in, 5V +/-5%
GND	GND, connect all GND pins to GND plane
VBAT In	RTC battery input. Leave open if not used
V33-Enable	3.3V/max. 100mA Vout use as enable for main board 3.3V regulator if more current is required
VLCD (on LVDS connector)	3.3V/max. 300mA Vout use as enable for external regulator if more current is required

7 LVDS-connector

The LVDS display port can be direct connected to a LVDS 18 or 24 bit single channel. Display is independent from RGB LCD.

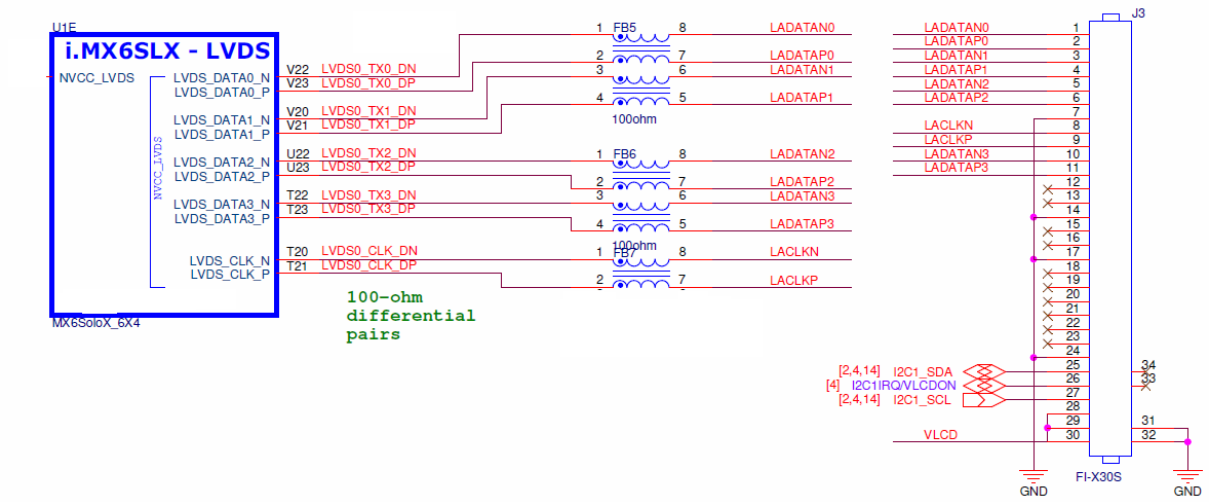
JILI30 JAE FI-X30SSLA Connector or compatible		*GF pin option*
Pin	Function	
28..30	VLCD (3.3V or 5V software configurable, max. 300mA)	-
7,14,17,24	GND	
1	LVDS0_DATA0-	*148*
2	LVDS0_DATA0+	*146*
3	LVDS0_DATA1-	*144*
4	LVDS0_DATA1+	*142*
5	LVDS0_DATA2-	*140*
6	LVDS0_DATA2+	*138*
8	LVDS0_CLK-	*152*
9	LVDS0_CLK+	*150*
10	LVDS0_DATA3- (24bit only)	*156*
11	LVDS0_DATA3+ (24bit only)	*154*
12,13,15,16,18-23	n.c. (second channel not available at efusA9X)	
25	I2C_C_DAT (4k7 PU onboard)	*(130)*
26	VLCDON/ I2C_C_IRQ (TTL 3.3V) (I2C_C_IRQ not supported at HW ≤ Rev 1.12; IO is changed in Rev 1.20)	
27	I2C_C_CLK (4k7 PU onboard)	*(132)*

Table 2: JILI30 LVDS connector

As special mounting option LVDS signals are available on goldfinger connector instead the JILI30. This needs a special mounting option. This function is not available on F&S evaluation baseboards. Please contact our sales and support for further details.

7.1 LVDS EMI filtering

The following schematic shows the internal connection of LVDS signals between connector and CPU. The common mode chokes are TDK MCZ2010CH240L4T, Panasonic EXC-28CG240U or equivalent parts.



8 WLAN/ BT

Starting HW Revision 1.20 efusA9X can provide a 802.11b/g/n/ac and BT4.1 + HS “Smart Ready” BLE solution based on QCA9377 chipset with U.FL connector for an external antenna on module.

The “Letter of Conformity” for this RF functionality excluding 802.11ac is available from our homepage. Our pre-approval is just re-usable by using the antennas listed on this letter.

In a customized version with minimum order quantity a GHz chip antenna for an external antenna can be mounted instead the U.FL connector.

Information about Bluetooth (QDID):

Please refer to the following BT QDID for efusA9X/efusA9Xr2:

QDID: 116846 (Controller Sybsystem)

https://launchstudio.bluetooth.com/ListingDetails/66528

If Bluez-5.37 will be used, the QDID from NXP can be used

https://launchstudio.bluetooth.com/ListingDetails/92249

Customer can use this QDIDs to create their device QDID.

Note: This component is optional and not mounted in all configurations. Please contact sales to get more information.

Note: If WLAN/BT module is mounted, UART_C is not available on efus B2B connector. UART-C is used for Bluetooth interface.

8.1 FCC Certification

This modular complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is only authorized for use in a mobile application. At least 20 cm of separation distance between the module and the user's body must be maintained at all times.

8.1.1 Instructions to Integrator

Labelling

A label must be affixed to the outside of final commercial product with the following statements:

This device contains FCC ID: 2A8IP-efusA9X

Antenna

The antenna gain of a new antenna should be of the same type as the originally approved antenna and the antenna gain should not be higher than the antenna gain of the originally tested antenna. The list of originally approved PCB antennas is the following:

- Type of antenna: 2.4/5GHz Multilayer Monopole Antenna

- P/N: AH104N2450D1
- Peak gain: 2.1 dBi (2.4GHz), 2.4 dBi (5GHz)

RF exposure considerations

Consistent with §2.909(a), the following text must be included within the user's manual or operator instruction guide for the final commercial product:

> This modular complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
> This device is only authorized for use in a mobile application. At least 20 cm of separation distance between the module and the user's body must be maintained at all times.

Additional testing, Part 15 Subpart B disclaimer

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device. The FCC Part 15 Statement shall be included in the user manual of final commercial product if applicable.

Caution Statement for Modifications

Following text must be included within the user's manual or operator instruction guide for the final commercial product:

> CAUTION: Any changes or modifications not expressly approved could void the user's authority to operate the equipment.

9 RTC

There is a NXP PCF8563TS or compatible implemented on board. The accuracy is limited because the warming of the crystal on the board in operation. The RTC could drift some seconds per day. For better accuracy F&S does support a mounting option with XTCO. Please ask your sales contact for pricing and minimal order quantity, if you have enhanced requirements.

Optional a temperature compensated XTCO is available. Please contact your sales contact for minimum order quantity, price and technical specification.

10 Electrical characteristic

VCC: 5V +/- 5%

VBAT In for RTC: 2.2 … 3.45V

power consumption

typical current consumption BATT: 3 µA

maximum power consumption BATT: 10 µA @25°C

Thermal design power (summary all chips)

With 1GHz SoloX CPU 5.5 Watt @25°C

Additional with Wifi mounted +1.6 Watt @25°C

Maximum output current VLCD 500 mA

Maximum output current V33-Enable 100 mA

Power consumption of connected devices like display, USB devices, SD card, miniPCIe card has to be added for power calculation.

Real power consumption could be much lower depends CPU workload, used graphic interfaces and features and the workload on I/O interfaces.

10.1 Absolute maximum ratings

Description	Condition	Min	Max	Unit
Input Voltage range 3.3V IO pins		-0.3	OVDD+0.3	V
USB VBUS (goldfinger pin 217)		-0.3	5.25	V

Table 3: maximum ratings

10.2 DC electrical characteristics for 3.3V IO pins

Parameter	Description	Condition	Min	Max	Unit
OVDD	On module 3.3V DCDC		3.15	3.45	V
Vih	High Level Input Voltage		0.7*OVDD	OVDD	V
Vil	Low Level Input Voltage		0	0.3*OVDD	V
Voh	High Level Output Voltage	Ioh=0.1mA	2.98		V
Vol	Low Level Output Voltage	Iol=0.1mA		0.15	V
Io	Output current			5	mA

OVDD = power on pin V33-Enable (pin 10 goldfinger connector)

Table 4: DC electrical characteristics

11 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

12 ESD and EMI implementing on COM

Like all other COM modules at the market there is no ESD protection on any signal out from the COM module. ESD protection hast to place as near as possible to the ESD source - this is the connector with external access on the COM baseboard. A helpful guide is available from TI; just search for slva680 at ti.com.

To reduce EMI the module supports spread spectrum. This will normally reduce EMI between 9 and 12 dB and so this decrease your shielding requirements. We strictly recommend having your baseboard with controlled impedance and wires as short as possible.

13 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

14 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

15 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

16 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
efus™ modules are shipped in trays. One tray can hold 10 boards. An empty tray is used as top cover.

Figure 3: Tray for shipment

17 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 4: Matrix code lable

18 Differences efusA9X vs efusA9Xr2

The difference between efusA9X and efusA9Xr2 is the Ethernet Phy.

efusA9X	Qualcomm	AR8035-AL1
efusA9Xr2	Realtek	RTL8211FD

Both Phys are Gbit Phys and are connected by RGMII interface to CPU. All frequencies are the same.

In the below picture we marked the area with changes.

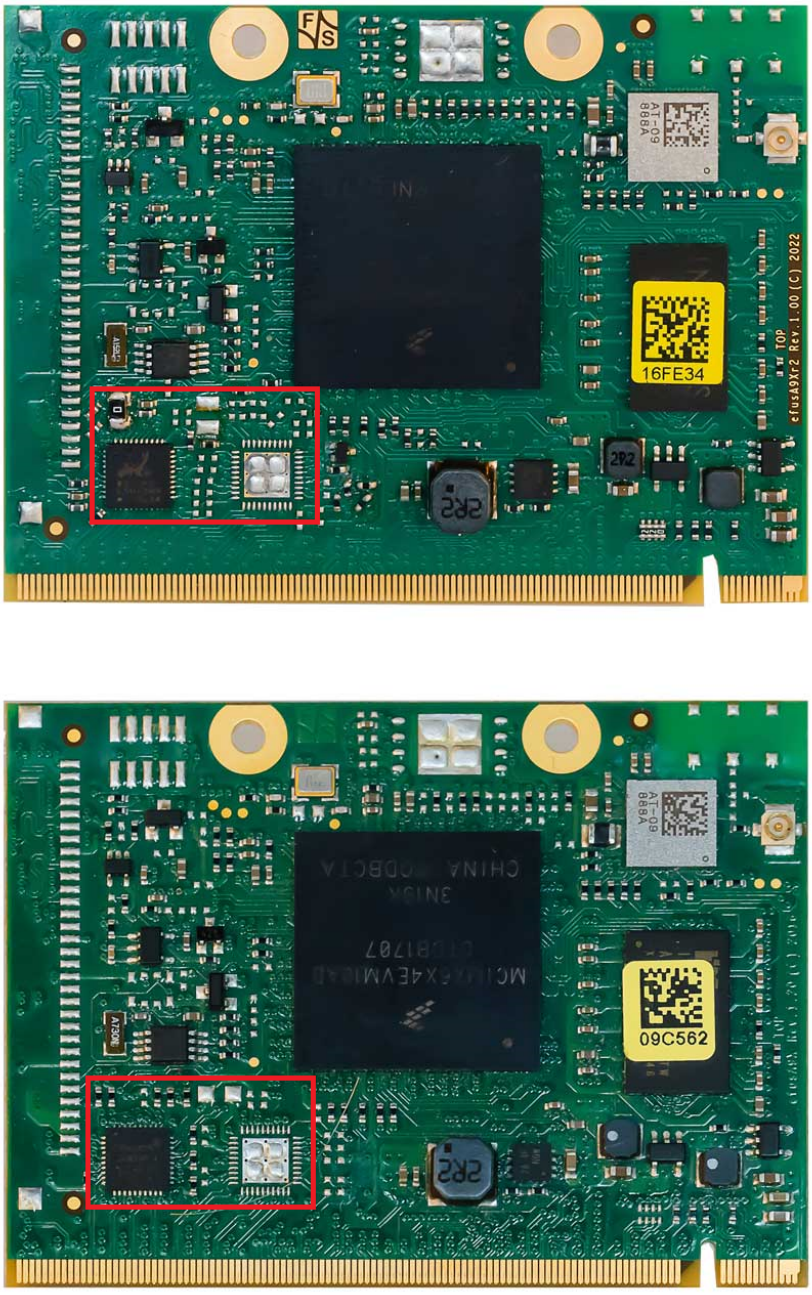


Figure 5: efusA9X (top) vs efusA9Xr2 (bottom)

19 Appendix

Important Notice

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