

# Hardware Documentation

## *ADP-MIPI2LVDS1 for HW Revision 1.20*

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# About This Document

This document describes how to use the [ADP-MIPI2LVDS1](#) adapter board with mechanical and electrical information. The latest version of this document can be found at:

<http://www.fs-net.de>.

## ESD Requirements



All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

## History

Date	V	Platform	A,M,R	Chapter	Description	Au
26.11.2019	000	All		-	Initial Version	MD
27.04.2020	001	All	A	2	Addition of the P/N numbers of connectors and mating parts	MD
04.05.2020	002	All	M	5	Update in chapter 5	MD
13.01.2021	003	All	A,M	All	New Hardware Version 1.10	MD
23.07.2021	004	All	M	All	Bugfixes and new Hardware Version 1.20	MD

V           Version  
A, M, R   Added, Modified, Removed  
Au         Author

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# 1 Physical Characteristics

ADP-MIPI2LVDS1 is an adapter board that is able to convert MIPI-DSI signals into LVDS signals. The board can produce 2-channels of LVDS signals from one channel (4-data lanes) MIPI-DSI signal interface with the usage of Toshiba TC358775. The board can support up to WUXGA 1920 x 1200, 24-bit/pixel or QXGA 2048 x 1536, 18-bit/pixel panel resolutions.

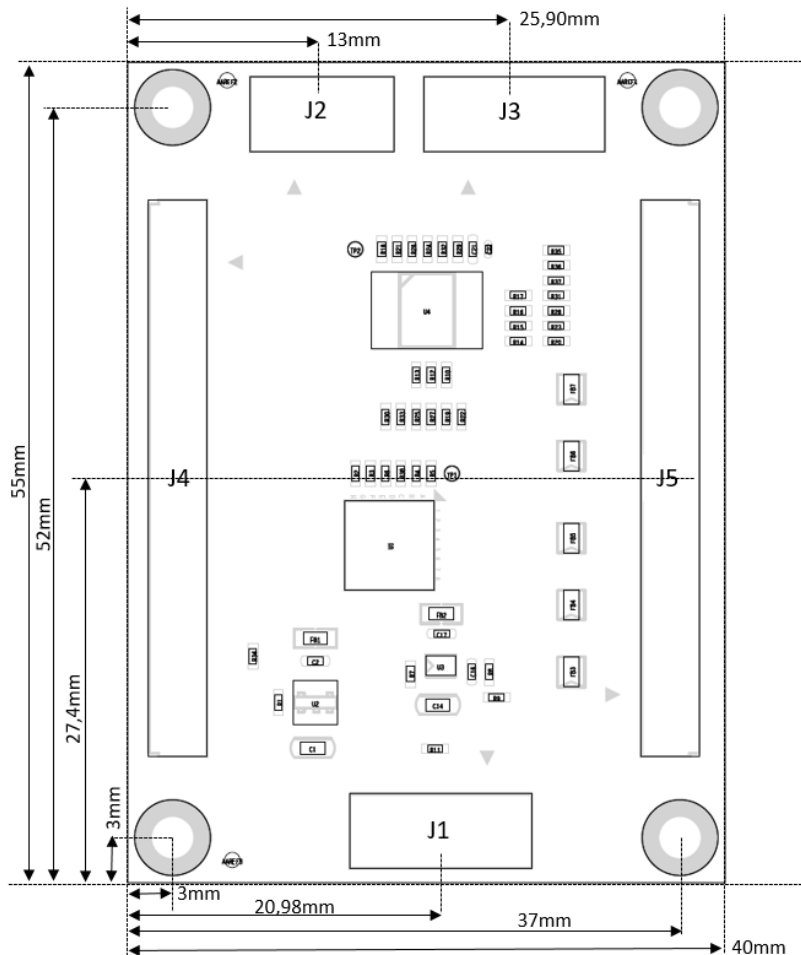


Figure 1: ADP-MIPI2LVDS1 Adapter Board

Dimensions	Description
Size	40mm x 55mm
PCB Thickness	1.66mm ± 0.16mm
Height of the parts on the top side	3.7mm
Height of the parts on the bottom side	0.5mm
Weight	N/A

Table 1: Mechanical Dimensions

## 2 Connector Layout

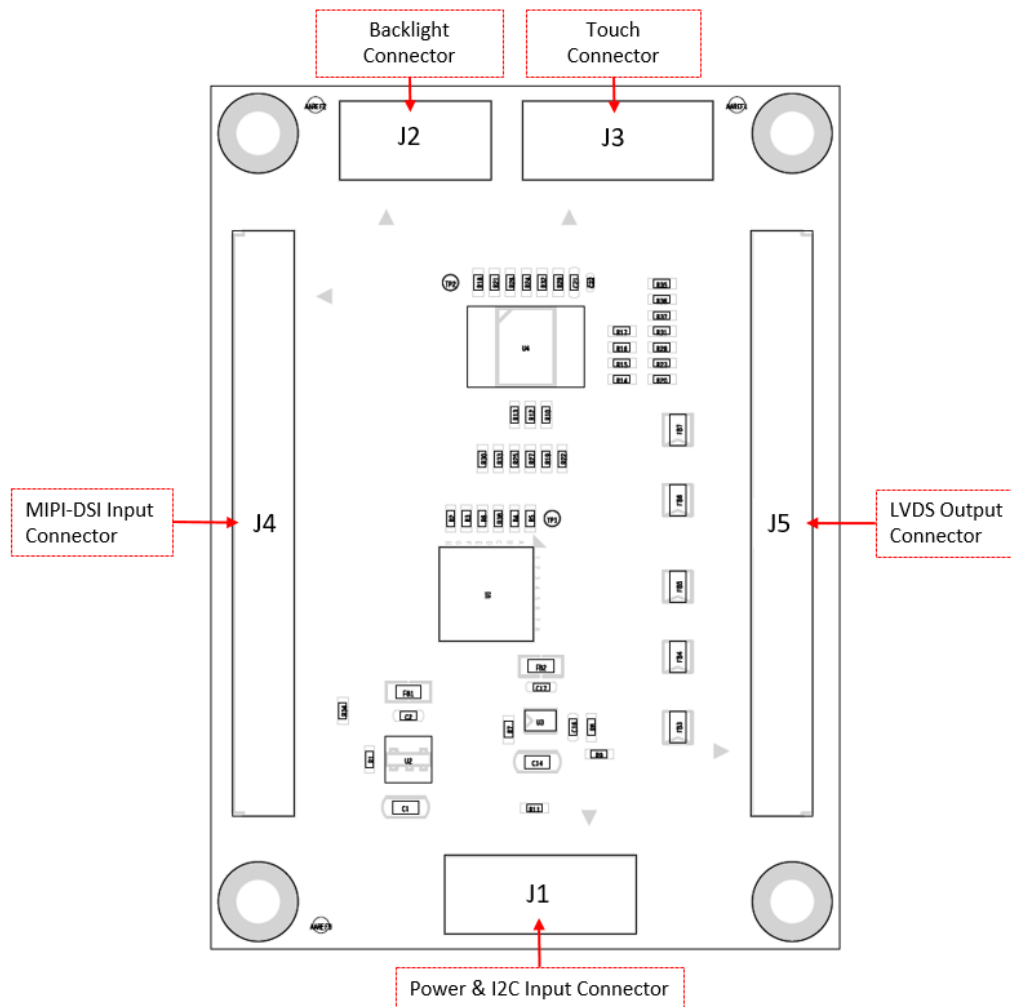


Figure 2: Connector Layout

Ref	Description	I/O	No. of Pins	Connector Type
J1	Power and I2C Connector	Input	6	DF13-6P-1.25H(20)
J2	Backlight Connector	Output	4	DF13-4P-1.25H(20)
J3	Touch Controller Connector	Output	6	DF13-6P-1.25H(20)
J4	MIPI-DSI Connector	Input	30	FI-X30SSLA-HF-R2500
J5	LVDS Connector	Output	30	FI-X30SSLA-HF-R2500
---	Mating Connector for J1 and J3	-	6	DF13-6S-1.25C
---	Mating Connector for J2	-	4	DF13-4S-1.25C
---	Mating Connector for J4 and J5	-	30	FI-X30H & FI-X30HL

Table 2: Connectors List and Types

### 3 Connector Pin Layouts

J4: MIPI-DSI Connector - Input				
Pin	Signal Name	I/O	Voltage	Description
1	MIPI_DSI_D0_N	I		MIPI-DSI Data Lane 0-
2	MIPI_DSI_D0_P	I		MIPI-DSI Data Lane 0+
3	MIPI_DSI_D1_N	I		MIPI-DSI Data Lane 1-
4	MIPI_DSI_D1_P	I		MIPI-DSI Data Lane 1+
5	MIPI_DSI_D0_N	I		MIPI-DSI Data Lane 2-
6	MIPI_DSI_D0_P	I		MIPI-DSI Data Lane 2+
7	GND			
8	MIPI_DSI_CLK_N	I		MIPI-DSI Clock Signal-
9	MIPI_DSI_CLK_P	I		MIPI-DSI Clock Signal+
10	MIPI_DSI_D3_N	I		MIPI-DSI Data Lane 3-
11	MIPI_DSI_D3_P	I		MIPI-DSI Data Lane 3+
12	N.C.	X	X	Not Connected
13	N.C.	X	X	Not Connected
14	GND			
15	N.C.	X	X	Not Connected
16	N.C.	X	X	Not Connected
17	GND			
18	N.C.	X	X	Not Connected
19	N.C.	X	X	Not Connected
20	N.C.	X	X	Not Connected
21	N.C.	X	X	Not Connected
22	N.C.	X	X	Not Connected
23	N.C.	X	X	Not Connected
24	GND			
25	I2C_SDA	I/O	3.3V	I2C Touch-Control Serial Data
26	I2C_IRQn	I	3.3V	I2C Touch-Control Interrupt
27	I2C_SCL	I	3.3V	I2C Touch-Control Clock
28	MIPI_RSTn	I	3.3V	MIPI Reset Signal
29	VLCD	PWR	3.3V	LCD Supply Voltage
30	VLCD	PWR	3.3V	LCD Supply Voltage

Table 3: MIPI-DSI Connector Pin Layout



J5: LVDS Connector - Output				
Pin	Signal Name	I/O	Voltage	Description
1	LVDS_A_DATA0_N	O	1.2V	LVDS A Data Lane 0-
2	LVDS_A_DATA0_P	O	1.2V	LVDS A Data Lane 0+
3	LVDS_A_DATA1_N	O	1.2V	LVDS A Data Lane 1-
4	LVDS_A_DATA1_P	O	1.2V	LVDS A Data Lane 1+
5	LVDS_A_DATA2_N	O	1.2V	LVDS A Data Lane2-
6	LVDS_A_DATA2_P	O	1.2V	LVDS A Data Lane 2+
7	GND			
8	LVDS_A_CLK_N	O	1.2V	LVDS A Clock Signal-
9	LVDS_A_CLK_P	O	1.2V	LVDS A Clock Signal+
10	LVDS_A_DATA3_N	O	1.2V	LVDS A Data Lane 3-
11	LVDS_A_DATA3_P	O	1.2V	LVDS A Data Lane 3+
12	LVDS_B_DATA0_N	O	1.2V	LVDS B Data Lane 0-
13	LVDS_B_DATA0_P	O	1.2V	LVDS B Data Lane 0+
14	GND			
15	LVDS_B_DATA1_N	O	1.2V	LVDS B Data Lane 1-
16	LVDS_B_DATA1_P	O	1.2V	LVDS B Data Lane 1+
17	GND			
18	LVDS_B_DATA2_N	O	1.2V	LVDS B Data Lane 2-
19	LVDS_B_DATA2_P	O	1.2V	LVDS B Data Lane 2+
20	LVDS_B_CLK_N	O	1.2V	LVDS B Clock Signal-
21	LVDS_B_CLK_P	O	1.2V	LVDS B Clock Signal+
22	LVDS_B_DATA3_N	O	1.2V	LVDS B Data Lane 3-
23	LVDS_B_DATA3_P	O	1.2V	LVDS B Data Lane 3+
24	GND			
25	I2C_SDA	I/O	3.3V	I2C Serial Data
26	MIPI_INTn	O	3.3V	MIPI Interrupt Signal
27	I2C_SCL	O	3.3V	I2C Clock Signal
28	MIPI_RSTn	PWR	3.3V	MIPI Reset Signal (optional N.C.)
29	VLCD	PWR	3.3V	LCD Supply Voltage
30	VLCD	PWR	3.3V	LCD Supply Voltage

Table 4: LVDS Connector Pin Layout

J1:Power and I2C Connector - Input				
Pin	Signal Name	I/O	Voltage	Description
1	VDD_3V3	PWR	3.3V	Voltage Power Supply
2	I2C_SDA	I/O	3.3V	I2C Serial Data
3	I2C_SCL	I	3.3V	I2C Clock
4	TOUCH_RSTn	I	3.3V	Touch Reset (optional N.C.)
5	I2C_INTn	I	3.3V	I2C Interrupt
6	GND			

Table 5: Power and I2C Connector Pin Layout

J2:Backlight Connector - Output				
Pin	Signal Name	I/O	Voltage	Description
1	N.C.	X	X	Not Connected
2	BL_ON	O	3.3V	Backlight On (Enable) -> Display
3	BL_PWM	O	3.3V	Backlight PWM -> Display
4	GND			

Table 6: Power and I2C Connector Pin Layout

J3:Touch Controller Connector - Output				
Pin	Signal Name	I/O	Voltage	Description
1	VDD_3V3	PWR	3.3V	Voltage Power Supply -> Display
2	I2C_SDA	I/O	3.3V	I2C Serial Data -> Display
3	I2C_SCL	O	3.3V	I2C Clock -> Display
4	TOUCH_RSTn	O	3.3V	Touch Reset -> Display
5	TOUCH_INTn	O	3.3V	Touch Interrupt -> Display
6	GND			

Table 7: Power and I2C Connector Pin Layout



## 4 Electrical Characteristics

Signal Name	Description	Min	Typ.	Max	Unit
VDD_3V3	Input Supply Voltage	3.0	3.3	3.6	V
VLCD	LCD Supply Voltage	3.0	3.3	3.6	V
GND	Ground	-	-	-	-

Table 8: Electrical Characteristics

## 5 ESD and EMI Implementation

The LVDS data lanes were filtered via ferrite beads in order to reduce the EMI. We highly recommend using the adapter board with wires as short as possible.

ESD Rating of the chip is  $\pm 2$  kV (HBM). The chip has limited built-in ESD protection. There is no ESD protection on the LVDS and MIPI-DSI connectors.

A helpful guide is available from TI; just search for slva680 at ti.com.

## 6 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

## 7 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months

Maximum storage on controlled conditions  $25 \pm 5$  °C, max. 60% humidity: 12 months

For longer storage, we recommend vacuum dry packs.

## 8 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.

Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.

Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

## 9 Packaging

All F&S ESD-sensitive products will shipping either in trays or in bags.

## 10 Matrix Code Sticker

All F&S hardware will ship with a matrix code sticker including the serial number. Enter your serial number here <https://www.fs-net.de/en/support/serial-number-info-and-rma/> to get information on shipping date and type of board.



*Figure 3: Matrix Code Sticker*

# 11 Appendix

## Important Notice

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